OSRAM SFH 5721

Datasheet

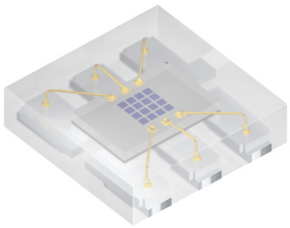
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OSRAM

Chip LED

SFH 5721

Digital Ambient Light Sensor



Applications

- Projection & display

Features

- Package: clear epoxy
- ESD: 2 kV acc. to ANSI/ESDA/JEDEC JS-001 (HBM)
- Adapted to human eye sensitivity (V_λ)
- Integrated and independent Infrared Detection Channel
- I²C Interface
- supports two I²C slave addresses
- Zero dark count value
- 16 Bit ADC resolution

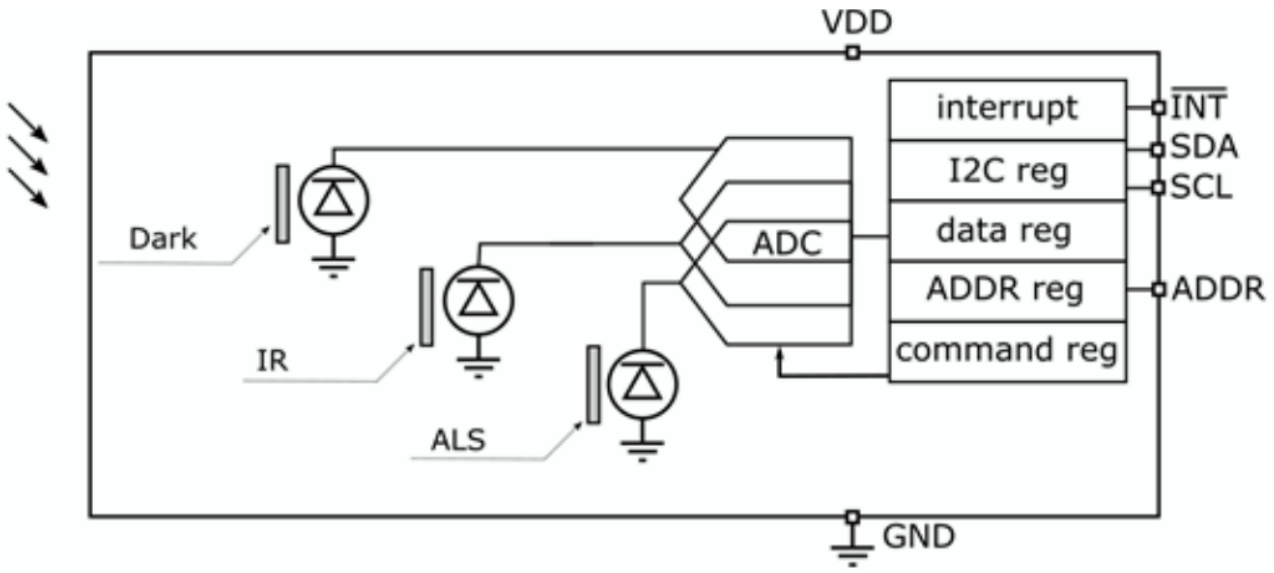
Ordering Information

Type	Ordering Code
SFH 5721	Q65112A9489

General description

The SFH5721 Digital Ambient Light Sensor combines an array of photodiodes and wide dynamic range readout channels to enable ambient light and infrared sensing. In the figure below you can see a simplified block diagram of the digital light sensor IC. The sensor consists of photopic, infrared and dark channel integrated in one single chip. Three integrated ADCs convert the photodiode signal into a digital output which can be accessed by an external microcontroller through I²C. Photopic filter coating deposited on broadband photodiode provides near V lambda response. IR filter coating covering the broadband photodiode provides a response to an IR light. Signal of the dark photodiode is subtracted from the illumined photodiodes and is used for dark current compensation. An Interrupt feature allows to detect a significant change in light intensity. Programmable interrupt threshold register allows the user to define max and min levels above and below a desired light level. Read-out and control of the sensor is accomplished through a two-wire serial I²C interface via set of registers. The user can select two different slave addresses via an external address select pin. Both integration time and gain of the ADC can also be programmed via control register.

Block diagram



Pin description

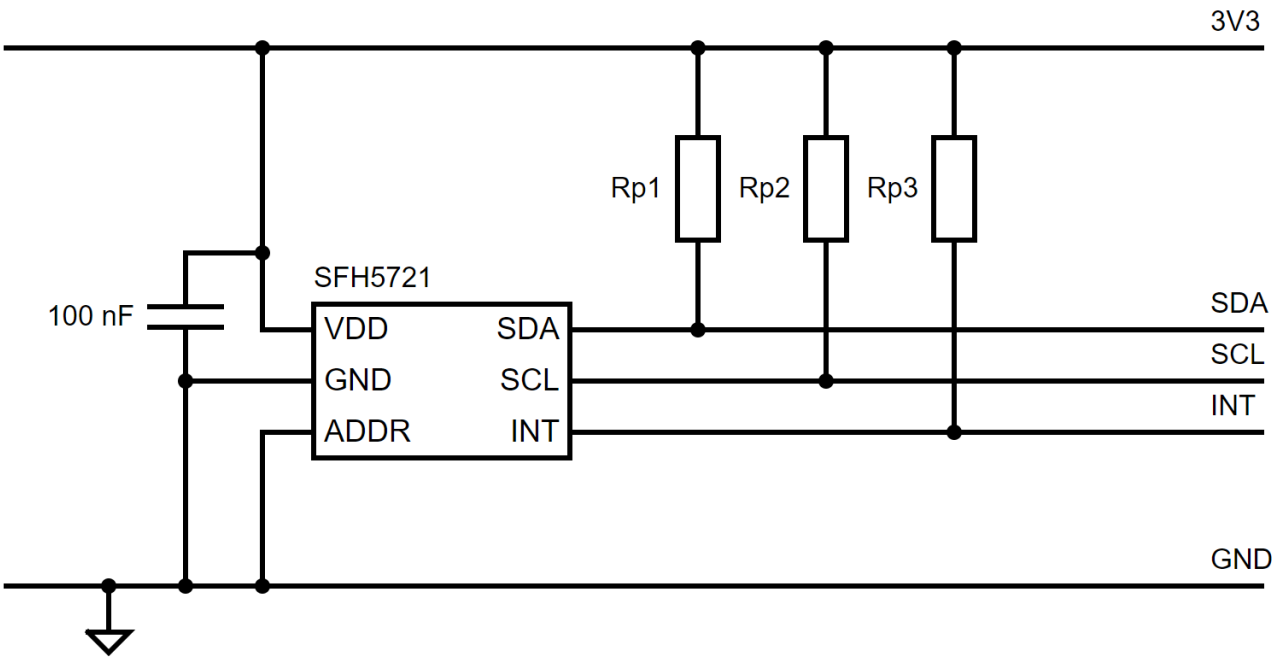
Pin	Name	Function
1	VDD	Power supply pin
2	GND	Ground pin
3	ADDR	Address pin
4	INT	Interrupt pin
5	SCL	I²C bus serial clock pin
6	SDA	I²C bus serial data pin

Channel assignments

Channel	Description
2 (DATA2)	IR channel
3 (DATA3)	ALS channel

Product and Application Information

Application diagram



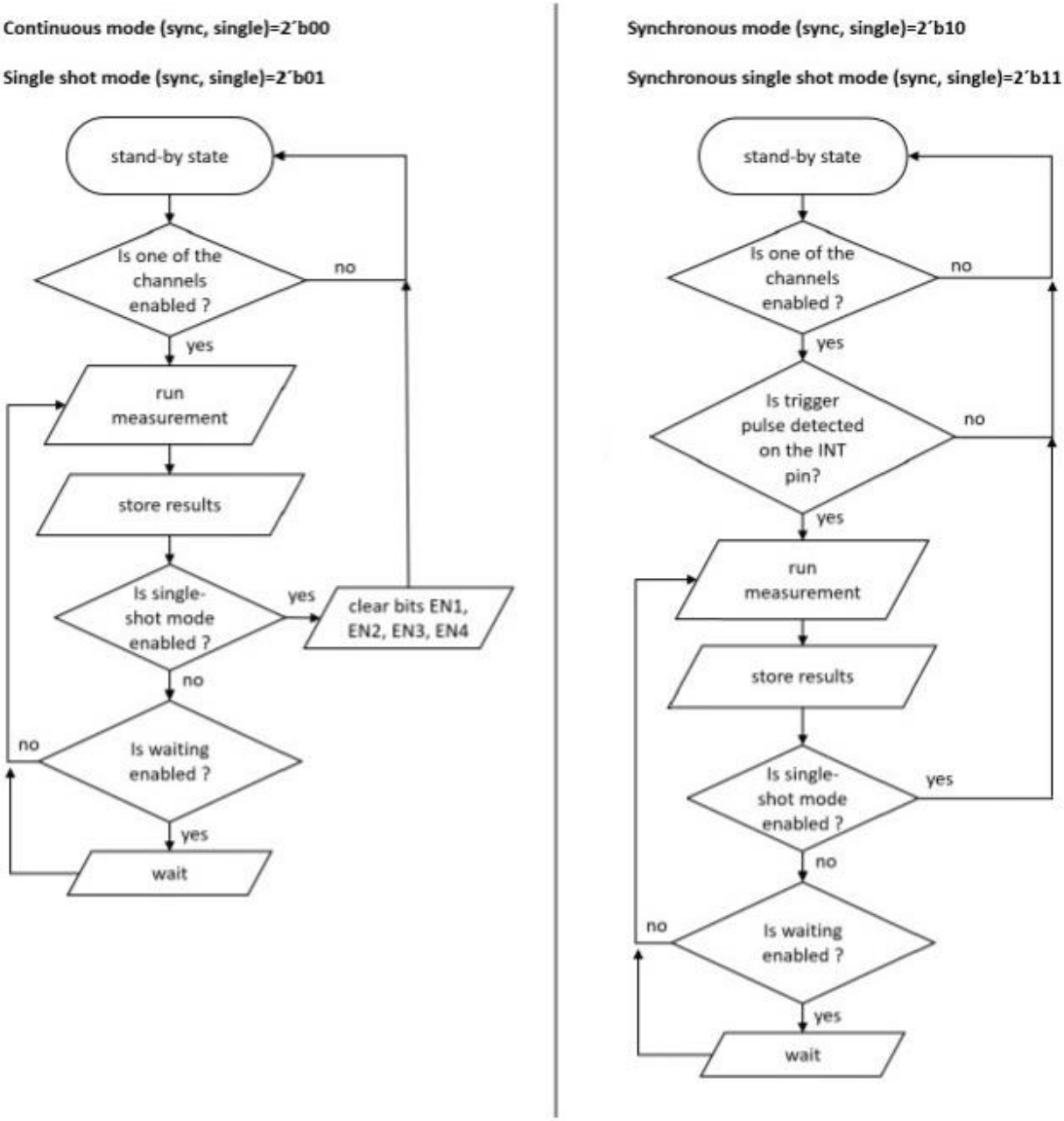
- Bypass capacitors for Vdd are required for proper operation of the device.
- Proposed size for pull-up resistors Rp1, Rp2 and Rp3 are 10kOhm.
- ADDR can be connected to GND or VDD, address depends on the voltage sensed on the ADDR pin.
- I/O-pins are open drain type and logic high level is set with external pull-up resistor to VDD

Measurement modes

Mode	Description
Continuous Mode	In continuous mode, the IC continuously performs measurements. Interrupt pin is configured as output and the interrupt functionality can be configured using interrupt configuration registers. Interrupt persistence can be configured in a way that an interrupt is generated after every measurement. Wait time between measurements can be set by user.
Single-shot Mode	In single-shot mode, the IC performs a single measurement and returns to stand-by state. Single measurement is initiated by I^2C command. Interrupt is disabled in this mode.
Synchronous Mode	In synchronous mode, the IC continuously performs measurements. The start of the measurements is initiated by a negative edge of the pulse detected on the interrupt pin. Interrupt pin is initially configured as input. After initiation of the measurements, the interrupt pin is configured as output. Interrupt functionality can be configured using interrupt configuration registers. Interrupt persistence can be configured in a way that an interrupt is generated after every measurement. Wait time between measurements can be set by user.
Synchronous Single-shot Mode	In synchronous single-shot mode, the IC performs a single measurement and returns to stand-by state. The start of the single measurement is initiated by a negative edge of the pulse detected on the interrupt pin. Interrupt pin is configured as input. Interrupt is disabled in this mode.

State diagram

Measurement state diagram:



Maximum Ratings

Parameter	Symbol		Values
Storage Temperature	T_{stg}	min. max.	-40 °C 100 °C
Operating Ambient Temperature	T_{op}	min. max.	-40 °C 95 °C
Supply Voltage (with respect to GND)	V_{DD}	max.	3.8 V
Input Current	I	min. max.	-20 mA 20 mA
Latch-up acc. to EIA/ JESD78 (Class 2)	$I_{LATCHUPT}$	min.	200 mA
ESD Tolerance HBM acc. to ANSI/ ESDA/ JEDEC JS-001 – HBM, single pulse, both directions	V_{HBM}	max.	2 kV
ESD Tolerance CDM acc. to ANSI/ ESDA/ JEDEC JS-002 – CMD	V_{CDM}	max.	0.75 kV

Recommended operating conditions

T_A = 25 °C

Parameter	Symbol		Values
Supply Voltage [1]	V_{DD}	min. max.	2.1 V 3.6 V
Supply Voltage Rise Time [1]	S_{VDD}	min.	1 V/ ms
Supply Current (Specified for three channels, dark condition, continuous mode, default settings)	I_{VDD}	typ.	265 µA
Shutdown Current (Dark condition, all channels disabled)		typ.	0.315 µA
I²C-Clock Frequency (I²C fast mode)	f_{SCL}	min. max.	0 kHz 400 kHz
SCL, SDA Input High Voltage	V_{BUS}	min. max.	0.53* V_{DD} V_{DD}
INT Output Low Voltage (6 mA sink current)		min. max.	0 V 0.4 V

[1] Both V_{DD} minimum S_{VDD} must be met for guaranteed device operation.

ALS Channel Characteristics

T_A = 25 °C

Parameter	Symbol		Values
Dark Current A_{GAIN} = 256; T_{INT} = 50 ms; Dark Condition	I_d	typ. max.	0 count 11 count
Resolution		typ.	16 bit
Dynamic Range		min. max.	0.001 lx 64000 lx
Sensitivity A_{GAIN} = 256; T_{INT} = 1600 ms	S_{ALS}	typ.	0.00028 lx/ count
Integration Time (Programmable)	T_{int}	min. max.	0.2 ms 1600 ms
Wait Time (Programmable)	T_{wait}	min. max.	0 s 12.8 s
Analog Gain (Programmable)	A_{GAIN}	min. max.	1 256
Startup Time (time after power supply until part reacts to I^2C)	T_{start}	min. typ. max.	2 ms 3 ms 4 ms
IR leakage (% of max. response for wavelengths above 850nm)		typ.	0.7 %
Relative Sensitivity Deviation at 85 °C (Compared to 25°C, V_{DD} = 3 V, A_{GAIN} = 16; T_{INT} = 100 ms)		typ.	-6 %
Field of view (Half-power angle-50% of full power reading; ref. to for specified and measured value)	Φ	typ.	47 °
Spectral angular shift (Validated at 0° - 80° rotation angle)		max.	0.34 nm/°
Photocurrent variation for different light sources (For light source with sharp peaks in photonic range, max. variation of 10% can occur)		max.	10 %
Part to part variation		min. max.	-5 % 5 %

ALS Channel Characteristics (continued)

T_A = 25 °C

Parameter	Symbol		Values
ALS output 1 A_{GAIN} = 1; D_{GAIN} = 1; T_{INT} = 50 ms; E_V = 100 lx	$COUNT_{ALS}$	typ.	50
ALS output 2 A_{GAIN} = 4; D_{GAIN} = 1; T_{INT} = 50 ms; E_V = 100 lx	$COUNT_{ALS}$	typ.	200
ALS output 3 A_{GAIN} = 16; D_{GAIN} = 1; T_{INT} = 50 ms; E_V = 100 lx	$COUNT_{ALS}$	typ.	800
ALS output 4 A_{GAIN} = 128; D_{GAIN} = 1; T_{INT} = 50 ms; E_V = 100 lx	$COUNT_{ALS}$	typ.	6300
ALS output 5 A_{GAIN} = 256; D_{GAIN} = 1; T_{INT} = 50 ms; E_V = 100 lx	$COUNT_{ALS}$	typ.	12500

IR Channel Characteristics

T_A = 25 °C

Parameter	Symbol		Values
Dark Current A_{GAIN} = 256; T_{INT} = 50 ms; Dark Condition	I_d	typ. max.	0 count 11 count
Resolution		typ.	16 bit
Dynamic Range		min. max.	0.00004 µW/ cm² 10000 µW/ cm²
Sensitivity A_{GAIN} = 256; T_{INT} = 1600 ms	S_{IR}	typ.	0.000057 [µW/ cm²]/ count
Integration Time (Value is programmable)	T_{int}	min. max.	0.2 ms 1600 ms
Wait Time (Value is programmable)	T_{wait}	min. max.	0 s 12.8 s
Analog Gain (Value is programmable)	A_{GAIN}	min. max.	1 256
Startup Time (Time after power supply until part reacts to I²C)	T_{start}	min. typ. max.	2 ms 3 ms 4 ms
IR pass filter cutoff frequency		typ.	714 nm
Relative Sensitivity Deviation at 85 °C (Compared to 25°C, V_{DD} = 3 V, A_{GAIN} = 16; T_{INT} = 100 ms)		typ.	15 %
Field of view (Half-power angle-50% of full power reading; ref. to for specified and measured value)	Φ	typ.	55 °
Spectral angular shift (Validated @ 30°-60° rotation angle)		typ.	0.83 nm/°
Part to part variation		min. max.	-5 % 5 %
IR output 1 A_{GAIN} = 1; D_{GAIN} = 1; T_{INT} = 50 ms; E_e = 10 µW/ cm²; λ_c = 850 nm	$COUNT_{IR}$	typ.	26
IR output 2 A_{GAIN} = 4; D_{GAIN} = 1; T_{INT} = 50 ms; E_e = 10 µW/ cm²; λ_c = 850 nm	$COUNT_{IR}$	typ.	102
IR output 3 A_{GAIN} = 16; D_{GAIN} = 1; T_{INT} = 50 ms; E_e = 10 µW/ cm²; λ_c = 850 nm	$COUNT_{IR}$	typ.	410
IR output 4 A_{GAIN} = 128; D_{GAIN} = 1; T_{INT} = 50 ms; E_e = 10 µW/ cm²; λ_c = 850 nm	$COUNT_{IR}$	typ.	3220
IR output 5 A_{GAIN} = 256; D_{GAIN} = 1; T_{INT} = 50 ms; E_e = 10 µW/ cm²; λ_c = 850 nm	$COUNT_{IR}$	typ.	6400

Formulas

The following formulas are used to get from digital COUNTS to the physical units. For the counts of the Ambient Light Channel we calculate the Illuminance in lux. For the Infrared Channel, we calculate the Irradiance in µW/cm². In the Table below, first the formulas and then the different integration time values and their value for the formula are listed. For the calculations you need three variables, digital gain (DGAIN), analog gain (AGAIN) and the right value for the current integration time (IT). These settings are adjustable and defined in the measurement configuration registers (MCONFA and MCONFB) of the sensor.

ALS Channel:

$$E_V[lx] = 512 * \frac{COUNT}{DGAIN * AGAIN * 2^{IT}}$$

IR Channel:

$$E_e[\mu W/cm^2] = 100 * \frac{COUNT}{DGAIN * AGAIN * 2^{IT}}$$

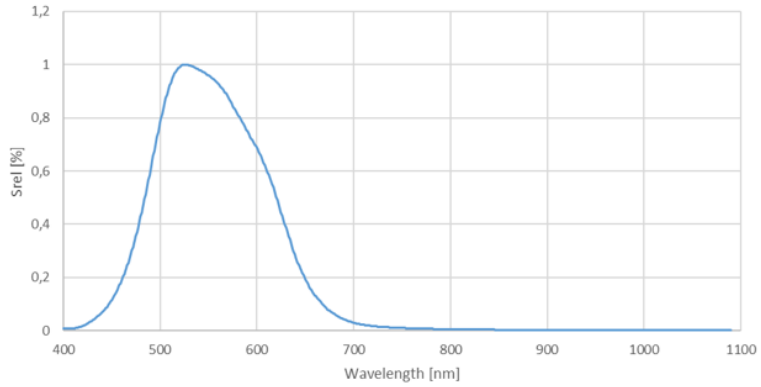
		Maximum ADC Scale	
T_{INT} [ms]	IT	[Bit]	[COUNTS]
0.2	0	9	511
0.4	1	10	1023
0.8	2	11	2047
1.6	3	12	4095
3.1	4	13	8191
6.3	5	14	16383
12.5	6	15	32767
25	7	16	65535
50	8	16	65535
100	9	16	65535
200	10	16	65535
400	11	16	65535
800	12	16	65535
1600	13	16	65535

T_{INT} = Integration Time in ms
IT = Integration Time Setting

Diagrams

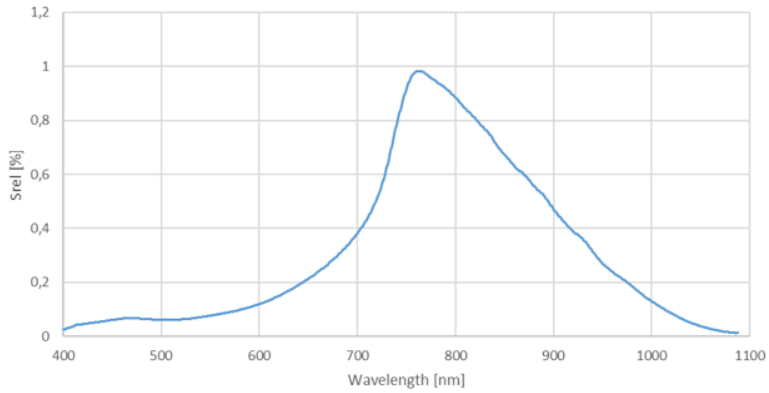
Relative Spectral Sensitivity

$S_{rel} = f(\lambda)$; ALS channel



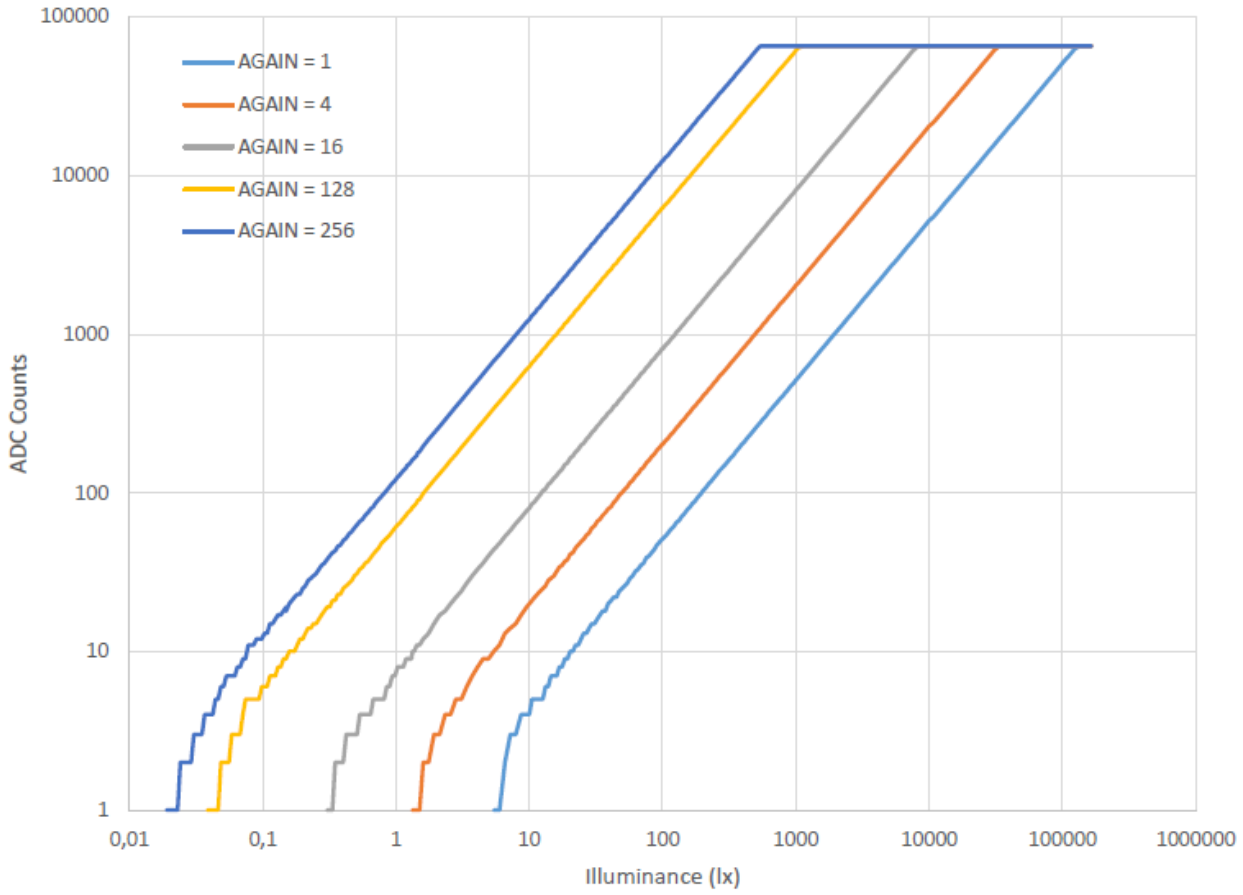
Relative Spectral Sensitivity

$S_{rel} = f(\lambda)$; IR channel



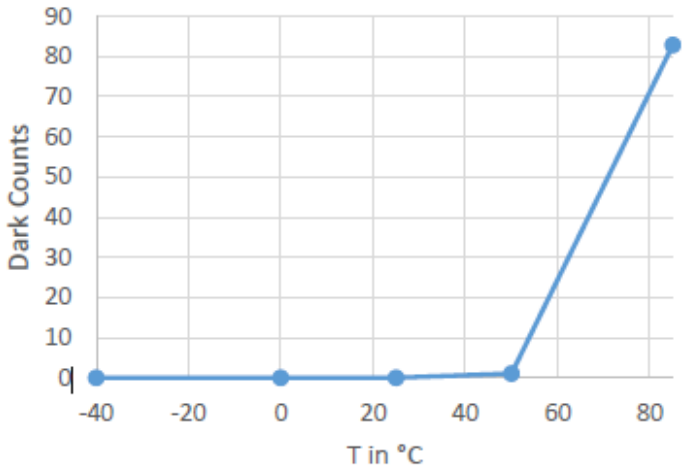
Output ALS Channel

T_{int} = 50ms, D_{GAIN} = 1, Light source = White LED

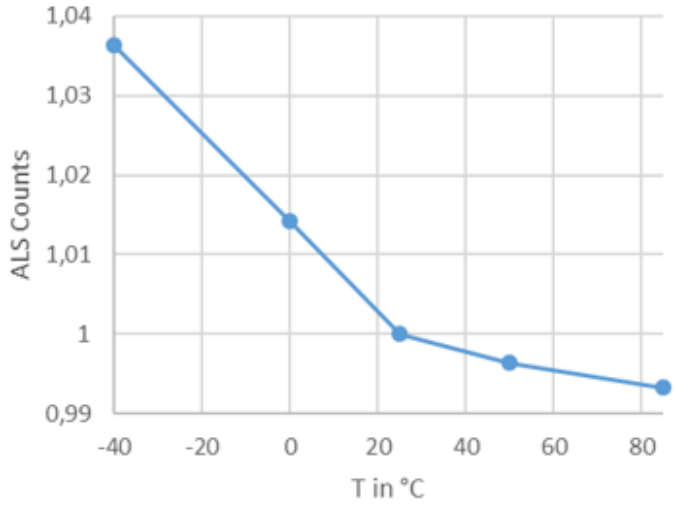


Dark Counts

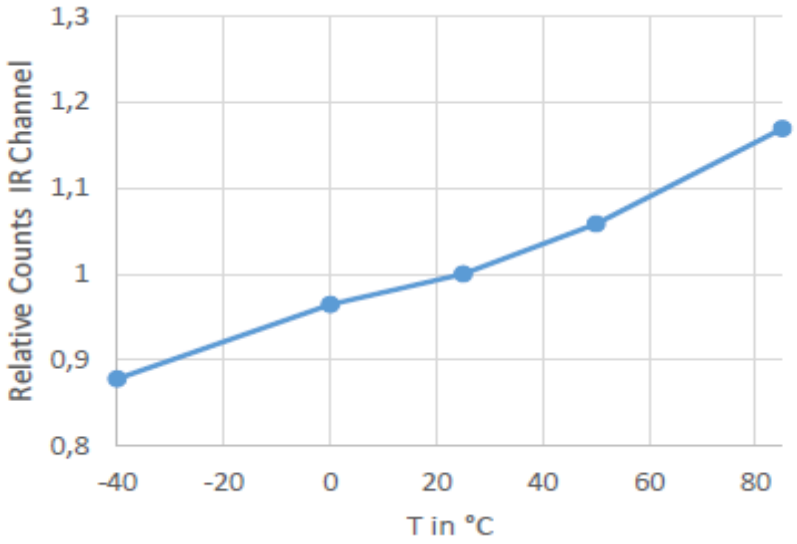
AGAIN = 256; T_{int} = 1.6s; Register 0x0A (MCONFB) bit 4 = 0



Output Counts ALS Channel

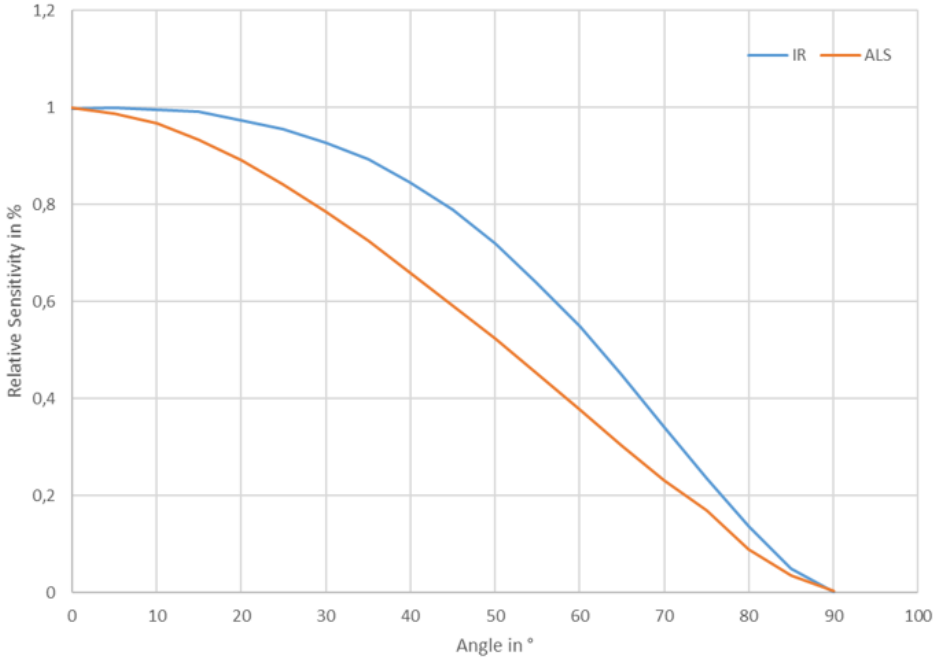


Output Counts IR Channel



Directional Characteristics

(both horizontal and vertical)



Register Set

The Digital Light Sensor (DLS) IC is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

For guaranteed startup operation (specifically with a low V_{DD} voltage and a slow V_{DD} rise time) the following sequence is recommended immediately following power up:

Sequence	Description
1.	V_{DD} power up
2.	Wait 5 ms
3.	Start I²C-addr, 0x62, 0x55, stop
4.	Start I²C-addr, 0xEC, stop
5.	Wait 5 ms
6.	IC is ready for use

Pointer Register

I²C Pointer Register

Bit	NAME	R/W	Default	Description
7:6	-	R/W	00	Not used
5:0	REGSEL[5:0]	R/W	00 0000	Register Select

The SFH 5721 operates in slave mode and is designed for I²C fast mode (400 kHz). The I²C pointer register is used to select a register for I²C reading and writing. For the selection of the different SFH 5721 registers you only need 6 bits, B6 and B7 must be 0.

Register Map (Default State)

REGISTER ADDR	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W	REGISTER FUNCTION
0x00	OPSEL	RESET	-[3]	SYNC	SINGLE	-	EN3	EN2	EN1	R/W	Operation selection
		0	0	0	0	0	0	0	0		
0x01	STAT	-	-	-	-	-	DRY3	DRY2	DRY1	R	Status register
		0	0	0	0	0	0	0	0		
0x02	IEN	-	-	IENH3	IENL3	IENH2	IENL2	IENH1	IENL1	R/W	Interrupt enable register
		0	0	0	0	0	0	0	0		
0x03	ICONF	-	-	ICC	IOA	IPERS[3:0]				R/W	Interrupt configuration register
		0	0	0	0	0	0	0	0		
0x04	ILTL	ILTL[7:0]								R/W	Interrupt low threshold low register (LSB)
		0	0	0	0	0	0	0	0		
0x05	ILTH	ILTH[7:0]								R/W	Interrupt low threshold high register (LSB)
		0	0	0	0	0	0	0	0		
0x06	IHTL	IHTL[7:0]								R/W	Interrupt high threshold low register (LSB)
		1	1	1	1	1	1	1	1		
0x07	IHTH	IHTH[7:0]								R/W	Interrupt high threshold high register (MSB)
		1	1	1	1	1	1	1	1		
0x08	IFLAG	-	-	IFHT3	IFLT3	IFHT2	IFLT2	IFHT1	IFLT1	R	Interrupt flag register
		0	0	0	0	0	0	0	0		
0x09	MCONFA	-	IT[3:0]				AGAIN[2:0]			R/W	Measurement configuration register A
		0	1	0	0	0	0	0	0		
0x0A	MCONFB	DGAIN[2:0]			SUB	WAIT[3:0]				R/W	Measurement configuration register B
		0	0	0	1	0	0	0	0		
0x0B	MCONFC	-	-	LPFDEPTH[1:0]		-	LPFEN3	LPFEN2	LPFEN1	R/W	Measurement configuration register C
		0	0	0	0	0	0	0	0		
0x0C	DATA1L[1]	DATA1L[7:0]								R	Dark Data low byte register (readout 1)
		0	0	0	0	0	0	0	0		

Register Map (continued)

REGISTER ADDR	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W	REGISTER FUNCTION
0x0D	DATA1H[1]	DATA1H[7:0]								R	Dark Data high byte register (readout 1)
		0	0	0	0	0	0	0	0		
0x0E	DATA2L[1]	DATA2L[7:0]								R	IR Data low byte register (readout 2)
		0	0	0	0	0	0	0	0		
0x0F	DATA2H[1]	DATA2H[7:0]								R	IR Data high byte register (readout 2)
		0	0	0	0	0	0	0	0		
0x10	DATA3L[1]	DATA3L[7:0]								R	ALS Data low byte register (readout 3)
		0	0	0	0	0	0	0	0		
0x11	DATA3H[1]	DATA3H[7:0]								R	ALS Data low byte register (readout 3)
		0	0	0	0	0	0	0	0		
0x14	DEVID[2]	-	-	-	-	DEVID[3:0]				R	Device ID register
		0	0	0	0	0	0	0	1		

[1] The data registers are not updated while read is in progress. The update is delayed until the read is finished.
[2] Calibration bits indicating Device ID are read into user register 0d20 during startup.
[3] “-“ = not used, always set to 0.

Operation Selection Register (OPSEL)

0x00

Bit	NAME	R/W	Default	Description
7	RESET	R/W	0	Reset to Default State
6	-	R/W	0	Not used
5	SYNC	R/W	0	Synchronous Mode
4	SINGLE	R/W	0	Single-shot Mode
3	-	R/W	0	Not used
2	EN3	R/W	0	Enable Control ALS Channel
1	EN2	R/W	0	Enable Control IR Channel
0	EN1	R/W	0	Enable Control Dark Channel

The OPSEL register is used for selecting the operation of the IC.

The EN1 to EN3 bits are used for enabling the four readout channels. The SINGLE bit is used to enable the single-shot operation mode. In single-shot operation mode a single measurement is performed after which the circuit returns to standby. In single shot mode, the interrupt function is disabled. The SYNC bit is used to enable the synchronous operation mode. In synchronous operation mode, interrupt pin is used as input to enable the start of the measurement. The measurement is started with the negative edge of the INT pin. The safest way of enabling SYNC mode is by first making INT bit HIGH and then enabling the SYNC. The RESET bit is used for restoring the default register settings. Writing a ‘1’ to the RESET bit will restore the default settings.

If a measurement is running, writing OPSEL register will restart the measurement. This is only the case if one of the EN1 to EN3 bits are set to ‘1’ with this I^2C write.

EN1	OPERATION
0	Readout Dark channel is disabled
1	Readout Dark channel is enabled

EN2	OPERATION
0	Readout IR channel is disabled
1	Readout IR channel is enabled

EN3	OPERATION
0	Readout ALS channel is disabled
1	Readout ALS channel is enabled

SINGLE	OPERATION
0	Single-shot mode of operation is disabled
1	Single-shot mode of operation is enabled

SYNC	OPERATION
0	Synchronous mode is disabled
1	Synchronous mode is enabled

RESET	OPERATION
0	Reset function is disabled
1	Default register settings are restored

Status Register (STAT)

0x01

Bit	NAME	R/W	Default	Description
7:3	-	R/W	00000	Not used
2	DRY3	R/W	0	Data Ready Status ALS Channel
1	DRY2	R/W	0	Data Ready Status IR Channel
0	DRY1	R/W	0	Data Ready Status Dark Channel

The STAT register is used for checking the status of the measurement data. The DRY bits indicate whether new results are available. These status bits are cleared when the new measurement results have been read (DATA registers).

DRY1	OPERATION
0	Data ready is cleared or not triggered yet.
1	Data ready is triggered. The status bit is cleared after data register DATA1H is read.

DRY2	OPERATION
0	Data ready is cleared or not triggered yet.
1	Data ready is triggered. The status bit is cleared after data register DATA2H is read.

DRY3	OPERATION
0	Data ready is cleared or not triggered yet.
1	Data ready is triggered. The status bit is cleared after data register DATA3H is read.

Interrupt Enable Register (IEN)

0x02

Bit	NAME	R/W	Default	Description
7:6	-	R/W	00	Not used
5	IENH3	R/W	0	Interrupt Enable High Threshold ALS Channel
4	IENL3	R/W	0	Interrupt Enable Low Threshold ALS Channel
3	IENH2	R/W	0	Interrupt Enable High Threshold IR Channel
2	IENL2	R/W	0	Interrupt Enable Low Threshold IR Channel
1	IENH1	R/W	0	Interrupt Enable High Threshold Dark Channel
0	IENL1	R/W	0	Interrupt Enable Low Threshold Dark Channel

The IEN register is used to enable the interrupt functions of the IC. Both IEL and IEH of a channel must be set to HIGH, to activate interrupt functionality of this single channel.

IENL1	OPERATION
0	Readout Dark low threshold interrupt function is disabled
1	Readout Dark low threshold interrupt function is enabled

IENH1	OPERATION
0	Readout Dark high threshold interrupt function is disabled
1	Readout Dark high threshold interrupt function is enabled

IENL2	OPERATION
0	Readout IR low threshold interrupt function is disabled
1	Readout IR low threshold interrupt function is enabled

IENH2	OPERATION
0	Readout IR high threshold interrupt function is disabled
1	Readout IR high threshold interrupt function is enabled

IENL3	OPERATION
0	Readout ALS low threshold interrupt function is disabled
1	Readout ALS low threshold interrupt function is enabled

IENH3	OPERATION
0	Readout ALS high threshold interrupt function is disabled
1	Readout ALS high threshold interrupt function is enabled

Interrupt Configuration Register (ICONF)

0x03

Bit	NAME	R/W	Default	Description
7:6	-	R/W	00	Not used
5	ICC	R/W	0	Interrupt Clear Configuration
4	IOA	R/W	0	Interrupt Or-And Configuration
3:0	IPERS[3:0]	R/W	0000	Persistence Configuration

The ICONF register is used to configure the interrupt function of the IC. The register controls the filtering interrupt capability of the device by IPERS[3:0] bits. Configurable filtering is provided to allow interrupts to be generated after each ADC integration cycle or if the ADC integration has produced a result that is outside of the values specified by high or low threshold register for some specified amount of time. When multiple readout channels are enabled, IOA (Interrupt-Or-And) bit determine if interrupt is generated when a single channel generates the interrupt (Or) or if all enabled channels whose interrupt is enabled generate the interrupt (And). Clearing of the interrupt is configured by ICC bit. If one of the Single Shot Modes is activated, the interrupt is activated for 24µs only and then released again.

IPERS[3:0]	OPERATION
0000	Every cycle generates an interrupt
0001	1 value out of range generates an interrupt
0010	2 consecutive values out of range generate an interrupt
…	…
…	…
1101	13 consecutive values out of range generate an interrupt
1110	14 consecutive values out of range generate an interrupt
1111	15 consecutive values out of range generate an interrupt

IOA	OPERATION
0	Interrupt is generated if a single readout channel generates the interrupt
1	Interrupt is generated if all enabled readout channels generate the interrupt

ICC	OPERATION
0	Interrupt is cleared when IFLAG register is read
1	Interrupt is cleared when any one of the eight DATA1L to DATA4H register is read

Interrupt Low Threshold LSB Register (ILTL)

0x04

Bit	NAME	R/W	Default	Description
7:0	ILTL[7:0]	R/W	0000 0000	Low Threshold Low Byte (LSB)

The ILTL and ILTH interrupt threshold registers are used as the low trigger point for the comparison function for the interrupt generation. If the value generated by the ADC conversion crosses below the specified low threshold, an interrupt is asserted on the interrupt pin.

Interrupt Low Threshold MSB Register (ILTH)

0x05

Bit	NAME	R/W	Default	Description
7:0	ILTH[7:0]	R/W	0000 0000	Low Threshold High Byte (MSB)

The ILTL and ILTH interrupt threshold registers are used as the low trigger point for the comparison function for the interrupt generation. If the value generated by the ADC conversion crosses below the specified low threshold, an interrupt is asserted on the interrupt pin.

Interrupt High Threshold LSB Register (IHTL)

0x06

Bit	NAME	R/W	Default	Description
7:0	IHTL[7:0]	R/W	1111 1111	High Threshold Low Byte (LSB)

The IHTL and IHTH interrupt threshold registers are used as the high trigger point for the comparison function for the interrupt generation. If the value generated by the ADC conversion crosses above the specified high threshold, an interrupt is asserted on the interrupt pin.

Interrupt High Threshold MSB Register (IHTH)

0x07

Bit	NAME	R/W	Default	Description
7:0	IHTH[7:0]	R/W	1111 1111	High Threshold High Byte (MSB)

The IHTL and IHTH interrupt threshold registers are used as the high trigger point for the comparison function for the interrupt generation. If the value generated by the ADC conversion crosses above the specified high threshold, an interrupt is asserted on the interrupt pin.

Interrupt Flag Register (IFLAG)

0x08

Bit	NAME	R/W	Default	Description
7:6	-	R/W	00	Not used
5	IFHT3	R/W	0	Interrupt Flag high side ALS Channel
4	IFLT3	R/W	0	Interrupt Flag low side ALS Channel
3	IFHT2	R/W	0	Interrupt Flag high side IR Channel
2	IFLT2	R/W	0	Interrupt Flag low side IR Channel
1	IFHT1	R/W	0	Interrupt Flag high side Dark Channel
0	IFLT1	R/W	0	Interrupt Flag low side Dark Channel

The IFLAG register is used to register the appropriate interrupt event. Once an interrupt is triggered, it can only be cleared by the master. Reading the IFLAG register (DATA1L register if ICC is set to ‘1’) or issuing a RESET command or enabling the synchronous mode together with single-shot mode will clear the interrupt flag register.

IFLT1	OPERATION
0	Readout Dark low side interrupt is cleared or not triggered yet.
1	Readout Dark low side interrupt is triggered. The interrupt is cleared when IFLAG (DATA1L*) register is read.

IFHT1	OPERATION
0	Readout Dark high side interrupt is cleared or not triggered yet.
1	Readout Dark high side interrupt is triggered. The interrupt is cleared when IFLAG (DATA1L*) register is read.

IFLT2	OPERATION
0	Readout IR low side interrupt is cleared or not triggered yet.
1	Readout IR low side interrupt is triggered. The interrupt is cleared when IFLAG (DATA1L*) register is read.

IFHT2	OPERATION
0	Readout IR high side interrupt is cleared or not triggered yet.
1	Readout IR high side interrupt is triggered. The interrupt is cleared when IFLAG (DATA1L*) register is read.

IFLT3	OPERATION
0	Readout ALS low side interrupt is cleared or not triggered yet.
1	Readout ALS low side interrupt is triggered. The interrupt is cleared when IFLAG (DATA1L*) register is read.

IFHT3	OPERATION
0	Readout ALS high side interrupt is cleared or not triggered yet.
1	Readout ALS high side interrupt is triggered. The interrupt is cleared when IFLAG (DATA1L*) register is read.

* ICC bit (BIT5 in ICONF (0x03)) defines if interrupt is cleared by reading IFLAG or DATA1L register.

Measurement Configuration Register A (MCONFA)

0x09

Bit	NAME	R/W	Default	Description
7	-	R/W	0	Not used
6:3	IT[3:0]	R/W	1000	Integration Time Selection
2:0	AGAIN[2:0]	R/W	000	Analog Gain Selection

The MCONFA register is used to set the analog gain and the ADC integration time of the measurements. If a measurement is running, writing MCONFA will restart the measurement.

AGAIN[2:0]	OPERATION
000	Analog gain is 1
001	Analog gain is 4
010	Analog gain is 16
011	Analog gain is 128
100 to 111	Analog gain is 256

IT[3:0]	OPERATION
0000	Integration time is 0.2ms
0001	Integration time is 0.4ms
0010	Integration time is 0.8ms
0011	Integration time is 1.6ms
0100	Integration time is 3.1ms
0101	Integration time is 6.3ms
0110	Integration time is 12.5ms
0111	Integration time is 25ms
1000	Integration time is 50ms
1001	Integration time is 100ms
1010	Integration time is 200ms
1011	Integration time is 400ms
1100	Integration time is 800ms
1101 to 1111	Integration time is 1600ms

Measurement Configuration Register B (MCONFB)

0x0A

Bit	NAME	R/W	Default	Description
7:5	DGAIN[2:0]	R/W	000	Digital Gain Selection
4	SUB	R/W	1	Subtraction Selection for Dark Current Compensation
3:0	WAIT[3:0]	R/W	0000	Wait Time Selection

The MCONFB register is used to set the wait time between the measurements, to configure the subtraction option of the IC and to set the digital gain of the measurement. The subtraction option is useful if a single readout channel is used for measuring ‘dark’ leakage current. This ‘dark’ leakage current can be subtracted digitally from other channels on the IC to compensate for the temperature dependent leakage current. If a measurement is running, writing MCONFB will restart the measurement.

WAIT[3:0]	OPERATION*
0000	Wait time between measurements is 0 * 6.1 µs (0 ms)
0001	Wait time between measurements is 2^7 * 6.1 µs (0.78 ms)
0010	Wait time between measurements is 2^8 * 6.1 µs (1.56 ms)
0011	Wait time between measurements is 2^9 * 6.1 µs (3.12 ms)
0100	Wait time between measurements is 2^10 * 6.1 µs (6.24 ms)
0101	Wait time between measurements is 2^11 * 6.1 µs (12.5 ms)
0110	Wait time between measurements is 2^12 * 6.1 µs (25 ms)
0111	Wait time between measurements is 2^13 * 6.1 µs (50 ms)
1000	Wait time between measurements is 2^14 * 6.1 µs (100 ms)
1001	Wait time between measurements is 2^15 * 6.1 µs (200 ms)
1010	Wait time between measurements is 2^16 * 6.1 µs (400 ms)
1011	Wait time between measurements is 2^17 * 6.1 µs (800 ms)
1100	Wait time between measurements is 2^18 * 6.1 µs (1.6 s)
1101	Wait time between measurements is 2^19 * 6.1 µs (3.2 s)
1110	Wait time between measurements is 2^20 * 6.1 µs (6.4 s)
1111	Wait time between measurements is 2^21 * 6.1 µs (12.8s)

* 6.1us = PCLKS = period of the low power clock (CLKS) which has a frequency of 164kHz.

SUB	OPERATION
0	Subtraction is disabled
1	Readout 1 data is used for subtraction from other readout channels

DGAIN[2:0]	OPERATION
000	Digital gain is 1
001	Digital gain is 2
010	Digital gain is 4
011	Digital gain is 8
1xx	Digital gain is 16

Measurement Configuration Register C (MCONFC)

0x0B

Bit	NAME	R/W	Default	Description
7:6	-	R/W	00	Not used
5:4	LPFDEPTH[1:0]	R/W	00	Lowpass Filter Depth Selection
3	-	R/W	0	Not used
2	LPFEN3	R/W	0	Lowpass Filter Enable ALS Channel
1	LPFEN2	R/W	0	Lowpass Filter Enable IR Channel
0	LPFEN1	R/W	0	Lowpass Filter Enable Dark Channel

The MCONFC register is used to configure the digital low pass filtering of the measurement data. If a measurement is running, writing MCONFC will restart the measurement.

LPFEN1	OPERATION
0	Digital lowpass filtering of readout Dark data is disabled
1	Digital lowpass filtering of readout Dark data is enabled

LPFEN2	OPERATION
0	Digital lowpass filtering of readout IR data is disabled
1	Digital lowpass filtering of readout IR data is enabled

LPFEN3	OPERATION
0	Digital lowpass filtering of readout ALS data is disabled
1	Digital lowpass filtering of readout ALS data is enabled

LPFDEPTH[1:0]	OPERATION
00	Digital lowpass filter depth is 2
01	Digital lowpass filter depth is 3
10	Digital lowpass filter depth is 4
11	Digital lowpass filter depth is 5

Data 1 LSB Register (DATA1L)

0x0C

Bit	NAME	R/W	Default	Description
7:0	DATA1L[7:0]	R/W	0000 0000	Data Low Byte Dark Channel

The DATA1L and DATA1H registers are used to store the data of readout Dark channel.

Data 1 MSB Register (DATA1H)

0x0D

Bit	NAME	R/W	Default	Description
7:0	DATA1H[7:0]	R/W	0000 0000	Data High Byte Dark Channel

The DATA1L and DATA1H registers are used to store the data of readout Dark channel.

Data 2 LSB Register (DATA2L)

0x0E

Bit	NAME	R/W	Default	Description
7:0	DATA2L[7:0]	R/W	0000 0000	Data Low Byte IR Channel

The DATA2L and DATA2H registers are used to store the data of readout IR channel.

Data 2 MSB Register (DATA2H)

0x0F

Bit	NAME	R/W	Default	Description
7:0	DATA2H[7:0]	R/W	0000 0000	Data High Byte IR Channel

The DATA2L and DATA2H registers are used to store the data of readout IR channel.

Data 3 LSB Register (DATA3L)

0x10

Bit	NAME	R/W	Default	Description
7:0	DATA3L[7:0]	R/W	0000 0000	Data Low Byte ALS Channel

The DATA3L and DATA3H registers are used to store the data of readout ALS channel.

Data 3 MSB Register (DATA3H)

0x11

Bit	NAME	R/W	Default	Description
7:0	DATA3H[7:0]	R/W	0000 0000	Data High Byte ALS Channel

The DATA3L and DATA3H registers are used to store the data of readout ALS channel.

Device ID Number (DEVID)

0x14

Bit	NAME	R/W	Default	Description
7:4	-	R/W	0000	Not used
3:0	DEVID[3:0]	R/W	0001	Device ID Number

The DEVID register is used to provide the silicon part number.

Sample Code

This section introduces you to a very basic dummy code for implementation of the Sensor. The write and read register functions are hardware dependent. The following code example shows you how to reset the sensor, do the interrupt a measurement configuration and finally how to start and get data from the sensor.

Reset:

```
// Reset Sensor to default state
I2C_8_write_register(0x00, 0b10000000);   // Reset in Operation selection register
```

Example Configuration:

```
// Example Configurate for interrupt settings
I2C_8_write_register(0x02, 0b00110000);   // Enable High & Low IR for ALS Channel
I2C_8_write_register(0x03, 0b00100000);   // Configurate IR settings
I2C_8_write_register(0x04, 0b11001100);   // Define Low Threshold LSB (30% of 16bit)
I2C_8_write_register(0x05, 0b01001100);   // Define Low Threshold MSB (30% of 16bit)
I2C_8_write_register(0x06, 0b11111111);   // Define High Threshold LSB (75% of 16bit)
I2C_8_write_register(0x07, 0b10111111);   // Define High Threshold MSB (75% of 16bit)

// Example Configuration for measurement settings
I2C_8_write_register(0x09, 0b00111001);   // Set AGAIN=4 & IT=25ms in MCONFA
I2C_8_write_register(0x0A, 0b00011000);   // Set Wait=100ms & DGAIN=1 in MCONFB
I2C_8_write_register(0x0B, 0b00010100);   // Set LPFDEPTH=3 & enable Filter in MCONFC
```

Enable:

```
// Start Procedure by enabling required mode and channel
I2C_8_write_register(0x00, 0b00000100);   // Enable Async Continuous mode & ALS Channel
```

Readout manually or after number of interrupts:

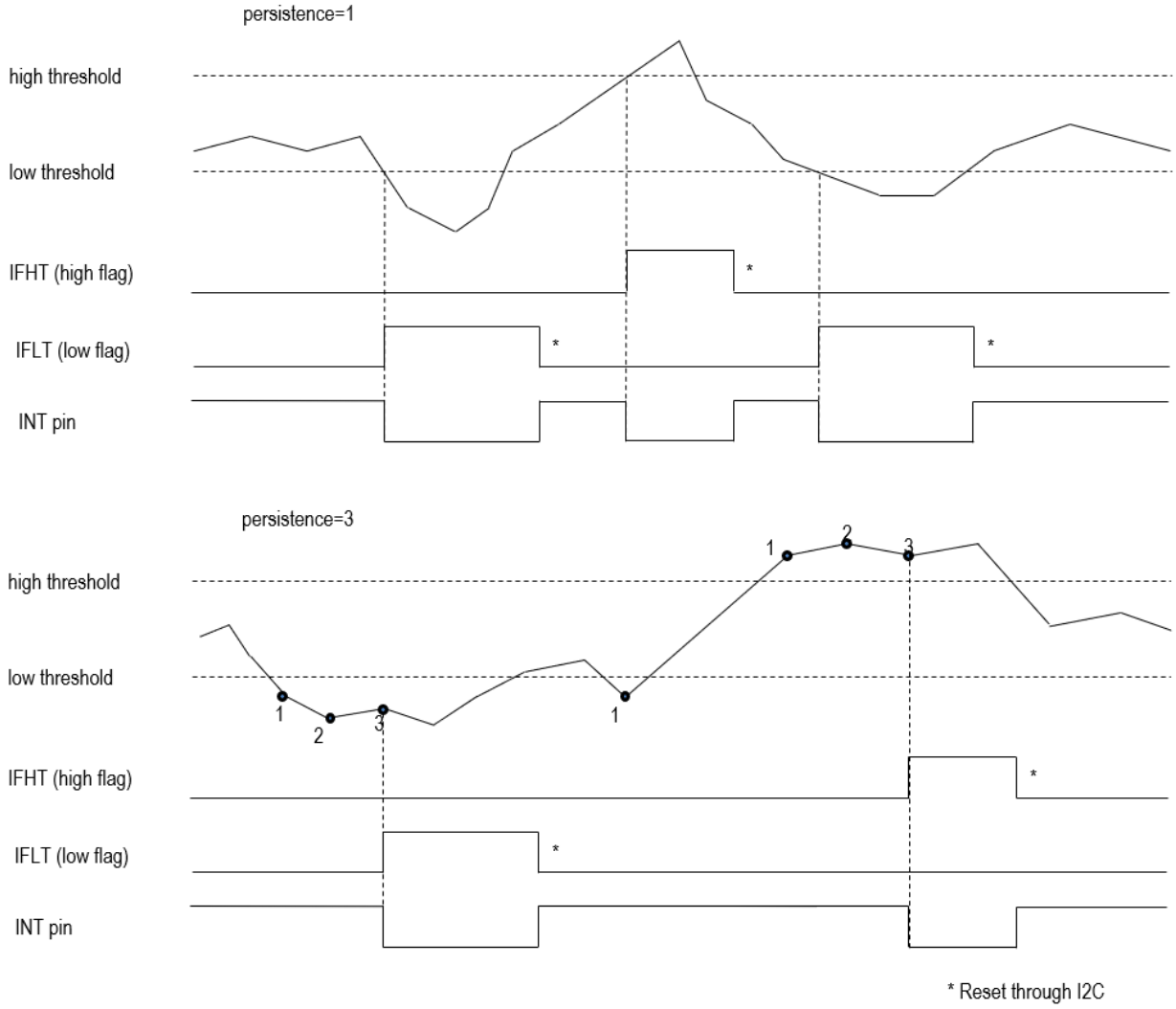
```
// Read and print out sensor data from ALS Data Register Addresses of i2c address
LSB = I2C_8_read_register(0x26, 0x10);    // Read DATA3L register from sensor address
MSB = I2C_8_read_register(0x26, 0x11);    // Read DATA3H register from sensor address
ALS_count = (MSB << 8) | LSB;             // Shifting together LSB & MSB for ALS channel counts
Print(ALS_count);                         // Print out ALS count
```

Interrupts

The interrupt feature of Digital Light Sensor (DLS) IC simplifies and improves system efficiency by eliminating the need to poll the sensor for data. The DLS IC implements four interrupt threshold registers that allow the user to define thresholds above and below a desired light level. The user can also select which data is used (from which readout channel; IEN register) for interrupt generation and if interrupt is generated when all enabled channels produce an interrupt (And) or if a single channel produces an interrupt (Or); IOA bit. To further control when an interrupt occurs, the DLS IC provides an interrupt persistence feature. This feature allows the user to specify the number of conversion cycles for which an event exceeding the interrupt threshold must persist, before generating an interrupt.

Both IENL and IENH must be set to HIGH to activate interrupt functionality of a single channel. The interrupt is activated when the selected measurement data is higher than the high threshold value (determined by registers IHTH and IHTL) or lower than the low threshold value (determined by registers ILTH and ILTL) for a consecutive number of measurements (determined by the IPERS[3:0] bits). The counter keeping track of the number of consecutive detections is reset when the measurement data is between the high threshold value and the low threshold value. Once the interrupt is activated it can only be reset through the I^2C interface by reading the IFLAG or DATA1L register (defined by ICC bit). When the interrupt is activated the interrupt pin (INT) is pulled low (open-drain output).

Interrupt Timing Diagram



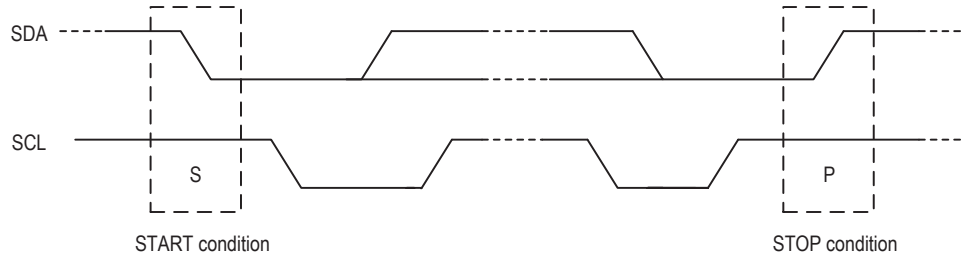
I2C Protocol

Interface and control of the Digital Light Sensor (DLS) IC is accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. Device address can be set to one of the two values found I table below. The IC address depends on the voltage sensed on the ADDR pin.

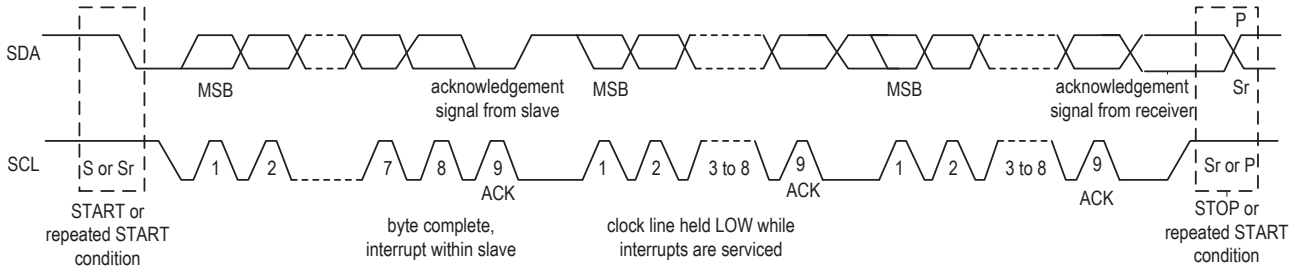
ADDR	I²C Address (dec)	I²C Address (hex)
GND	7'd38	0x26
VDD	7'd39	0x27

The I²C standard provides for three types of bus transaction: read, write and a combined protocol. During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. For a complete description of I²C protocols, please review the I²C Specification at: http://www.NXP.com.

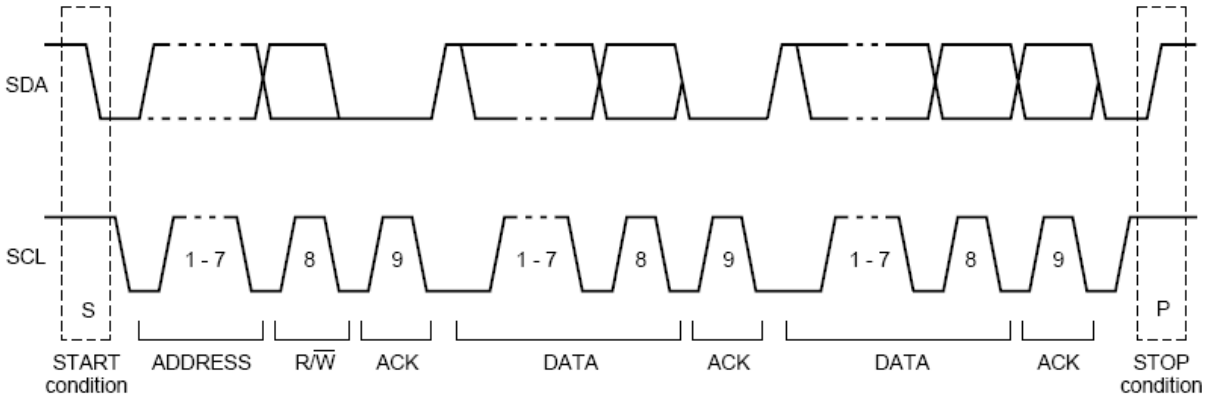
Start and Stop Conditions



Data Transfer on I2C Bus



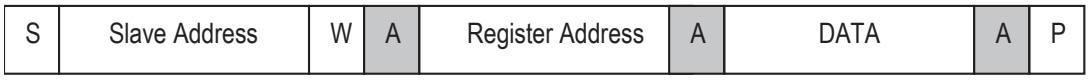
A Complete Data Transfer



A	Acknowledge (0)
N	Not Acknowledged (1)
P	Stop Condition
R	Read (1)
S	Start Condition
Sr	Repeated Start Condition
W	Write (0)
…	Continuation of protocol
	Master-to-Slave
	Slave-to-Master

I2C Write Protocol

For the continuous Write operation, the pointer register gets auto incremented. The slave acknowledges every bite.

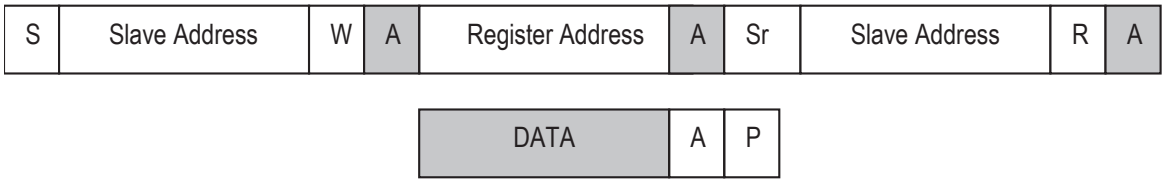


I2C Read Protocol

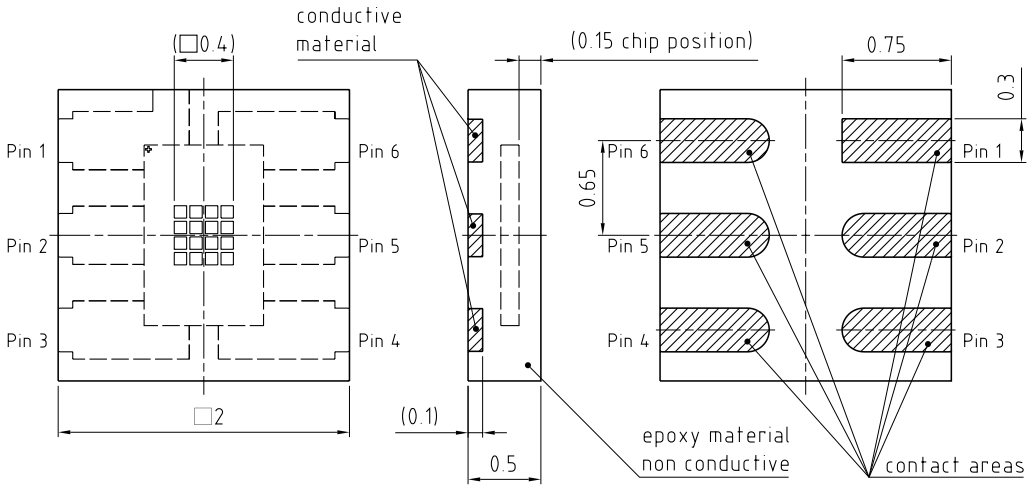
For the continuous Read operation, the pointer register gets auto incremented. The continuous Read stops when the Master does not acknowledge a byte.



I2C Read Protocol – Combined Format



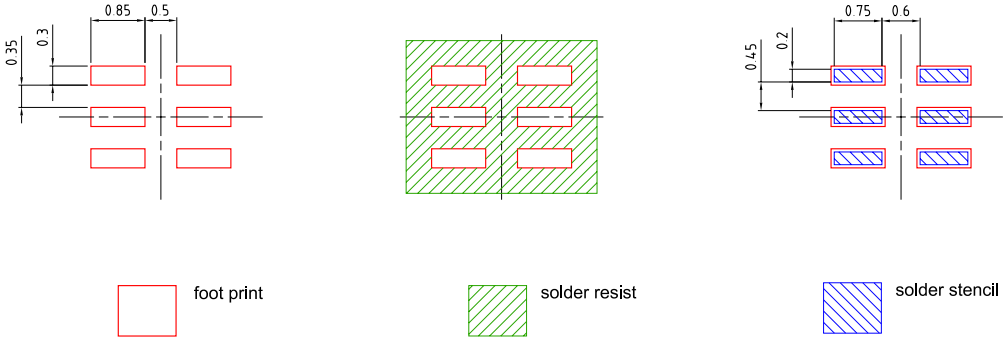
Dimensional Drawing [1)]

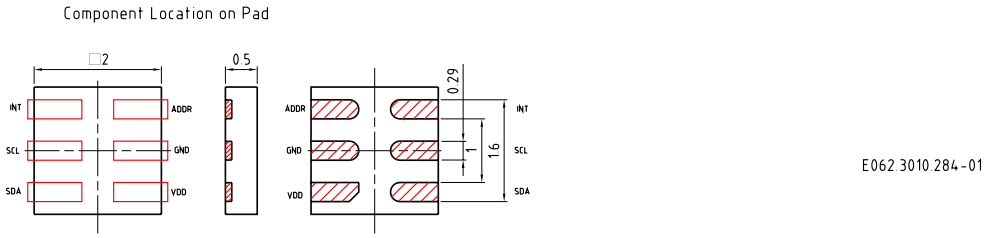


Further Information:

Approximate Weight: 4.0 mg

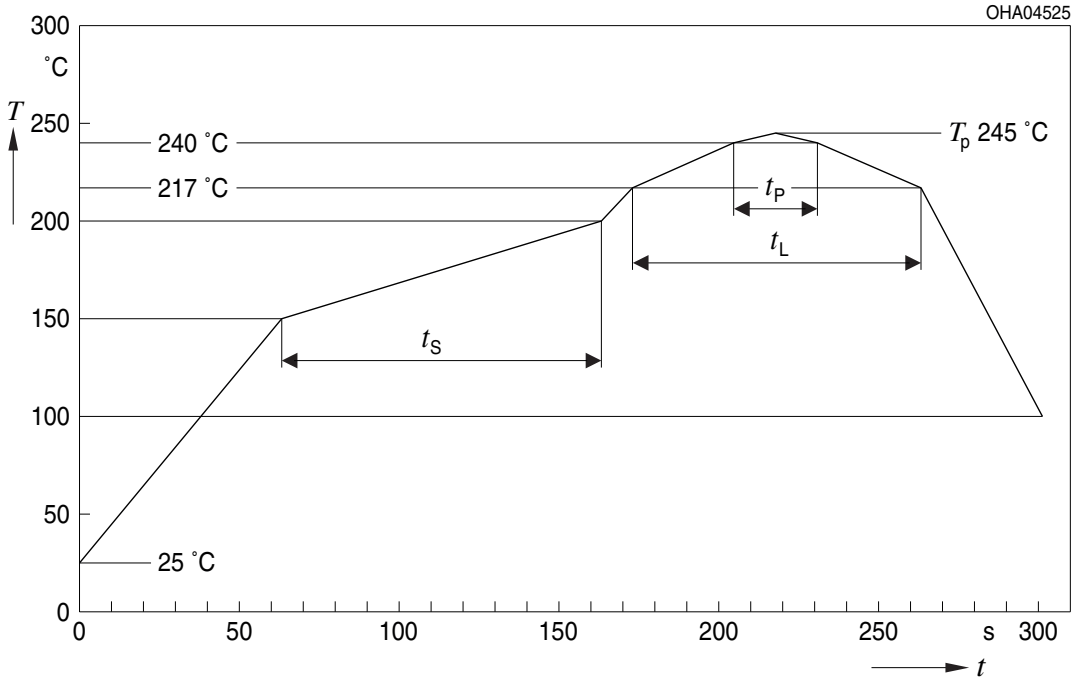
Recommended Solder Pad [1)]





Reflow Soldering Profile

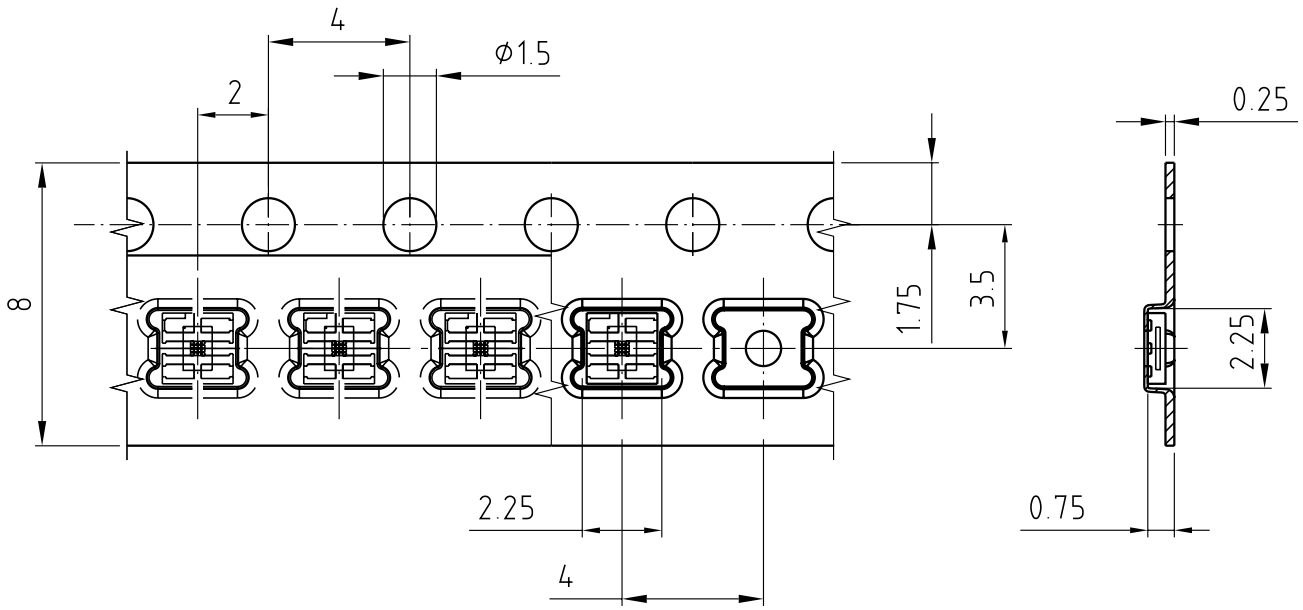
Product complies to MSL Level 3 acc. to JEDEC J-STD-020E



Profile Feature	Symbol	Pb-Free (SnAgCu) Assembly			Unit
		Minimum	Recommendation	Maximum	
Ramp-up rate to preheat*) 25 °C to 150 °C			2	3	K/s
Time t_S T_{Smin} to T_{Smax}	t_S	60	100	120	s
Ramp-up rate to peak*) T_{Smax} to T_P			2	3	K/s
Liquidus temperature	T_L		217		°C
Time above liquidus temperature	t_L		80	100	s
Peak temperature	T_P		245	260	°C
Time within 5 °C of the specified peak temperature T_P - 5 K	t_P	10	20	30	s
Ramp-down rate* T_P to 100 °C			3	6	K/s
Time 25 °C to T_P				480	s

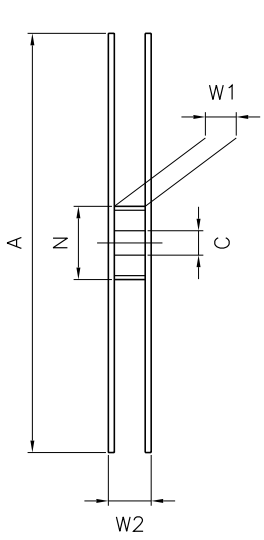
All temperatures refer to the center of the package, measured on the top of the component
* slope calculation DT/Dt: Dt max. 5 s; fulfillment for the whole T-range

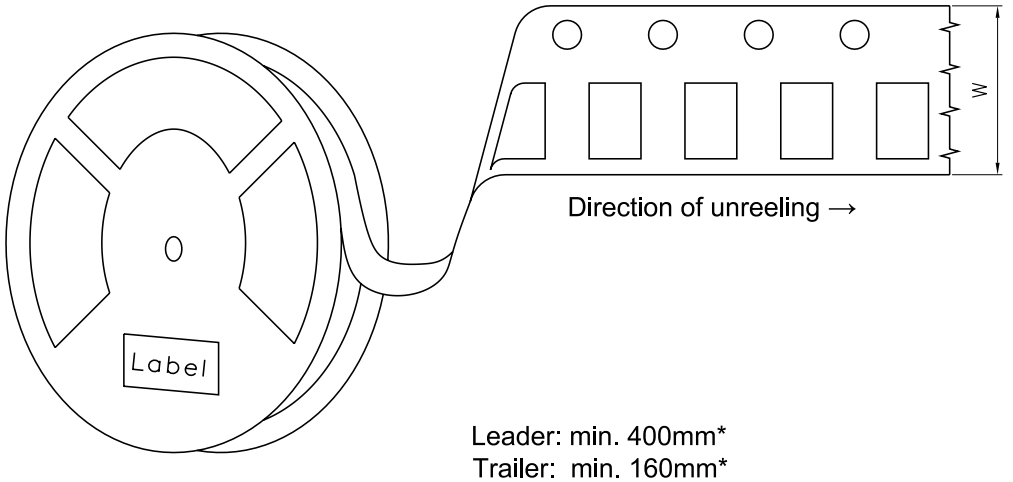
Taping [1)]



C63062-A4402-B1-03

Tape and Reel [2)]



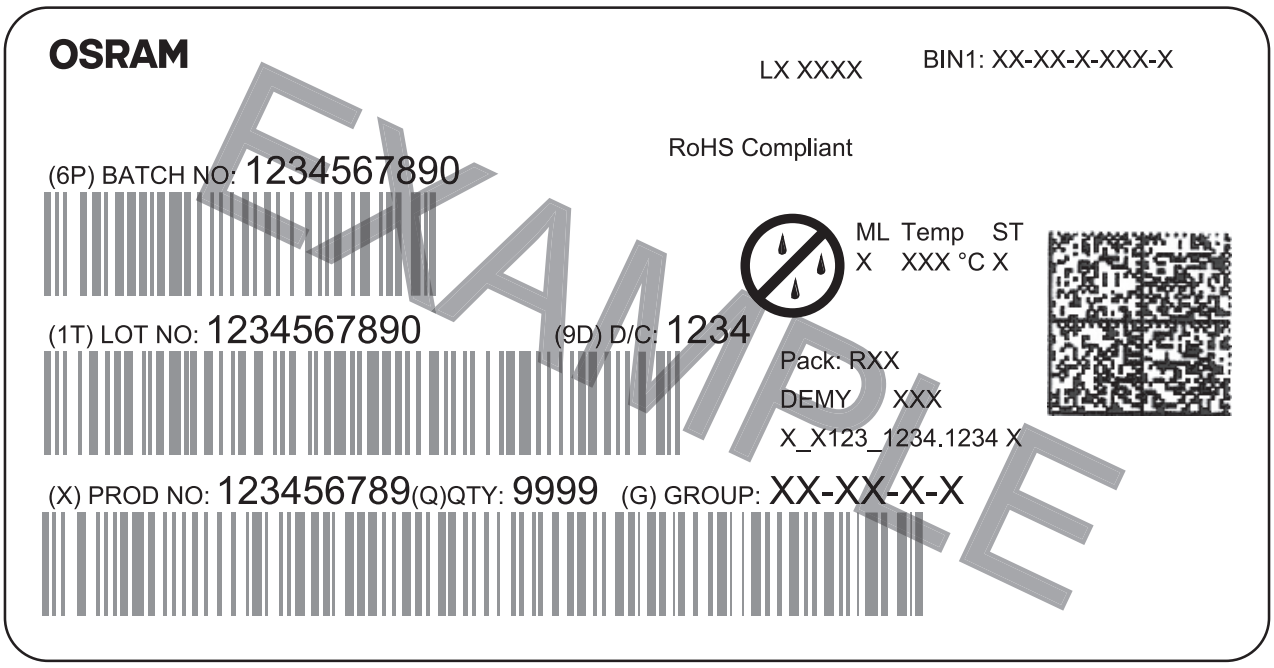


Leader: min. 400mm*
Trailer: min. 160mm*
*)Dimensions acc. to IEC 60286-3; EIA 481-E

Reel Dimensions

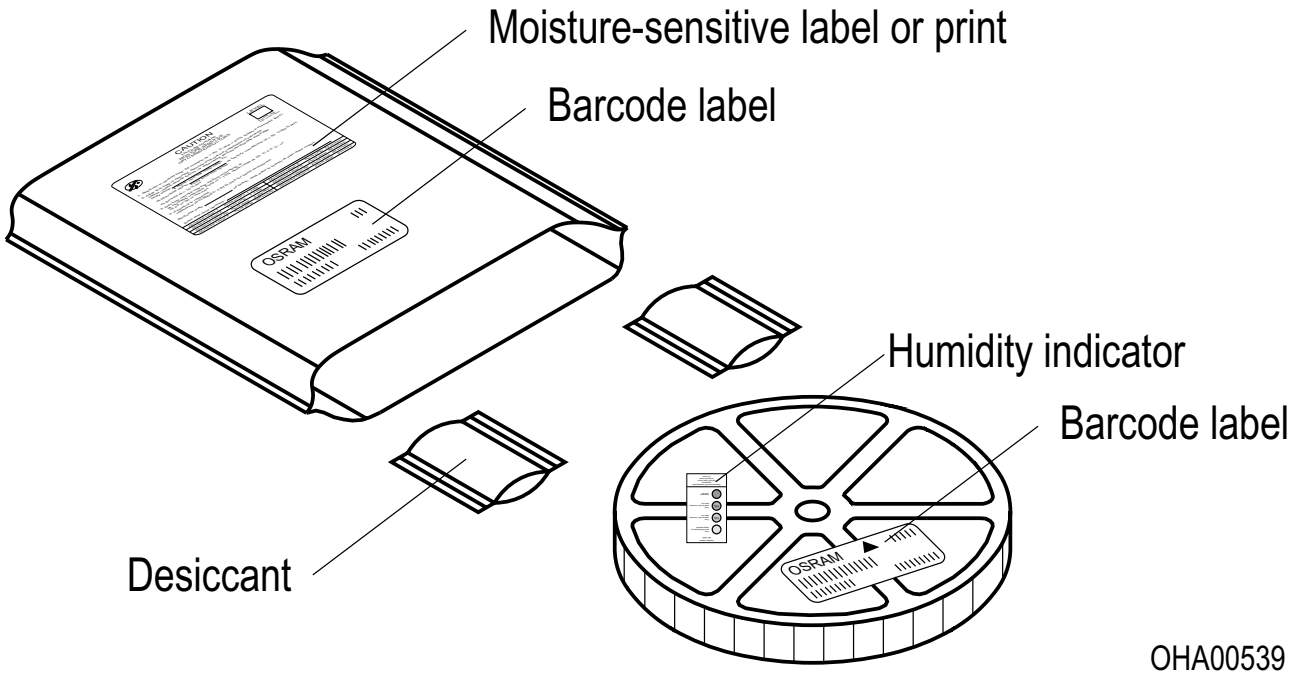
A	W	N_{min}	W_1	$W_{2\,max}$	Pieces per PU
180 mm	8 + 0.3 / - 0.1 mm	60 mm	8.4 + 2 mm	14.4 mm	4000

Barcode-Product-Label (BPL)



OHA04563

Dry Packing Process and Materials



OHA00539

Moisture-sensitive product is packed in a dry bag containing desiccant and a humidity card according JEDEC-STD-033.

Disclaimer

Attention please!

The information describes the type of component and shall not be considered as assured characteristics.
Terms of delivery and rights to change design reserved. Due to technical requirements components may contain dangerous substances.
For information on the types in question please contact our Sales Organization.
If printed or downloaded, please find the latest version on our website.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport. For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Product and functional safety devices/applications or medical devices/applications

Our components are not developed, constructed or tested for the application as safety relevant component or for the application in medical devices.
Our products are not qualified at module and system level for such application.

In case buyer – or customer supplied by buyer – considers using our components in product safety devices/ applications or medical devices/applications, buyer and/or customer has to inform our local sales partner immediately and we and buyer and /or customer will analyze and coordinate the customer-specific request between us and buyer and/or customer.

Glossary

1) **Tolerance of Measure:** Unless otherwise noted in drawing, tolerances are specified with ±0.1 and dimensions are specified in mm.

2) **Tape and Reel:** All dimensions and tolerances are specified acc. IEC 60286-3 and specified in mm.

Revision History

Version	Date	Change
1.0	2021-11-11	Initial Version
1.1	2022-02-28	New Layout Description
1.2	2026-10-13	Characteristics

EU RoHS and China RoHS compliant product
此产品符合欧盟 RoHS 指令的要求；
按照中国的相关法规和标准，
不含有毒有害物质或元素。

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