AS6223

Datasheet

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Table of contents

AS6223 Digital temperature sensor

1 General description

The AS6223 IC is a high accuracy digital temperature sensor system that communicates via a 2-wire digital bus with other devices. It consists of a Si bandgap temperature sensor, an ADC and a digital signal processor.

This sensor is especially designed to be used in applications where a small form factor with good performance is required, for example in mobile devices measuring the PCB and electronics temperature.

The very small form factor and ultra-low power consumption (low operation and quiescent current) makes the AS6223 ideally suited for mobile/battery powered applications.

The AS6223 is an easy to integrate and use solution, featuring a factory-calibrated sensor, integrated linearization and the possibility to use 4 different I²C addresses, enabling to use up to four AS6223 devices on one bus.

The AS6223 production test setup is calibrated according to NIST and the verification equipment is calibrated by an ISO/IEC-17025 accredited laboratory.

The AS6223 fulfills NIST traceability.

1.1 Key benefits & features

The benefits and features of AS6223, Digital temperature sensor are listed below:

Table 1: Added value of using AS6223

Benefits	Features
High measurement accuracy	± 0.09 °C (20 °C to 42 °C)
Low power consumption	6 µA @ Operation (typical, @ 4 Hz) 0.25 µA @ Sleep (typical)
Supply voltage range	1.14 V – 1.98 V (0 °C to 60 °C)
Small PCB footprint	0.82 mm x 0.82 mm (WLCSP)

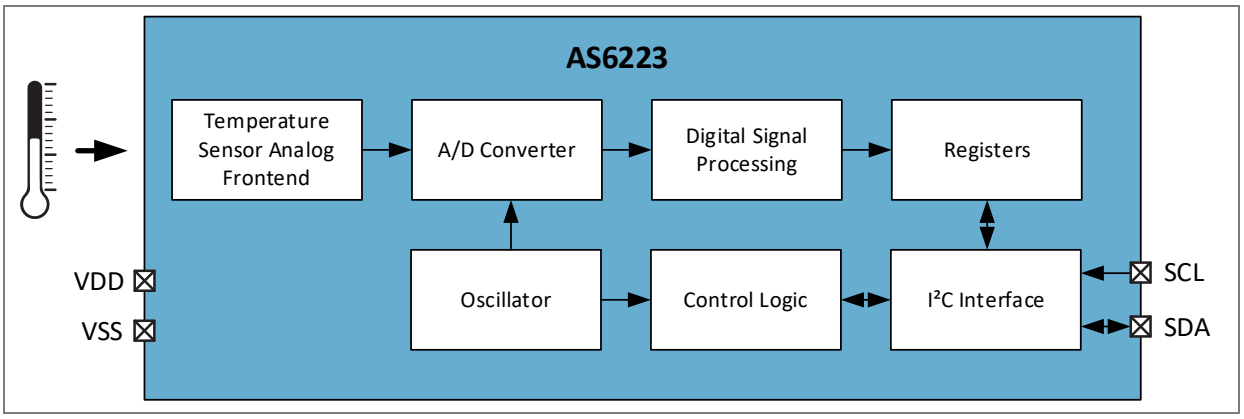
1.2 Applications

- Smartphones and Tablets (mobile devices)
- Wearables
- Cameras
- Electronic devices and PCB/component temperature control
- Cold chain monitoring
- Industrial automation
- Diabetes care products

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS6223



In Figure 1 the functional blocks are depicted. The sensing element for sensing the temperature is a Si bipolar transistor. The analog signal of the sensing element is converted into a digital signal by the A/D converter and the signal is further processed by a digital signal processor and written into the registers. The registers can be accessed via the serial bus interface (I²C bus).

2 Ordering information

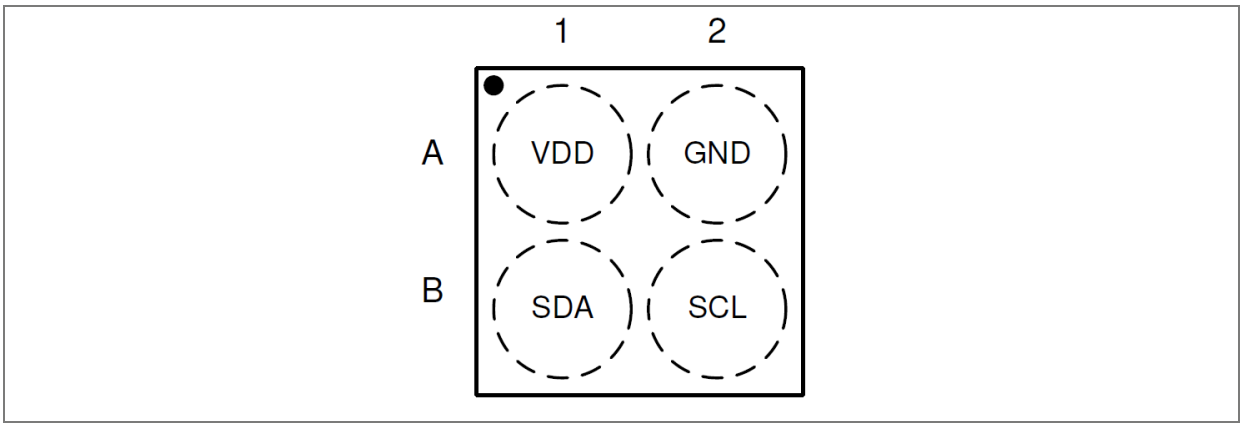
Product type	Ordering code	Package	Delivery form	Delivery quantity
AS6223A-AWLT	Q65113A8918	WLCSP	Tape & reel	12,000 pcs/reel
AS6223A-AWLM	Q65115A0751	WLCSP	Tape & reel	500 pcs/reel
AS6223B-AWLT	Q65115A0831	WLCSP	Tape & reel	12,000 pcs/reel
AS6223B-AWLM	Q65115A0832	WLCSP	Tape & reel	500 pcs/reel
AS6223C-AWLT	Q65115A0776	WLCSP	Tape & reel	12,000 pcs/reel
AS6223C-AWLM	Q65115A0778	WLCSP	Tape & reel	500 pcs/reel
AS6223D-AWLT	Q65115A0779	WLCSP	Tape & reel	12,000 pcs/reel
AS6223D-AWLM	Q65115A0780	WLCSP	Tape & reel	500 pcs/reel
AS6223E-AWLT	Q65115A0808	WLCSP	Tape & reel	12,000 pcs/reel
AS6223E-AWLM	Q65115A0809	WLCSP	Tape & reel	500 pcs/reel
AS6223F-AWLT	Q65115A0827	WLCSP	Tape & reel	12,000 pcs/reel
AS6223F-AWLM	Q65115A0828	WLCSP	Tape & reel	500 pcs/reel
AS6223G-AWLT	Q65115A0881	WLCSP	Tape & reel	12,000 pcs/reel
AS6223G-AWLM	Q65115A0891	WLCSP	Tape & reel	500 pcs/reel
AS6223H-AWLT	Q65115A0892	WLCSP	Tape & reel	12,000 pcs/reel
AS6223H-AWLM	Q65115A0893	WLCSP	Tape & reel	500 pcs/reel
AS6223I-AWLT	Q65115A0894	WLCSP	Tape & reel	12,000 pcs/reel
AS6223I-AWLM	Q65115A0895	WLCSP	Tape & reel	500 pcs/reel
AS6223J-AWLT	Q65115A0903	WLCSP	Tape & reel	12,000 pcs/reel
AS6223J-AWLM	Q65115A0998	WLCSP	Tape & reel	500 pcs/reel
AS6223K-AWLT	Q65115A0904	WLCSP	Tape & reel	12,000 pcs/reel
AS6223K-AWLM	Q65115A0905	WLCSP	Tape & reel	500 pcs/reel
AS6223L-AWLT	Q65115A0906	WLCSP	Tape & reel	12,000 pcs/reel
AS6223L-AWLM	Q65115A0907	WLCSP	Tape & reel	500 pcs/reel

3 Pin assignment

3.1 Pin diagram

In Figure 2 the pin assignment of the WLCSP package is shown. The viewing side is from the top. The A1 pin is also marked with a point on the top side.

Figure 2: Pin diagram of AS6223 (WLCSP)



3.2 Pin description

In Table 2 the pins of AS6223 are described. External pull up resistors (to VDD) are necessary for the pins “SDA” and “SCL”.

Table 2: Pin description of AS6223 (WLCSP)

Pin number	Pin name	Pin type(1)	Description
A1	VDD	S	Positive supply voltage
A2	VSS	S	Ground pin
B1	SDA	DIO_SOD	Serial interface data
B2	SCL	DI_S	Serial interface clock

(1) Explanation of abbreviations:

S	Supply
DI_S	Digital Schmitt Trigger Input
DIO_SOD	Digital Schmitt Trigger Input / Open Drain Output

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS6223

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameter					
V_{DD} / V_{SS}	Supply voltage to VSS	-0.3	2.1	V	Reference to VSS
VDIO	IO pin voltage	-0.3	2.1	V	Reference to VSS
I_SCR	Input current (latch up immunity)	-100	100	mA	According to JESD78D
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM		±2000	V	MIL_STD_833J-3015.9
Temperature ranges and storage conditions					
T_A	Operating ambient temperature	-40	125	°C	
T_J	Operating junction temperature	-40	125	°C	
T_{STRG}	Storage temperature range	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020(1)
R_{HNC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level		1		Unlimited floor life time

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).

5 Operating conditions

The AS6223 is a complete sensor system that has an integrated sensing element, the analog frontend, the A/D converter and the digital signal processing part.

The digital signal processing part consists of the signal processor, the registers and the serial bus interface.

5.1 Analog system parameters

In Table 4 an overview of the analog system parameters is given.

The current consumption for less than 4 conversions per second is lower than the values given in Table 4.

Table 4: Analog system parameters of AS6223

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD	1.14	1.2	1.98	V	T= 0 °C to 60 °C
		1.62	1.8	1.98	V	T= -40°C to 125°C
Temperature range	T	-40		125	°C	
Standby current consumption	$IDD_{standby}$		0.25	1.0	µA	T= 0 °C to 45 °C
				1.5	µA	T= 45 °C to 60 °C
Current consumption (4 conversions /s)	IDD		6	8	µA	T= 0 °C to 45 °C Serial bus inactive
				9.5	µA	T= 45 °C to 60 °C Serial bus inactive
Resolution	N		16		Bits	
Conversion time	TS	11	16	21	ms	OSR[2:0]=010
		22	32	42	ms	OSR[2:0]=011
		44	64	84	ms	OSR[2:0]=100
Conversion rate	NS		0.25 1 4 8	0.35 1.35 5.5 10.7	Conv/s	CR[1:0]=00 CR[1:0]=01 CR[1:0]=10 CR[1:0]=11
Supply voltage rise time	TRise_VDD			20	ms	From 0.1 V to 0.8 * VDD
Supply voltage slew rate	SR_VDD	200			mV/ms	From 0.1 V to 0.8 * VDD

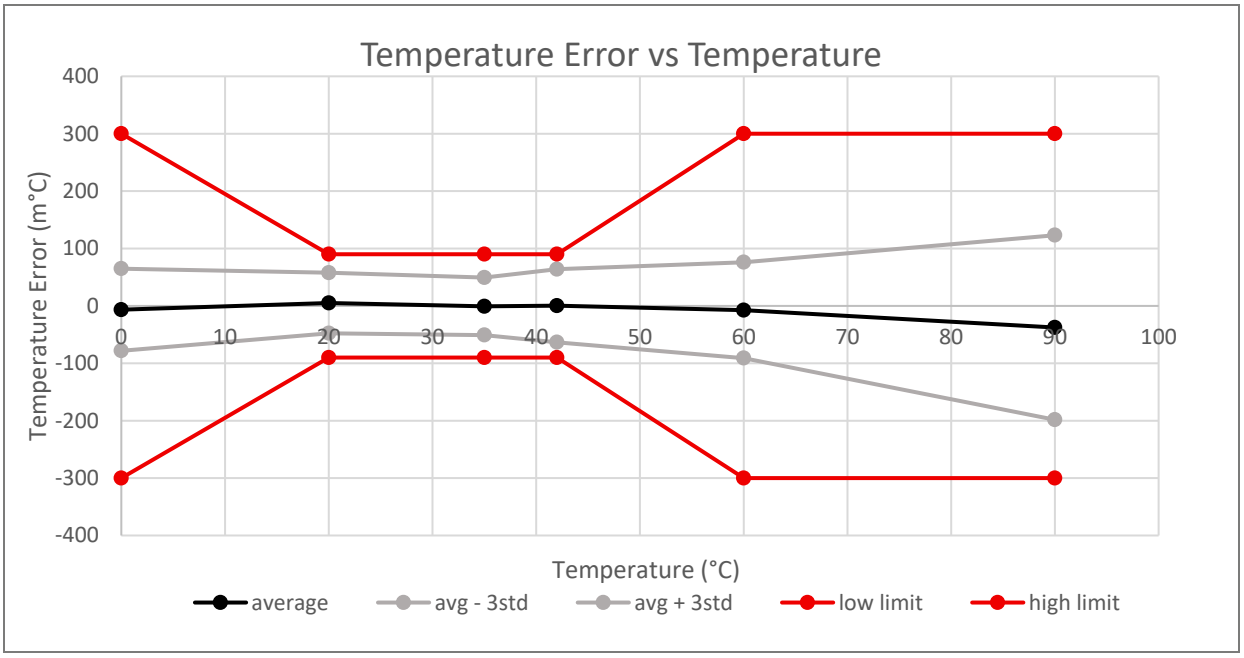
In Table 5 the different accuracy values of AS6223 are shown. These values are representative for a 3σ distribution. All accuracy values are valid for the complete supply voltage range given in Table 4.

Table 5: Temperature accuracy values of AS6223

Parameter	Symbol	Min	Typ	Max	Unit	Note
Temperature error	T_ERR	-0.3		0.3	°C	T= -40 °C to -20 °C
		-0.2		0.2		T= -20 °C to 0 °C
		-0.15		0.15		T= 0 °C to 20 °C
		-0.09*	0.03	0.09*		T= 20 °C to 42 °C
		-0.15		0.15		T= 42 °C to 60 °C
		-0.2		0.2		T= 60 °C to 85 °C
		-0.3		0.3		T= 85 °C to 125 °C
Temperature noise	T_NOISE		0.06	0.075	°C	OSR[2:0]=011
			0.044	0.054	°C	OSR[2:0]=100
Long-term drift	T_DRIFT		0.048		°C	1000hrs at 125°C

(1) *Considering sampling rate setting [011]

Figure 3: AS6223 measurement accuracy over temperature



5.2 Digital system parameters

In Table 6 an overview of the digital system parameters is given.

Table 6: Digital system parameters of AS6223

Parameter	Symbol	Pins	Min	Max	Unit	Note
High level input voltage	V_IH	SCL	0.8 * VBUS		V	
Low level input voltage	V_IL	SCL		0.3 * VBUS	V	
Hysteresis voltage	V_HYST	SCL, SDA	200	1200	mV	
Input leakage current	I_LEAK	SCL	-1	1	µA	V_IL=0.0 V
High level input voltage	V_IH	SDA	0.8 * VBUS		V	
Low level input voltage	V_IL	SDA		0.3 * VBUS	V	
Low level output voltage	V_OL	SDA		VSS+0.4	V	
Tristate leakage current	I_OZ	SDA	-10	10	µA	To VSS

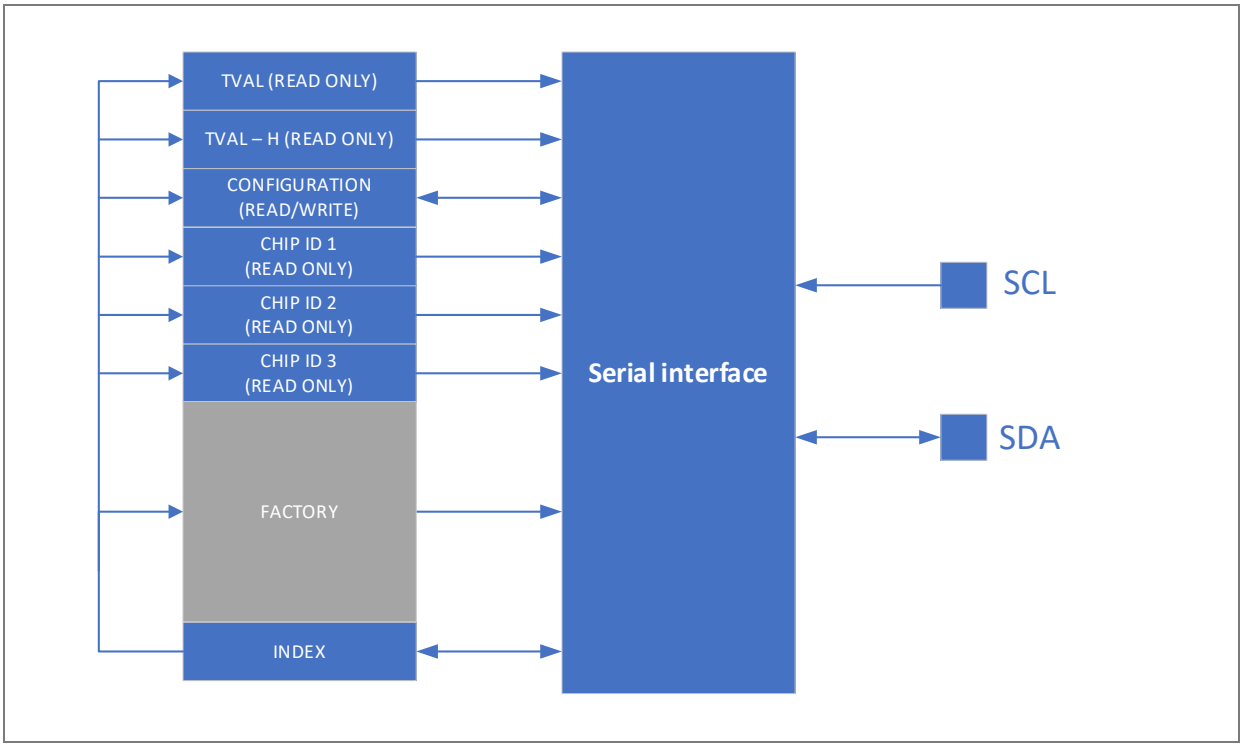
6 Register description

6.1 Register overview

In Figure 4 the registers that the device contains are shown.

With the use of the index register, it is possible to address the specific register. The index register is an 8-bit register, where only bits 0 and 1 are used as shown in Table 7 and all other bits are set to 0 and read only.

Figure 4: Register map with serial interface



6.1.1 Index register

Table 7: Index register

Bit	Bit name	Default	Access
0	Address bit	0	RW
1	Address bit	0	RW
2	Reserved	0	RO
3	Reserved	0	RO
4	Reserved	0	RO
5	Reserved	0	RO
6	Reserved	0	RO
7	Reserved	0	RO

The first 2-bit addresses in the index register define the access to the registers shown in Table 8. This means that to access the different registers, the index register must be set accordingly. Except for the TVAL & CHIP ID registers (which contain the temperature value data as well as the unique chip identifier), all registers are read/write accessible.

Table 8: Register map

Address	Symbol	Register	Description
0x0	TVAL	Temperature register	Contains the temperature value
0x1	TVAL - H	TEMP_ACCU_MSB + Temp_ready	Temperature register MSB values plus TEMP ready bit
0x2	CONFIG	Configuration register	Configuration settings of the temperature sensor
0x3	CHIP ID 1	Chip ID register	First 16 bits of CHIP ID
0x4	CHIP ID 2	Chip ID register	Second 16 bits of CHIP ID
0x5	CHIP ID 3	Chip ID register	Third 16 bits of CHIP ID

6.2 Detailed register description

6.2.1 TVAL register (Address 0x00)

Table 9: TVAL register (Address 0x00)

Addr: 0x00

Bit	Bit name	Default	Access	Bit description
0	T 00	0	RO	Temperature value Bit [00]
1	T 01	0	RO	Temperature value Bit [01]
2	T 02	0	RO	Temperature value Bit [02]
3	T 03	0	RO	Temperature value Bit [03]
4	T 04	0	RO	Temperature value Bit [04]
5	T 05	0	RO	Temperature value Bit [05]
6	T 06	0	RO	Temperature value Bit [06]
7	T 07	0	RO	Temperature value Bit [07]
8	T 08	0	RO	Temperature value Bit [08]
9	T 09	0	RO	Temperature value Bit [09]
10	T 10	0	RO	Temperature value Bit [10]
11	T 11	0	RO	Temperature value Bit [11]
12	T 12	0	RO	Temperature value Bit [12]
13	T 13	0	RO	Temperature value Bit [13]
14	T 14	0	RO	Temperature value Bit [14]
15	T 15	0	RO	Temperature value Bit [15]

6.2.2 TVAL – high register (Address 0x01)

Table 10: TVAL – high register (Address 0x01)

Addr: 0x01

Bit	Bit name	Default	Access	Bit description
0	T 16	0	RO	Temperature value Bit [16]
1	T 17	0	RO	Temperature value Bit [17]
2	T 18	0	RO	Temperature value Bit [18]
3	TR	0	RO	New temperature ready
4 - 15	Reserved	0	RO	Reserved

(1) The bits T16 - T18 will only be enabled when AVG bit has been set to 1.

6.2.3 Configuration register (Address 0x02)

The configuration register is a 16-bit register which defines the operation modes of the device. Any read/write operation processes the MSB byte first.

In Table 11 the configuration register is shown. The bits 6-15 are not to be used and are set to read only. The explanation of the other bits are detailed in the following sections.

Table 11: Configuration register (Address 0x02)

Addr: 0x02

Bit	Bit name	Default	Access	Bit description
0	CR [0]	0	RW	Conversion RATE (CR)
1	CR [1]	1	RW	Conversion RATE (CR)
2	OSR[0]	1	RW	Oversampling ratio (OSR-0)
3	OSR[1]	1	RW	Oversampling ratio (OSR-1)
4	OSR[2]	0	RW	Oversampling ratio (OSR-2)
5	Reserved	0	RW	Reserved – please keep this ‘0’
6	AVG	0	RW	Averaging enable (8 conv.)
7	SM	0	RW	Sleep mode (SM)
8	SS	0	RW	Single shot
9	SR	0	RW	Soft reset
10	Reserved	0	RO	Reserved
11	Reserved	0	RO	Reserved
12	Reserved	0	RO	Reserved
13	Reserved	0	RO	Reserved
14	Reserved	0	RO	Reserved
15	Reserved	0	RO	Reserved

6.2.4 Conversion rate bits

The conversion rate bits define the number of executed temperature conversions per time unit. Additional readouts of the temperature register between conversions are possible but not recommended because the value is changed only after a conversion is finished.

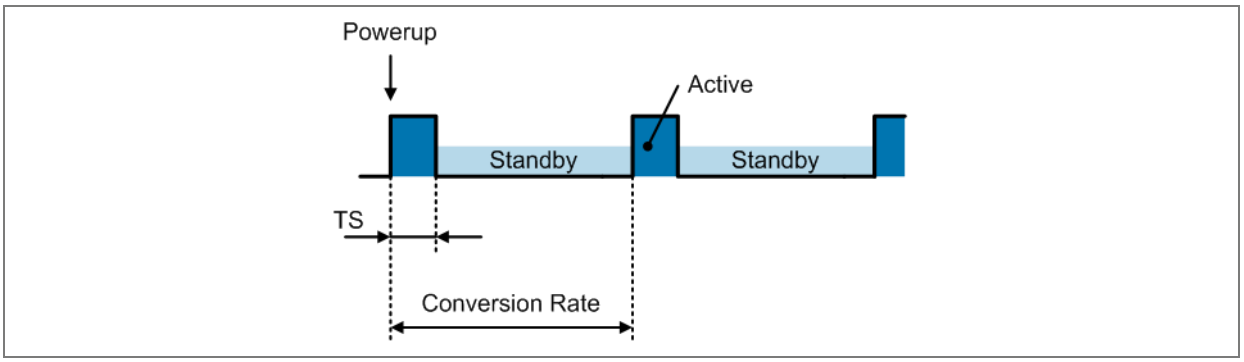
Values of 125 ms, 250 ms, 1 s and 4 s for a conversion can be configured while the default rate is set to 4 conversions per second.

Table 12: Conversion rate configuration

Conversion rate bits		Conversion rate
Bit 1	Bit 0	Conv/s
0	0	0.25
0	1	1
1	0	4
1	1	8

The device immediately starts a conversion after a power-on sequence and provides the first result after typ. 36 ms. A higher power consumption occurs during the actual conversion while the device stays in the standby mode after a finished conversion until the next conversion is activated. This is shown in the following Figure 5.

Figure 5: Conversion sequence



6.2.5 Sampling rate

The OSR bits are used to set the conversion speed and noise level. Per default oversampling ratio (OSR) is 0x03 which means conversion rate is at 32ms (typ.). By reducing conversion rate the noise performance will be improved. Writing values greater than 0x04 in the OSR register are invalid.

Table 13: Oversampling ratio bits

Oversampling ratio bits			Conversion rate
OSR[2]	OSR[1]	OSR[0]	
0	1	0	16 ms
0	1	1	32 ms (default)
1	0	0	64 ms
1	0	1	Invalid case
1	1	0	Invalid case
1	1	1	Invalid case

6.2.6 Sleep mode

The sleep mode is activated by setting the bit SM in the configuration register to 1. This shuts the device down immediately and reduces the power consumption to a minimum value.

The serial interface is the only active circuitry in the sleep mode in order to provide access to the digital registers.

Entering the sleep mode will take some time (250µs maximum).

After resetting the SM bit to 0, the device enters the continuous conversion mode.

By default, the sleep mode bit is set to 0, hence the device is in continuous mode.

Table 14: Sleep mode configuration

Sleep mode bit	Operation mode
0	Continuous conversion mode
1	Sleep mode

6.2.7 Soft reset

By setting SR Bit to 1 a full chip reset is triggered when STOP condition is sent on I²C bus.

By default, this bit is set to 0.

Table 15: Soft reset configuration

Soft RESET bit	Operation mode
0	Default function
1	Chip reset triggered after I²C STOP

6.2.8 Averaging

By setting AVG bit an averaging can be applied to the available temperature information. When AVG bit is set the device performs an accumulation based on 8 conversions. The accumulated values are stored in register 0x01 bit T16 – T18. This is used to improve noise performance. Averaging function is no running average and can be used on continuous conversion and single shot mode.

Table 16: Consecutive faults bit settings

Averaging bit	Accumulations
0	No averaging
1	8 samples accumulated

6.2.9 Single shot conversion

The device features a single shot measurement mode if the device is in sleep mode (SM=1). By setting the “Single Shot-bit” to 1, a single temperature conversion is started, and the SS-bit can be read as 1 during the active conversion operation. Once the conversion is completed, the device enters the sleep mode again and the SS-bit is set to 0. The single shot conversion allows very low power consumption since a temperature conversion is executed on demand only. This allows a user defined timing of the temperature conversions to be executed and is used if the consecutive operation mode is not required.

The first conversion triggered in this mode has a longer conversion time.

Sleep mode is detailed together with the recommendation to trigger the first conversion simultaneously with entering the sleep mode.

As the device exhibits a very short conversion time, the effective conversion rate can be increased by setting the single shot bit repetitively after a conversion has finished. However, it has to be ensured that the additional power is limited, otherwise self-heating effects have to be considered.

Table 17: Single shot conversion bit settings

Single shot bit	Conversion
0	No conversion ongoing
1	Start single shot conversion

Once single shot conversion is completed, TR bit (temperature ready) is set to 1. Reading CONF register will lead to clear the single shot bit SS to 0.

6.2.10 Temperature register and value calculation

Table 18: Temperature value register

Addr: 0x0

Bit	Bit name
0	T0
1	T1
2	T2
3	T3
4	T4
5	T5
6	T6
7	T7
8	T8
9	T9
10	T10
11	T11
12	T12
13	T13
14	T14
15	T15

The temperature register contains the digitally converted temperature value and can be read by setting the index pointer to the TVAL register (0x0).

Two consecutive bytes must be read to obtain the complete temperature value. The MSB byte (Bits 15 to 8) is transmitted upon the first read access and the LSB byte (Bits 7 to 0) is transmitted after the second read access.

A temperature value is represented as a two-complement value in order to cover also negative values. After power-up, the temperature value is read as 0 °C until the first conversion has been completed. One LSB corresponds to 0.0078125 °C (= 1/128 °C).

The binary values can be calculated according to the following formulas:

Positive values: |Value| / LSB

Negative values: Complement (|Value| / LSB) + 1

Example 50 °C:

$50°C/0.0078125°C = 6400 = Binary\ 0001\ 1001\ 0000\ 0000 = Hex\ 1900$

Table 19: Temperature conversion examples

Temperature (°C)	Digital output (Binary)	Digital output (Hex)
60.0	0001 1110 0000 0000	1E00
50.0	0001 1001 0000 0000	1900
25.0	0000 1100 1000 0000	0C80
0.125	0000 0000 0001 0000	0010
0.0078125	0000 0000 0000 0001	0001
0.0	0000 0000 0000 0000	0000

6.2.11 Chip ID register (Address 0x03 – 0x05)

The Chip ID register is a 48-bit register (split into 3 x 16-bit registers) which allows full traceability of every individual sensor to fulfill NIST traceability. In these registers read-only access is granted.

In Table 20 – Table 22 the CHIP ID register is shown. All bits are factory programmed and cannot be overwritten anymore. To calculate back CHIP ID values to relevant information please reach out to ams OSRAM technical support.

Table 20: CHIP ID register 1

Addr: 0x03

Bit	Bit name	Default	Access	Bit description
0:15	Chip ID 0-15	Factory programmed	RO	Chip ID bit 0-15

Table 21: CHIP ID register 2

Addr: 0x04

Bit	Bit name	Default	Access	Bit description
0-15	Chip ID 16:31	Factory programmed	RO	Chip ID bit 16 - 31

Table 22: CHIP ID register 3

Addr: 0x05

Bit	Bit name	Default	Access	Bit description
0-15	Chip ID 32-47	Factory programmed	RO	Chip ID bit 32-47

6.3 Serial interface

The device employs a standard I²C-serial bus.

6.3.1 Bus description

A data transfer must be invoked by a master device (e.g. microcontroller) which defines the access to the slave device. The master device defines and generates the serial clock (SCL) and the start/stop conditions.

In order to address a specific device, a START condition has to be generated by the master device by pulling the data line (SDA) from a logic high level to a logic low level while the serial clock signal (SCL) is kept at high level.

After the start condition, the slave address byte is transmitted which is completed with a ninth bit which indicates a read (bit = ‘1’) or a write operation (bit = ‘0’) respectively. All slaves read the data on the rising edge of the clock. An acknowledge signal is generated by the addressed slave during the ninth clock pulse. This acknowledge signal is produced by pulling the pin SDA to a low level by the selected slave.

Subsequently, the byte data transfer is started and finished by an acknowledge bit. A change in the data signal (SDA) while the clock signal (SCL) is high causes a START or STOP condition. Hence, it must be ensured such a condition is prevented during a data transfer phase.

After completing the data transfer, the master generates a STOP condition by pulling the data line (SDA) from low level to high level while the clock signal (SCL) is kept at high level.

6.3.2 Data interface

A bus connection is created by connecting the open drain input/output lines SDA and SCL to the two-wire bus. The inputs of SDA and SCL feature Schmitt-trigger inputs as well as low pass filters in order to suppress noise on the bus line. This improves the robustness against spikes on the two-wire interface.

Both fast transmission mode (1 kHz to 400 kHz).

Any data transfer transmits the MSB first and the LSB as last bit.

6.3.3 Bus address

A slave address consists of seven bits, followed by a data direction bit (read/write operation). The slave address can be selected from 8 different address variants of AS6223. This will be shown in Table 23.

Table 23: I²C address select variant

AS6223 variant	Device address (bin)	Device address (hex)	Voltage variant (V)
AS6223A	101 0100	0x54	VDD = VBUS = 1.8V
AS6223B	101 0101	0x55	VDD = VBUS = 1.8V
AS6223C	101 0110	0x56	VDD = VBUS = 1.8V
AS6223D	101 0111	0x57	VDD = VBUS = 1.8V
AS6223E	101 0100	0x54	VDD = VBUS = 1.2V
AS6223F	101 0101	0x55	VDD = VBUS = 1.2V
AS6223G	101 0110	0x56	VDD = VBUS = 1.2V
AS6223H	101 0111	0x57	VDD = VBUS = 1.2V
AS6223I	101 1000	0x58	VDD = 1.8V; VBUS = 1.2V
AS6223J	101 1001	0x59	VDD = 1.8V; VBUS = 1.2V
AS6223K	101 1010	0x5A	VDD = 1.8V; VBUS = 1.2V
AS6223L	101 1011	0x5B	VDD = 1.8V; VBUS = 1.2V

(1) VDD needs to be equal or greater VBUS
VDD/VBUS = 1.8V variation ±10%
VDD/VBUS = 1.2V variation ±5%

6.3.4 Read/write operation

In order to access an internal data register, the index register must be written in advance. This register contains the actual register address and selects the appropriate register for an access. A typical transfer consists of the transmission of the slave address with a write operation indication, followed by the transmission of the register address and is finalized with the actual register content data transfer. This implies that every write operation to the temperature sensor device requires a value for the index register prior to the transmission of the actual register data.

The index register defines the register address for both the write and read operation. Consequently, if a read operation is executed, the register address is taken from the index register which was defined from the last write operation.

If a different register needs to be read, the index register has to be written in advance to define the new register address. This is accomplished by transmitting the slave address with a low R/W bit, followed by the new content of the index register. Subsequently, the master provokes a START condition on the bus and transmits the slave address with a high R/W bit in order to initiate a read operation.

Since the index register always keeps its last value, reads can be executed repetitively on the same register.

Similarly to the byte transfer where the MSB is transmitted first, the transfer of a 16-bit word is executed by a two-byte transfer whereas the MSB byte is always transmitted first.

6.3.5 Slave operation

The device employs a slave functionality only (slave transmitter and slave receiver) and cannot be operated as a bus master. Consequently, the device never actively drives the SCL line.

6.3.6 Slave receiver mode

Any transmission is invoked by the master device by transmitting the slave address with a low R/W bit. Subsequently, the slave device acknowledges the reception of the valid address by pulling the ninth bit to a low level. Following to acknowledge, the master transmits the content of the index register. This transfer is again acknowledged by the slave device. The next data byte(s) are written to the actual data register which is selected by the index register while each transfer is acknowledged upon a completed transfer by the slave device. A data transfer can be finished if the master transmits a START or a STOP condition on the bus.

6.3.7 Slave transmitter

The master transmits the slave address with a high R/W bit. In turn, the slave acknowledges a valid slave address. Subsequently, the slave transmits the MSB byte of the actual selected data register by the index register. After the MSB byte transmission, acknowledge is sent by the master. Afterwards, the LSB byte is transmitted by the slave which is also acknowledged by the master after the completed transmission. The data transfer can be terminated by the master by transmitting a Not-Acknowledge after the transmitted slave data or by invoking a START or a STOP condition on the bus.

6.3.8 General call

A general call is issued by the master by transmitting the general call address (000 0000) with a low R/W bit. When this command is issued on the bus, the device acknowledges this command. The device also acknowledges the second byte but ignores the data. Subsequent bytes sent by the master during the general call are not acknowledged.

6.3.9 Start byte

When the master transmits address 000 0000 and a high R/W bit (“START byte”) the device acknowledges the address. The device then send the MSB data byte and LSB data byte, where the data corresponds to the content of the register which was addressed. After reset this corresponds to the temperature register.

6.3.10 Timeout function

The serial interface of the slave device is reset if the clock signal SCL is kept low for typ. 30 ms. Such a condition results in the release of the data line by the slave in case it has been pulled to low level. The slave remains inactive after a timeout and waits for a new START command invoked by the bus master. In order to prevent a timeout, the bus transfer rate must be higher than 1 kHz. This function is only available when the sensor is not in sleep mode (SM = 1).

6.3.11 Bus conditions

The following conditions occur on the serial bus which is compatible to the I²C-bus.

Bus idle

The signals SDA and SCL are not actively driven and pulled to a high level by an external pull-up resistor.

Start data transfer

A transition of the SDA input from high to low level while the SCL signal is kept at high level results in a START condition. Such a START condition must precede any data transfer.

Stop data transfer

A transition of the SDA input from low to high level while the SCL signal is kept at high level results in a STOP condition. Any data transfer is finished by generating a STOP or START condition.

Data transfer

The master device defines the number of data bytes between a START and STOP condition and there is no limitation in the amount of data to be transmitted.

If it is desired to read only a single MSB byte without the LSB byte, a termination of the data transfer can be provoked by issuing a START or STOP condition on the bus.

Acknowledge

It is mandatory for each slave device to respond with acknowledge if the device is addressed by the master. Acknowledge is indicated by pulling down the data line (SDA) while the clock signal (SCL) is high in the acknowledge clock phase. In order to avoid an unwanted, START or STOP condition on the bus, setup and hold times must be met.

The master can signal an end of data transmission by transmitting a Not-Acknowledge on the last transmitted data byte by keeping the acknowledge bit at high level.

6.3.12 Timing characteristics

Figure 6: Serial interface timing diagram

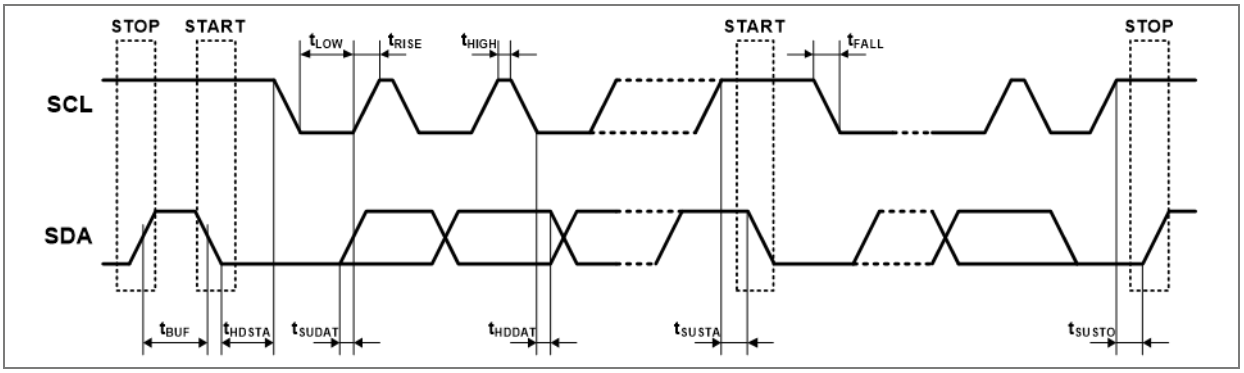


Table 24: Bus timing specifications

Parameter	Symbol	Fast mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0.001	0.4	MHz
Bus free time between STOP and START condition	t_{BUF}	600		ns
Hold time after repeated START condition	t_{HDSTA}	100		ns
Repeated START condition setup time	t_{SUSTA}	100		ns
Data in hold time	t_{HDDAT}	0		ns
Data out hold time(1)	t_{DH}	100		ns
Data setup time	t_{SUDAT}	100		ns
SCL clock low period	t_{LOW}	1300		ns
SCL clock high period	t_{HIGH}	600		ns
Clock/Data fall time	t_F		300	ns
Clock/Data rise time	t_R		300	ns
Clock/Data rise time for SCL ≤ 100 kHz	t_R		1000	ns

(1) The device will hold the SDA line high for 100 ns during the falling edge of the SCL.

6.3.13 Timing diagrams

The following timing diagrams depict the different bus operation modes and data transmission:

Figure 7: Timing diagram for word write

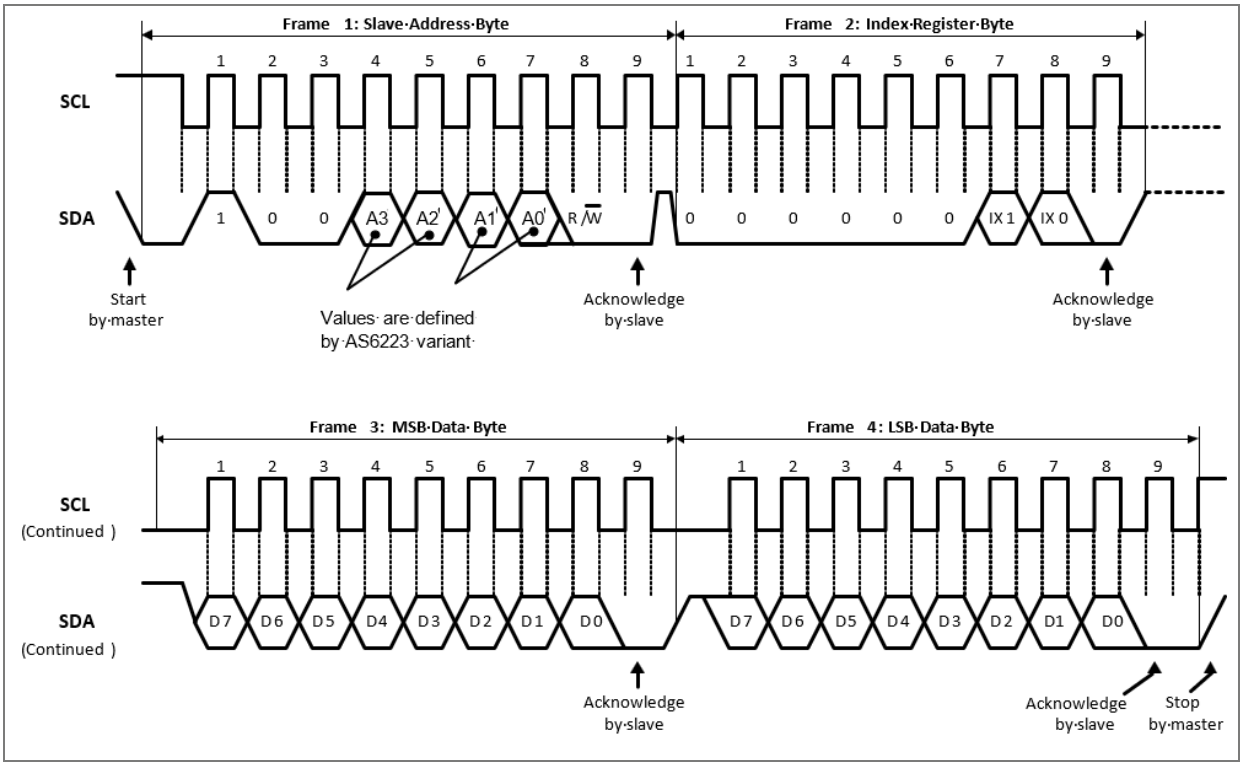
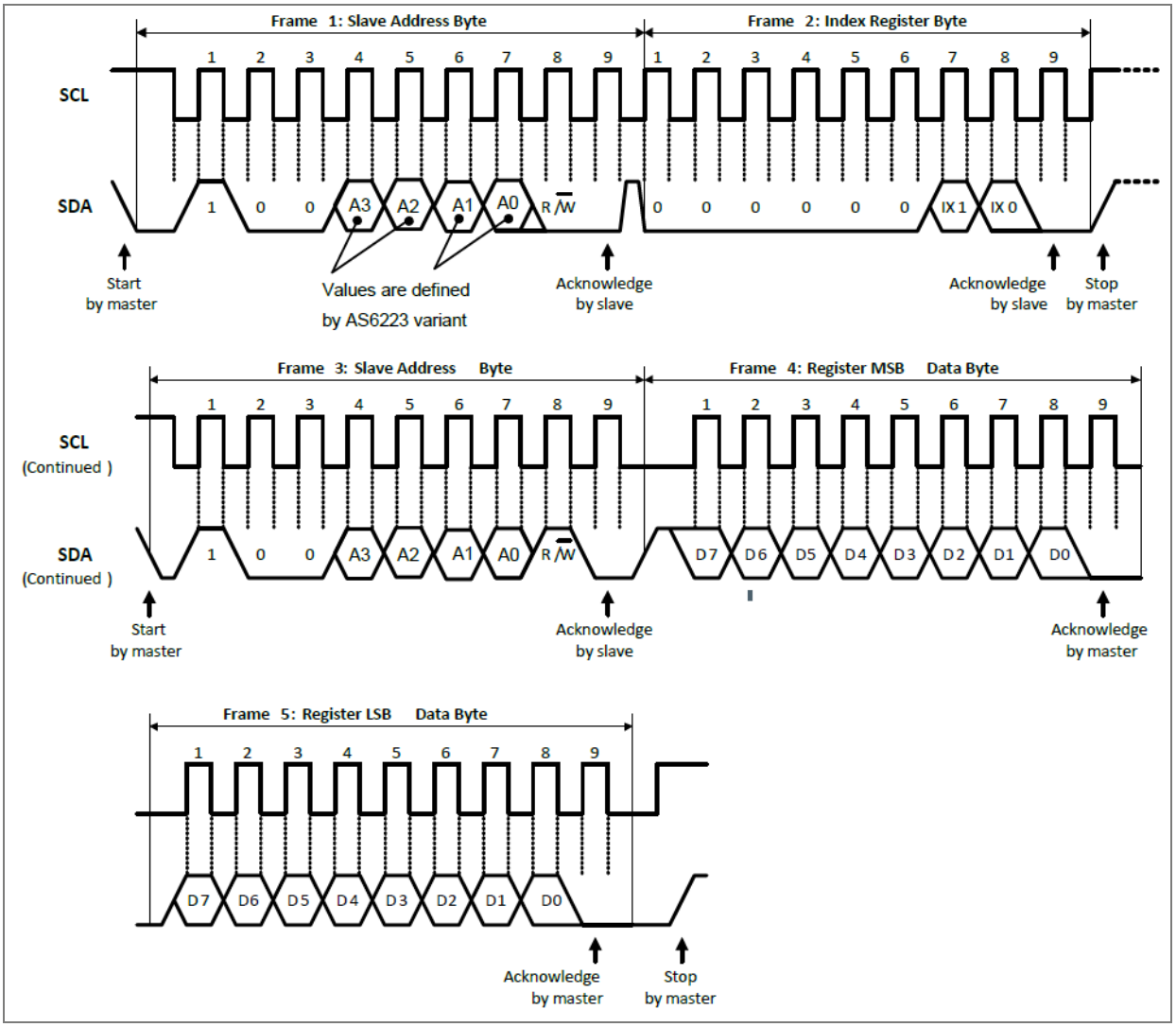


Figure 8: Timing diagram for word read



7 Application information

7.1 External components

In Figure 9 and Table 25 the schematics and the recommended values for external components are shown.

The decoupling capacitor for the supply should have a value of at least 10 nF.

For the serial interface, pull up resistors to VDD are mandatory.

The pull up resistors on the serial interface and the interrupt depend on the bus capacitance and on the clock speed.

Figure 9: Schematic with external components

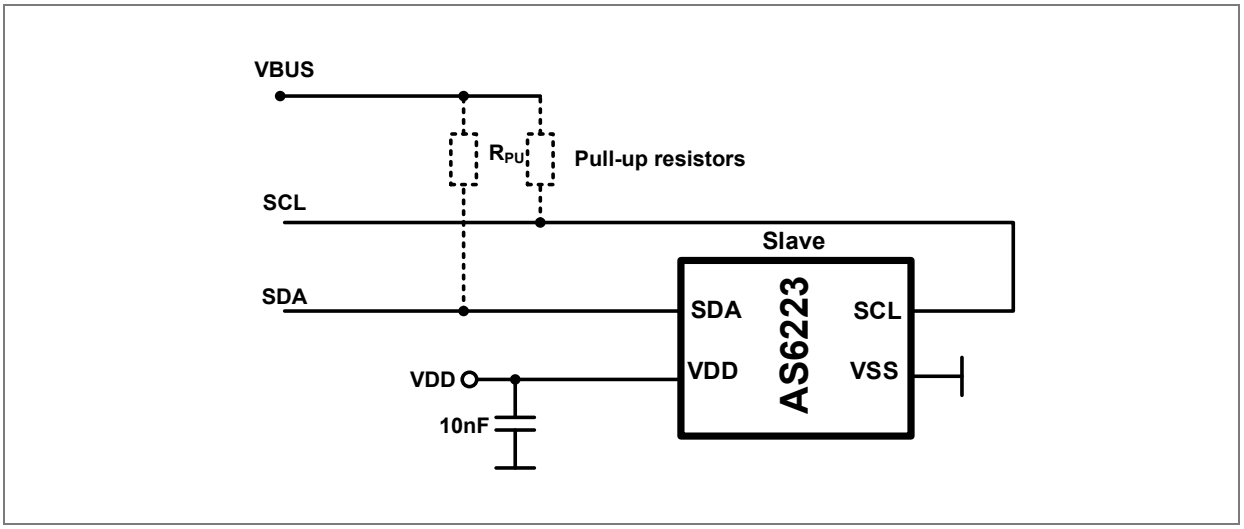
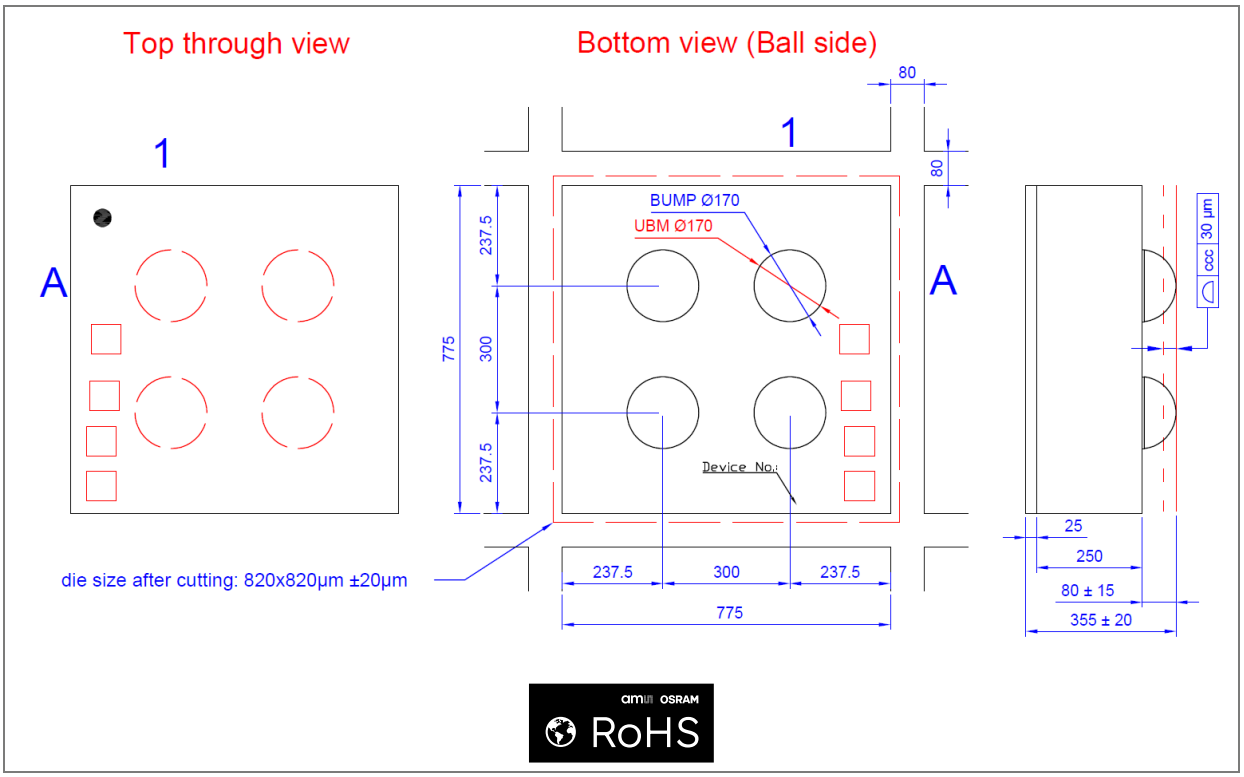


Table 25: Values for external components

Parameter	Min	Typ	Unit
Decoupling capacitor	10		nF
Pull-up resistors		10	kΩ

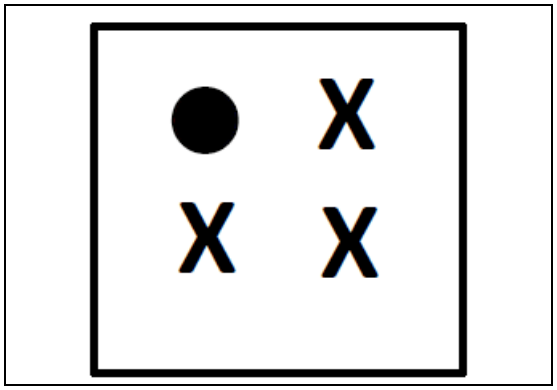
8 Package drawings & markings

Figure 10: WLCSP outline drawing (Bottom & side view)



(1) All dimensions are in micrometers. Angles in degrees.
(2) Dimensioning and tolerance conform to ASME Y14.5M-1994.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 11: WLCSP package marking/code for AS6223



XXX Tracecode
● Pin A1 indicator

9 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous released version to current revision v5-00	Page
Change power naming in the application example from VDD to VBUS for pull-up resistors	32

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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