

am^u AS7100

Datasheet

Published by ams-OSRAM AG

Tobelbader Strasse 30, 8141 Premstaetten, Austria

Phone +43 3136 500-0

ams-osram.com

© All rights reserved

am^u OSRAM

Table of contents

1	General description	4
1.1	Key benefits & features.....	5
1.2	Applications	6
1.3	Block diagram	7
2	Ordering information	8
3	Pin assignment	9
3.1	Pin diagram.....	9
3.2	Pin description	10
4	Absolute maximum ratings	12
5	Electrical characteristics.....	13
5.1	Power consumption	16
6	Optical characteristics	18
7	Typical operating characteristics	20
8	Detail description	24
8.1	Operation modes	24
8.2	Power up.....	27
8.3	LED driver.....	28
8.4	On-chip photodiodes.....	31
8.5	Analog to digital converter	32
8.6	Data processing.....	37
8.7	Proximity detection	38
8.8	Measurement sequencer	40
8.9	Communication interfaces	50
8.10	On chip temperature measurement	63
8.11	FIFO description	65
9	Register description	70
9.1	Register map	70

9.2 Detailed register description 75

10 Application information..... 137

10.1 Schematic 137

10.2 External components 140

10.3 PCB layout..... 141

10.4 PCB pad layout..... 142

11 Package drawings & markings 143

12 Tape & reel information 144

13 Storage information 145

13.1 Moisture sensitivity 145

13.2 Shelf life 145

13.3 Floor life 145

13.4 Rebaking instructions 146

14 Revision information 147

15 Legal information 148

AS7100 Proximity sensor for optical force sensing applications

1 General description

The AS7100 device is a low noise, high dynamic range proximity detection solution. It has been optimized for optical force sensing applications designed for automotive and industrial markets.

The device features two low-noise ADC channels, capable of simultaneous data acquisition of two programmable photodiode arrays, a relative temperature sensor, an integrated 940nm IRED and an advanced IRED driver. It comes in an optimized 4.0mm x 3.05mm x 0.7mm package.

The proximity function synchronizes IR emission and detection to sense nearby objects. The architecture of the engine features low noise, high dynamic range, ambient light subtraction, advanced crosstalk cancelation, FIFO, and interrupt-driven I²C communication.

Sensitivity, power consumption, and noise can be optimized with adjustable IRED timing and power. The proximity engine recognizes detect/release events and produces a configurable interrupt whenever the proximity result crosses the upper or lower threshold settings.

1.1 Key benefits & features

The benefits and features of AS7100, Proximity sensor for optical force sensing applications are listed below:

Table 1: Added value of using AS7100

Benefits	Features
Qualifications	• AEC-Q102-003 Qualified
Automotive and Industrial design flexibility	• 4.0mm x 3.05mm x 0.7mm module with wettable flanks • On-chip temperature sensor • Dual photodiode architecture • Centered emitter and detector package design
Optimized for Optical force sensing	• Fully programmable photodiode array • Wide dynamic range with up to 20 bits of resolution • Programmable gain and integration time 256 Byte FIFO • Integrated factory calibrated 940nm IRED
Proximity detection	• Crosstalk and ambient light cancellation • Split near and far photodiode array for short- and long-range proximity sensing. • Programmable IRED driver capable of sinking up to 250mA
Low power consumption	• 3.3V power supply with 3.3V and 1.8V I²C bus • I²C communication with data rate up to 400 kHz • Sleep mode (200nA) with fast wakeup • Interrupt driven device
Integrated status checking for all device functions	• Digital and analog ALS saturation flags • Proximity saturation flag • SYNC status flag

1.2 Applications

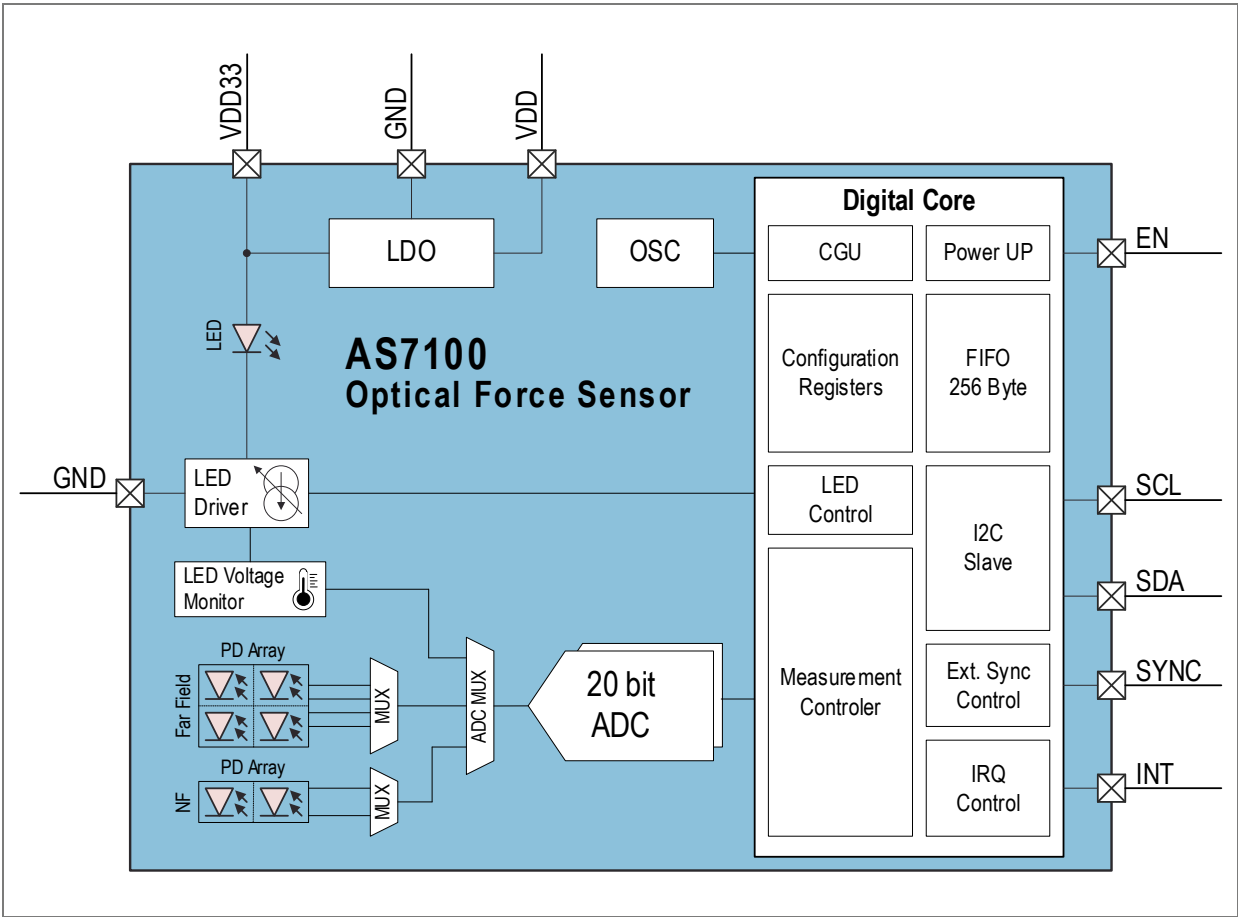
AS7100 integrates multiple applications within one device. The AS7100 applications include:

- Smart surfaces
- Steering wheel switches
- Seat & side mirror adjustment
- Key fobs
- Control knob
- Smart appliances
- Light switches & dimmers

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS7100



2 Ordering information

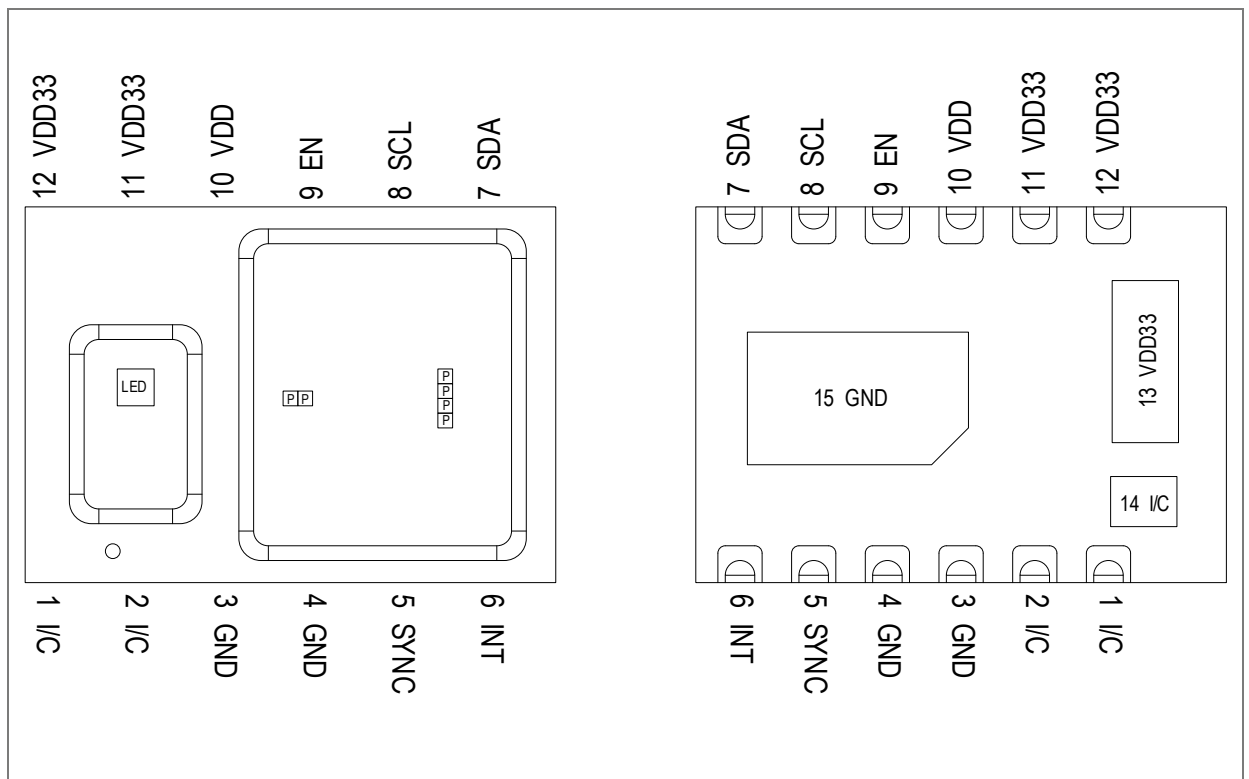
Product type	Ordering code	I/O voltage V_{IO_VDD}	7-bit I ² C address	Delivery form	Delivery quantity
AS7100	Q65115A2700	3.3V	0x55	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2697	3.3V	0x53	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2699	3.3V	0x51	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2698	3.3V	0x52	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2701	3.3V	0x54	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2715	3.3V	0x56	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2716	3.3V	0x57	Tape & reel (13")	5000 pcs/reel
AS7100	Q65115A2717	3.3V	0x58	Tape & reel (13")	5000 pcs/reel

3 Pin assignment

3.1 Pin diagram

Device pinout is described below:

Figure 2: Pin diagram of AS7100



- (1) Pin 13 is connected internally to pin 11 and pin 12.
- (2) Pin 14 is connected internally to pin 1 and pin 2.
- (3) Do not connect pin 14 externally.
- (4) Pin 15 is connected internally to pin 3 and pin 4.
- (5) Exposed pads can be used for heat dissipation.

3.2 Pin description

Table 2: Pin description of AS7100

Pin number	Pin name	Pin type ⁽¹⁾	Description
1	I/C	AO	This is a pin for test production side testing only. Pin must not be connected externally. Please leave this pin unconnected and floating.
2	I/C	AO	This is a pin for test production side testing only. Pin must not be connected externally. Please leave this pin unconnected and floating.
3	GND	G	0V ground terminal of AS7100. All device voltages are referenced to GND.
4	GND	G	0V ground terminal of AS7100. All device voltages are referenced to GND.
5	SYNC	DI	Digital synchronization input pin order to synchronize multiple devices or synchronize AS7100 to other third-party sensors.
6	INT	DO	This is the digital interrupt open drain output pin. In default configuration it is configured to active low operation mode. Please mind that an external pull up resistor is mandatory for operation. This pin does not support push pull output mode. In case INT pin is not used pin must be connected to ground.
7	SDA	DIO	I ² C serial data I/O terminal. This pin requires external pull up resistors for operation.
8	SCL	DI	I ² C serial clock input terminal. This pin requires external pull up resistor for operation.
9	EN	DI	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.
10	VDD	P	This is the positive output terminal of the internal 1.8V LDO which supplies AS7100 digital and analog blocks. This pin must be connected to an external low ESR capacitor C _{VDD} . Please refer to chapter 10.2 for recommended capacitors.
11	VDD33	P	Positive 3.3V supply terminal for AS7100. Please refer to symbol V _{DD33} listed in chapter 5 Electrical characteristics for power supply operating range of the device.
12	VDD33	P	Positive 3.3V supply terminal for AS7100. Please refer to symbol V _{DD33} listed in chapter 5 Electrical characteristics for power supply operating range of the device.
13	VDD33	P	Positive 3.3V supply terminal for AS7100. Please refer to symbol V _{DD33} listed in chapter 5 Electrical characteristics for power supply operating range of the device.
14	I/C	AO	This is a pin for test production side testing only. Pin must not be connected externally. Please leave this pin unconnected and floating.

Pin number	Pin name	Pin type ⁽¹⁾	Description
15	GND	G	Ground. All voltages are referenced to GND.

- (1) Abbreviations:
- DI Digital Input
 - DO Digital Output
 - DIO Digital Input/Output
 - AI Analog Input
 - AO Analog Output
 - P Power Supply
 - G Ground

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages are with respect to GND. Device parameters are guaranteed at $V_{DD33} = 3.3V$ and $T_A = 25^{\circ}C$ unless otherwise noted.

Table 3: Absolute maximum ratings of AS7100

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V _{VDD_MAX}	Maximum supply voltage to ground	-0.3	1.98	V	Applicable to pin VDD pin to GND
V _{VDD33_MAX}	Maximum supply voltage to ground	-0.3	3.6	V	Applicable to all VDD33 pins to GND
V _{IO_MAX}	Max. digital input / output voltage	-0.3	V _{VDD} + 0.3 V; max. 3.6 V	V	Applicable to pins EN, SCL, SDA, SYNC and INT
Electrostatic discharge					
ESD _{HBM}	Electrostatic discharge HBM	± 2000		V	Applicable to all pins according to AEC - Q100-002 REV-E
ESD _{CDM}	Electrostatic discharge CDM	± 750		V	Applicable to all pins according to AEC - Q100-011 REV-D
I _{SCR}	Input current (latch-up immunity)	± 100		mA	Applicable to all pins according to AEC-Q100-004 REV-D, Class II; T _A = 125°C
Temperature ranges and storage conditions					
T _A	Operating ambient temperature	-40	110	°C	
T _J	Junction temperature range	-40	125	°C	
T _{STRG}	Storage temperature range	-40	110	°C	
T _{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 ⁽¹⁾
RH _{NC}	Relative humidity (non-condensing)		85	%	
MSL	Moisture sensitivity level	3			Represents a max. floor lifetime of 168h

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed at $V_{VDD33} = 3.3\text{ V}$ and $T_A = 25\text{ °C}$ unless otherwise noted.

Table 4: AS7100 electrical characteristics, $V_{VDD33} = 3.3\text{ V}$, $T_A = 25\text{ °C}$ (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Electrical parameters						
V_{VDD}	Internal LDO output voltage.		1.7	1.8	1.98	V
V_{VDD33}	Supply Voltage to Sensor & IRED		2.4	3.3	3.6	V
f_{OSC}	Oscillator frequency		8.24	8.4	8.56	MHz
Digital I/O						
V_{EN_HIGH}	EN pin high input voltage level	$V_{VDD33} = 2.4\text{ V} - 3.6\text{ V}$	1.4		V_{VDD33}	V
V_{EN_LOW}	EN pin low input voltage level	$V_{VDD33} = 2.4\text{ V} - 3.6\text{ V}$	0		0.3	V
$V_{IL1.8V}$	1.8V digital input low voltage	I ² C interface voltage 1.8V; Applicable to pin SCL, SDA and SYNC; 1.8V compliant AS7100 must to be used in application	0		0.54	V
$V_{IH1.8V}$	1.8V digital input high voltage	I ² C interface voltage 1.8V; Applicable to pin SCL, SDA and SYNC; 1.8V compliant AS7100 must be used in application	1.26		V_{VDD18}	V
$V_{IL3.3V}$	3.3V digital input low voltage	I ² C interface voltage 3.3V; Applicable to pin SCL, SDA and SYNC; 3.3V compliant AS7100 must be used in application	0		1.0	V
$V_{IH3.3V}$	3.3V digital input high voltage	I ² C interface voltage 3.3V; Applicable to pin SCL, SDA and SYNC; 3.3V compliant AS7100 must be used in application	2.31		V_{VDD33}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL1.8V}$	1.8V digital output low voltage	6mA sink current; applicable to pin INT and SDA; pins configured to full driving strength; 1.8V compliant AS7100 must be used in application	0		0.4	V
$V_{OH1.8V}$	1.8V digital output high voltage	6mA source current; applicable to pin INT and SDA; pins configured to full driving strength; 1.8V compliant AS7100 must be used in application	2.97		V_{DD33}	V
$V_{OL1.8V}$	1.8V digital output low voltage	6mA sink current; applicable to pin INT and SDA; pins configured to full driving strength; 1.8V compliant AS7100 must be used in application	0		0.4	V
$V_{OH1.8V}$	1.8V digital output high voltage	6mA source current; applicable to pin INT and SDA; pins configured to full driving strength; 1.8V compliant AS7100 must be used in application	1.62		V_{DD18}	V
I_{LEAK}	Digital input leakage current	Applicable to pin SCL, SDA, and SYNC	-5		5	μA
Other characteristics						
t_{ACTIVE}	Time from power-on to ready to receive I ² C commands ⁽¹⁾				2	ms
LED driver						
LED_{RES}	LED driver resolution			6		Bit
I_{LED}	LED driving current	Register $IRANGE = 0$	0		250	mA
		Register $IRANGE = 1$	0		25	mA
V_{COMPL}	Compliance voltage for LED driver	Register $IRANGE = 0$			0.6	V
		Register $IRANGE = 1$			0.3	V
LED_{DUTY}	LED duty cycle	$I_{LED} = 250\text{ mA}$			5	%
IR LED						
λ_{PEAK}	Peak wavelength	$I_F = 100\text{ mA};$		950		nm

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\lambda_{\text{CENTROID}}$	Centroid Wavelength	$I_F = 100 \text{ mA}$	930	940	950	nm
TC_λ	Temperature coefficient of wavelength			0.3		nm/K
TC_I	Temperature coefficient of brightness	-0.5 %/K medium -40°C to 125°C @100mA		-0.5		%/K
TC_V	Temperature coefficient of voltage	$I_F = 100 \text{ mA}$		-1.3		mV/K
Φ_e	Total radiant flux	$I_F = 100 \text{ mA}$		63.5		mW
$\Delta\lambda$	Spectral bandwidth	At 50% $I_{\text{rel,max}}$ (FWHM)		42		nm
t_r	Rise time	Rise time (10%/ 90%) $I_F = 100 \text{ mA}$; $RL = 50 \Omega$		12		ns
t_f	Fall time	Fall time (10% / 90%) $I_F = 100 \text{ mA}$; $RL = 50 \Omega$		12		ns
I_R	Reverse current				300	nA
I_P	Pulsed current				250	mA
V_F	Forward voltage	$I_F = 100 \text{ mA}$; $t_p = 20 \text{ ms}$		1.5	1.7	V

(1) t_{ACTIVE} does not include the situation when the device needs extra time to wait for the Bus Idle Condition (t_{IDLE}).

5.1 Power consumption

Table 5: AS7100 typical power consumption, $V_{DD33} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Electrical parameters						
I_{PDWN}	Power down current	EN pin = low; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 0\text{ V}$			1	μA
I_{SLEEP}	Sleep mode current consumption	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; LED disabled; no measurement on going; oscillator disabled; ADC disabled		76		μA
I_{IDLE}	IDLE current consumption	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 0\text{ mA}$		400		μA
I_{ACTIVE}	Active current consumption	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 0\text{ mA}$; 1 ADC channel enabled		700		μA
I_{STBY}	Current consumption during standby enabled	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 0\text{ mA}$		400		μA
I_{Force_25Hz}	Force current consumption 25Hz	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 5.08\text{ mA}$; $t_{sample} = 151\text{ }\mu\text{s}$; $t_{Integration} = 1363\text{ }\mu\text{s}$; $t_{period} = 40\text{ ms}$; 1 ADC channel enabled; STANDBY_EN = 0		618		μA
$I_{Force_25Hz_STBY}$	Force current consumption 25Hz with standby enabled	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 5.08\text{ mA}$; $t_{sample} = 151\text{ }\mu\text{s}$; $t_{Integration} = 1363\text{ }\mu\text{s}$; $t_{period} = 40\text{ ms}$; 1 ADC channel enabled; STANDBY_EN = 1		436		μA
I_{Force_100Hz}	Force current consumption 100Hz	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 5.08\text{ mA}$; $t_{sample} = 151\text{ }\mu\text{s}$; $t_{Integration} = 1363\text{ }\mu\text{s}$; $t_{period} = 10\text{ ms}$; 1 ADC channel enabled; STANDBY_EN = 0		689		μA
$I_{Force_100Hz_STBY}$	Force current consumption 100Hz with standby enabled	EN pin = high; $V_{DD33} = 3.3\text{ V}$; $V_{DD} = 1.8\text{ V}$; $I_{LED} = 5.08\text{ mA}$; $t_{sample} = 151\text{ }\mu\text{s}$; $t_{Integration} = 1363\text{ }\mu\text{s}$; $t_{period} = 10\text{ ms}$; 1 ADC channel enabled; STANDBY_EN = 1		528		μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{FD_25Hz_STBY}$	Differential force current consumption 25Hz with standby enabled	EN pin = high; $V_{VDD33} = 3.3\text{ V}$; $V_{VDD} = 1.8\text{ V}$; $I_{LED} = 5.08\text{ mA}$; $t_{sample} = 151\text{ }\mu\text{s}$; $t_{Integration} = 1363\mu\text{s}$; $t_{period} = 40\text{ ms}$; 2 ADC channel enabled; STANDBY_EN = 1		440		μA
$I_{FD_100Hz_STBY}$	Differential force current consumption 100Hz with standby enabled	EN pin = high; $V_{VDD33} = 3.3\text{ V}$; $V_{VDD} = 1.8\text{ V}$; $I_{LED} = 5.08\text{ mA}$; $t_{sample} = 151\text{ }\mu\text{s}$; $t_{Integration} = 1363\mu\text{s}$; $t_{period} = 10\text{ ms}$; 2 ADC channel enabled; STANDBY_EN = 1		550		μA
I_{PROX_10Hz}	Proximity measurement 10Hz standby disabled	EN pin = high; $V_{VDD33} = 3.3\text{ V}$; $V_{VDD} = 1.8\text{ V}$; $I_{LED} = 50.8\text{ mA}$; $t_{sample} = 1200\text{ }\mu\text{s}$; $t_{Integration} = 10.8\text{ ms}$; $t_{period} = 100\text{ ms}$; 1 ADC channel enabled; STANDBY_EN = 0		1.2		mA
$I_{PROX_10Hz_STBY}$	Proximity measurement 10Hz standby enabled	EN pin = high; $V_{VDD33} = 3.3\text{ V}$; $V_{VDD} = 1.8\text{ V}$; $I_{LED} = 50.8\text{ mA}$; $t_{sample} = 1200\text{ }\mu\text{s}$; $t_{Integration} = 10.8\text{ ms}$; $t_{period} = 100\text{ ms}$; 1 ADC channel enabled; STANDBY_EN = 1		1.1		mA

6 Optical characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed at $V_{DD33} = 3.3V$ and $T_A = 25^{\circ}C$ unless otherwise noted.

Table 6: Proximity photodiode optical characteristics ($V_{DD33} = 3.3V$, $T_A = 25^{\circ}C$ unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Near photodiodes response absolute	$I_{LED} = 187\text{ mA}$; $irange = 0$; $mod1_gain1 = 0x01$ (2 x gain) $pp_mod1_gain = 0x03$ (0 dB gain) $prx_sample_count1 = 0x00$; $t_{Integration} = 2.25\text{ ms}$; $t_{SAMPLE} = 250\text{ }\mu s$; $t_{LED_WAIT} = 21.4\text{ }\mu s$; $t_{LED_ON} = 81.4\text{ }\mu s$; Target distance: 2 mm PD1 and PD2 enabled.		10800		counts
Far photodiodes response absolute	$I_{LED} = 187\text{ mA}$; $irange = 0$; $mod1_gain1 = 0x01$ (2 x gain) $pp_mod1_gain = 0x03$ (0 dB gain) $prx_sample_count1 = 0x00$; $t_{Integration} = 2.25\text{ ms}$; $t_{SAMPLE} = 250\text{ }\mu s$; $t_{LED_WAIT} = 21.4\text{ }\mu s$; $t_{LED_ON} = 81.4\text{ }\mu s$; Target distance: 2 mm PD3, PD4, PD5 and PD6 enabled.		27700		counts
SNR _{1mm}	$I_{LED} = 25\text{ mA}$; $mod1_gain1 = 0x01$ (2 x gain) $pp_mod1_gain = 0x03$ (0 dB gain) $prx_sample_count1 = 0x00$; $t_{Integration} = 25.2\text{ ms}$; $t_{SAMPLE} = 1\text{ ms}$; $t_{LED_WAIT} = 0\text{ ms}$; $t_{LED_ON} = 9\text{ ms}$; Target material: 90% white card Target size: 100 mm x 120mm Target distance: 1mm Applicable to PD1 - PD5 No ambient light		82		dB
SNR _{3mm}	$I_{LED} = 25\text{ mA}$; $mod1_gain1 = 0x01$ (2 x gain) $pp_mod1_gain = 0x03$ (0 dB gain) $prx_sample_count1 = 0x00$; $t_{Integration} = 25.2\text{ ms}$; $t_{SAMPLE} = 1\text{ ms}$; $t_{LED_WAIT} = 0\text{ ms}$; $t_{LED_ON} = 9\text{ ms}$; Target material: 90% white card Target size: 100 mm x 120mm Target distance: 3 mm Applicable to PD1 - PD5 No ambient light		81		dB

Parameter	Conditions	Min	Typ	Max	Units
SNR _{10mm}	<i>I</i> _{LED} = 25 mA; <i>mod1_gain1</i> = 0x01 (2 x gain) <i>pp_mod1_gain</i> = 0x03 (0 dB gain) <i>prx_sample_count1</i> = 0x0; <i>t</i> _{Integration} = 25.2 ms; <i>t</i> _{SAMPLE} = 1 ms; <i>t</i> _{LED_WAIT} = 0 ms; <i>t</i> _{LED_ON} = 9 ms; Target material: 90% white card Target size: 100 mm x 120mm Target distance: 10 mm Applicable to PD1 - PD5 No ambient light		75		dB
Proximity Detection Range	<i>I</i> _{LED} = 246 mA; <i>mod1_gain1</i> = 0x04 (16 x gain) <i>pp_mod1_gain</i> = 0x03 (0 dB gain) <i>prx_sample_count1</i> = 0x01; <i>t</i> _{Integration} = 25.2 ms; <i>t</i> _{SAMPLE} = 1.8 ms; <i>t</i> _{LED_WAIT} = 0 ms; <i>t</i> _{LED_ON} = 1.8 ms; Target material: 18% gray card Target size: 100 mm x 120mm No ambient light	0		300	mm

7 Typical operating characteristics

Figure 3: PD1 proximity count value vs. target distance (90% white reflector card)

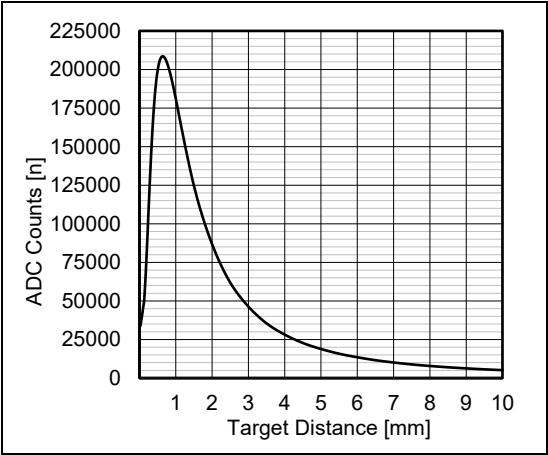


Figure 4: PD2 proximity count value vs. target distance (90% white reflector card)

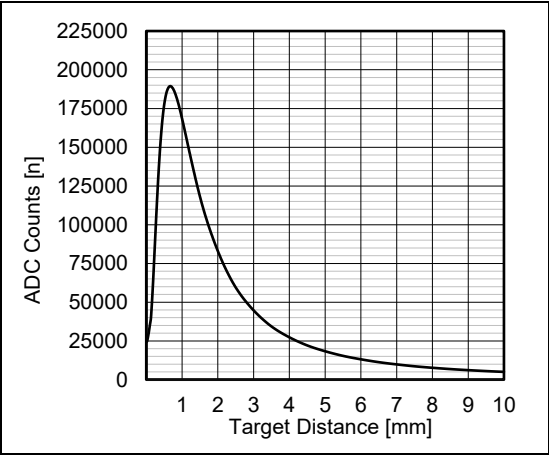


Figure 5: PD3 proximity count value vs. target distance (90% white reflector card)

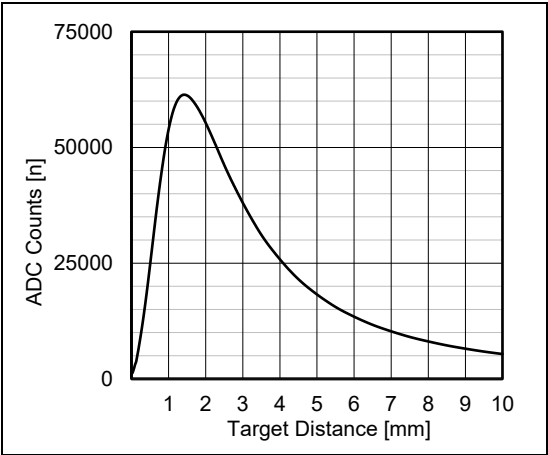


Figure 6: PD4 proximity count value vs. target distance (90% white reflector card)

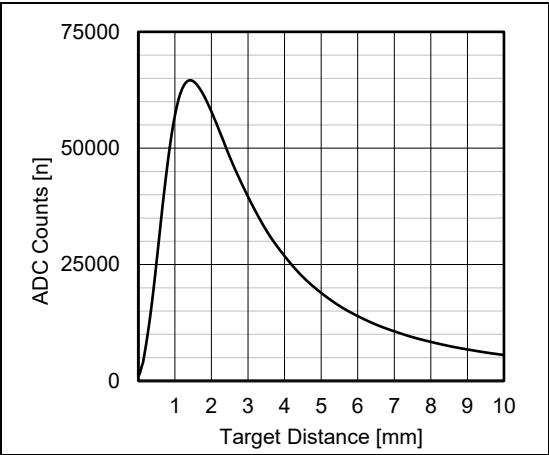


Figure 7: PD5 proximity count value vs. target distance (90% white reflector card)

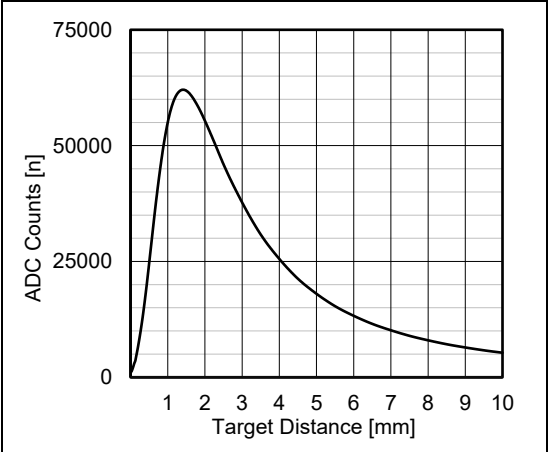


Figure 8: Relative sensitivity vs. wavelength for all photodiodes

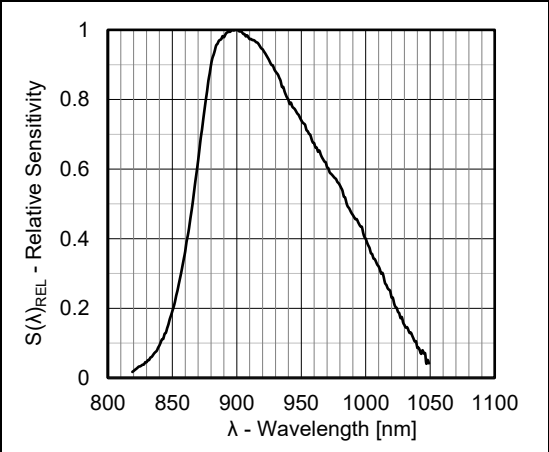


Figure 9: IR LED FoI relative radiation characteristics

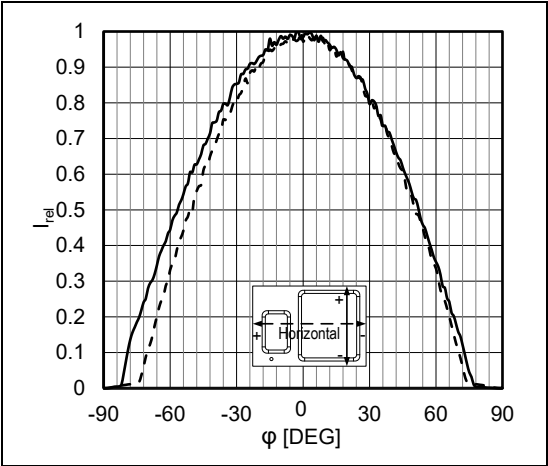


Figure 10: PD1 FoV relative sensitivity

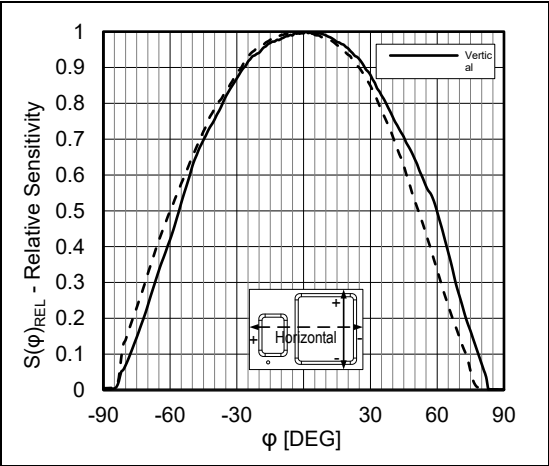


Figure 11: PD2 FoV relative sensitivity

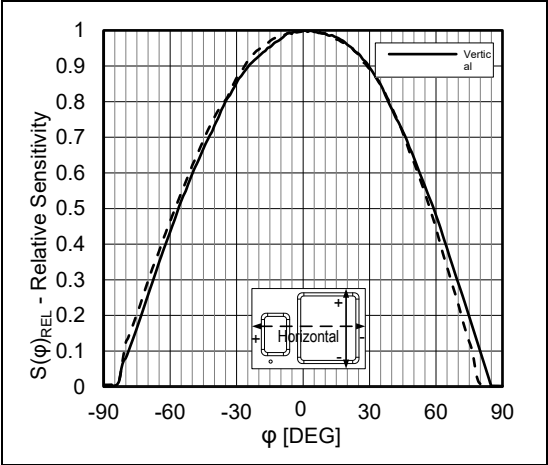


Figure 12: PD3 FoV relative sensitivity

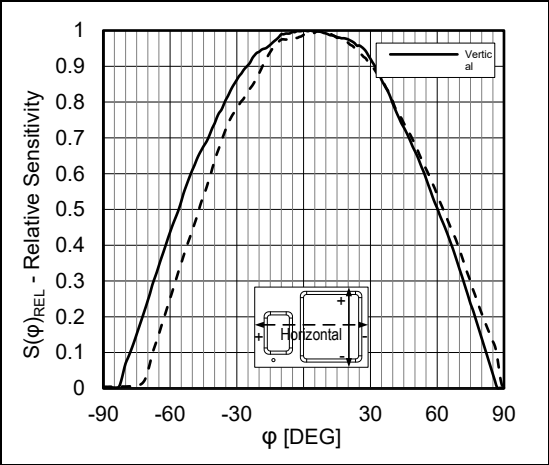


Figure 13: PD4 FoV relative sensitivity

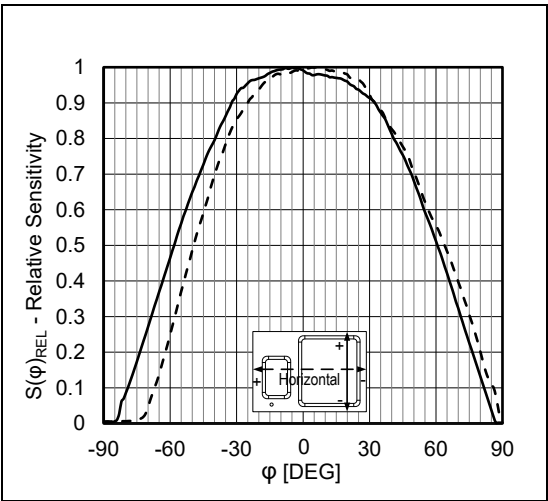


Figure 14: PD5 FoV relative sensitivity

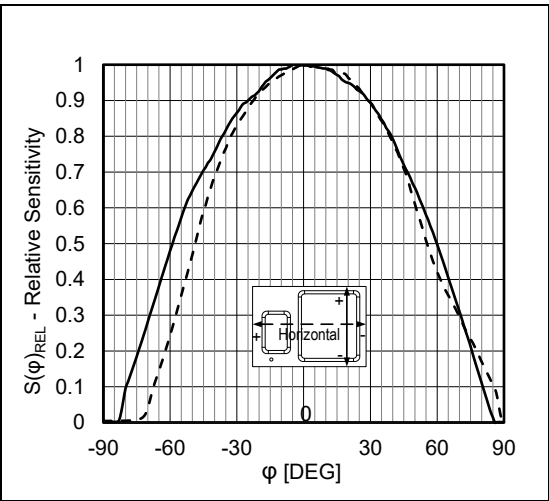


Figure 15: PD6 FoV relative sensitivity

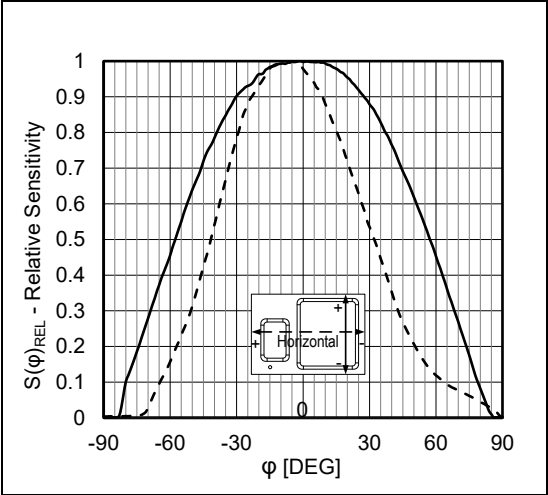
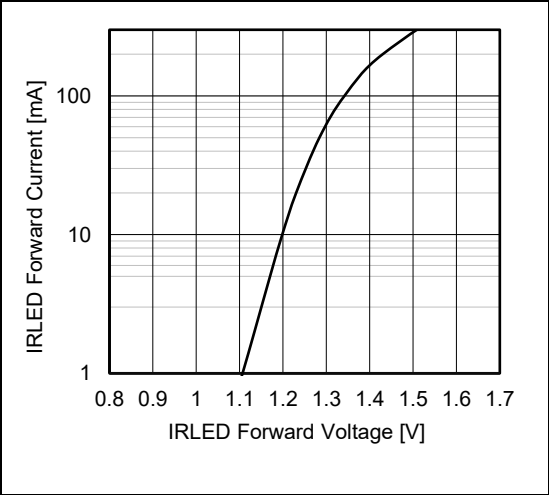


Figure 16: LED forward current vs. forward voltage

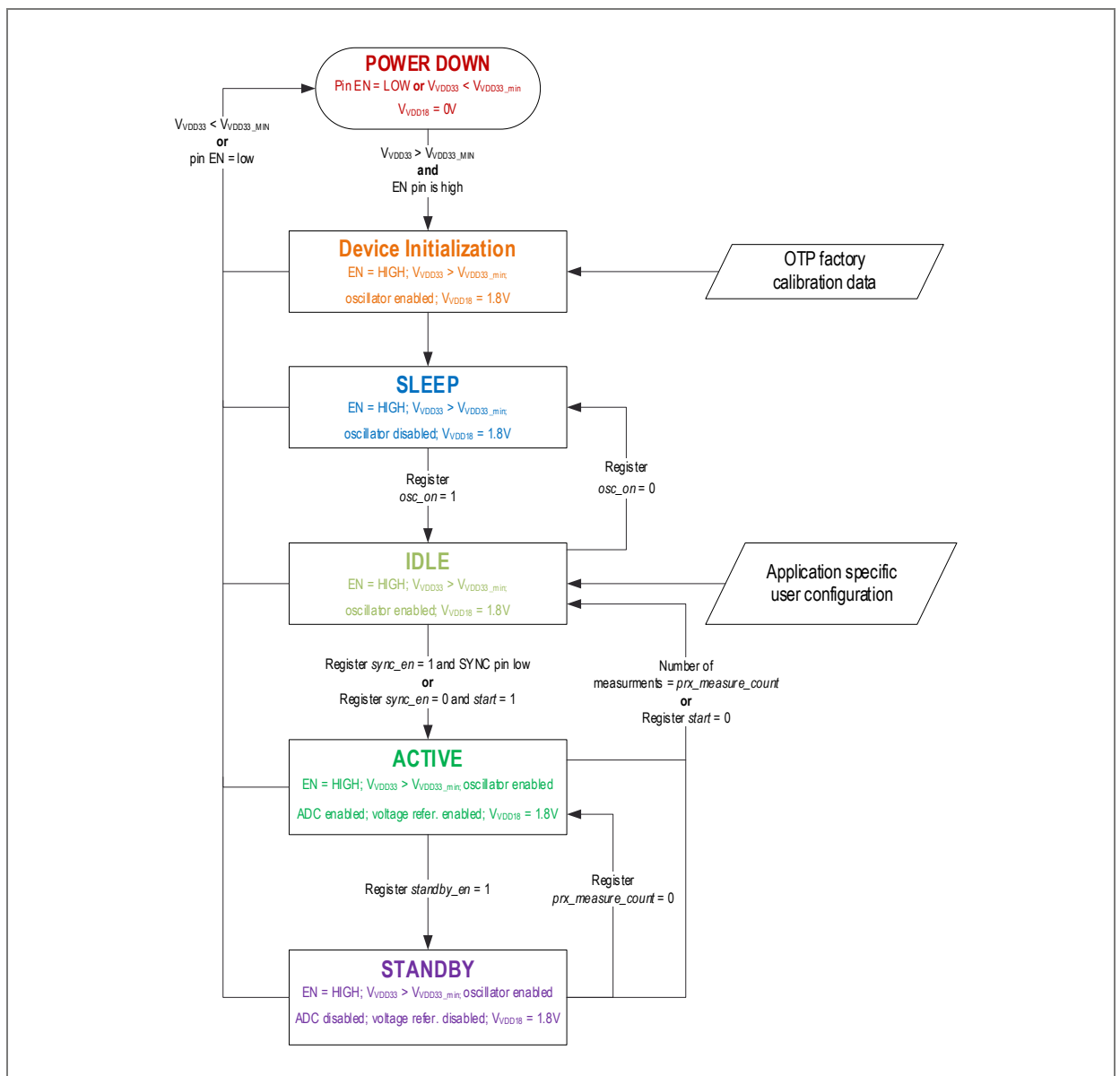


8 Detail description

8.1 Operation modes

This chapter provides information about the different operation modes of AS7100. For illustration purpose Figure 17 shows a simplified state diagram how each operation mode can be entered.

Figure 17: Operation modes state diagram



8.1.1 POWER DOWN mode

This is the operation mode which provides lowest power consumption. In Power Down operation mode, the EN pin of AS7100 is driven low by its host processor and the on-chip LDO which provides the device digital and analog chip supply V_{DD} is disabled. In this operation mode there is no host communication via the I²C interface possible. Please refer to chapter 5.1 and parameter I_{PDWN} for a detailed current consumption value in this operation mode.

8.1.2 SLEEP mode

The SLEEP operation mode is entered once VDD33 pin reaches its minimum supply voltage V_{VDD33_MIN} and the enable pin of AS7100 is driven high by its host processor. In this mode the device wakes up and runs through the device initialization phase where the on-chip oscillator is enabled and all production trimming registers are read out. The production trimming registers are used to compensate production variations of the voltages and currents to guarantee highest accuracy for the later optical force and ambient light measurements. After successful readout of all registers the oscillator is shot down again and the device is in SLEEP operation mode. The device is now ready for I²C host communication.

8.1.3 IDLE mode

The IDLE operation mode is the preliminary stage to the ACTIVE mode. In this operation mode the on-chip oscillator is enabled which prepares the device to be ready for a measurement start which can be triggered via SYNC pin or register control once the device is configured for measurements correctly.

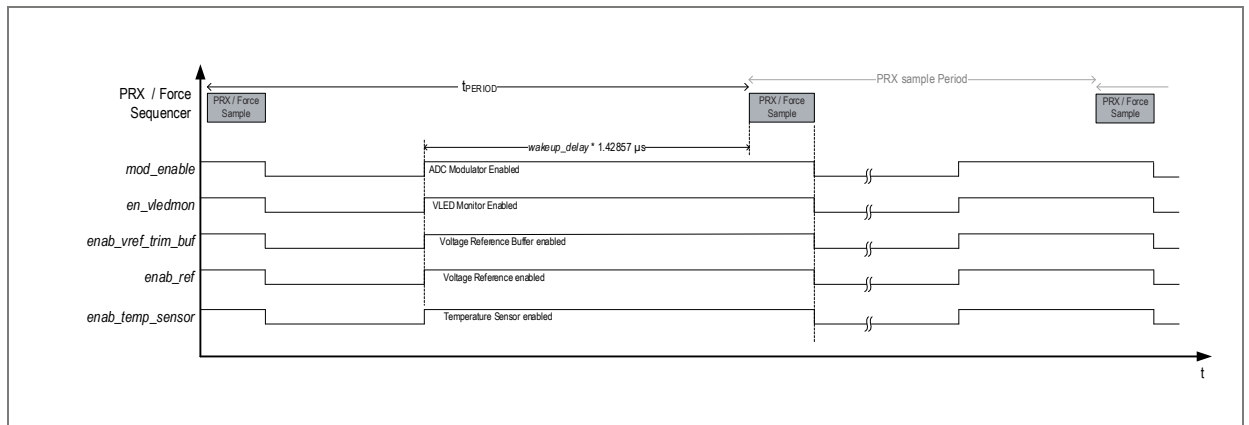
8.1.4 ACTIVE mode

The ACTIVE operation mode is entered once a measurement is started. Once the measurement gets started all relevant blocks and voltage references are enabled automatically.

8.1.4.1 Standby mode

Once the device is in ACTIVE operation mode and a measurement is ongoing a Standby mode can be enabled. This is a power save operation mode where during measurement breaks unused hardware blocks are disabled to reduce overall power consumption. A simplified timing diagram, which shows the standby mode control registers with its related hardware blocks as well the function of the **WAKEUP_DELAY** register, is shown in Figure 18. In the timing diagram we can see the measurement period time t_{PERIOD} which is typically much longer compared to the active measurement time. Therefore, it makes sense to disable hardware blocks during measurement breaks. Since all analog hardware blocks like the ADCs and voltage references do need some time to startup after power down the **WAKEUP_DELAY** register is used to define the startup time prior to a measurement start. This makes sure that all relevant blocks are properly running when the proximity measurement is supposed to start. To select which block is powered down during standby mode the **STANDBY_EN** register is used. Each bit represents a dedicated hardware block of AS7100 which can be powered down during a measurement pause.

Figure 18: Standby mode timing diagram



The wakeup delay time $t_{\text{STDB_WAKEUP}}$ can be calculated with the calculation shown in Equation 1.

Equation 1: Standby wakeup delay time

$$t_{\text{STBY_WAKEUP}} = \text{WAKEUP_DELAY} * \frac{1}{700000} [\text{s}]$$

$t_{\text{STBY_WAKEUP}}$... Standby wakup time for powered down hardware blocks

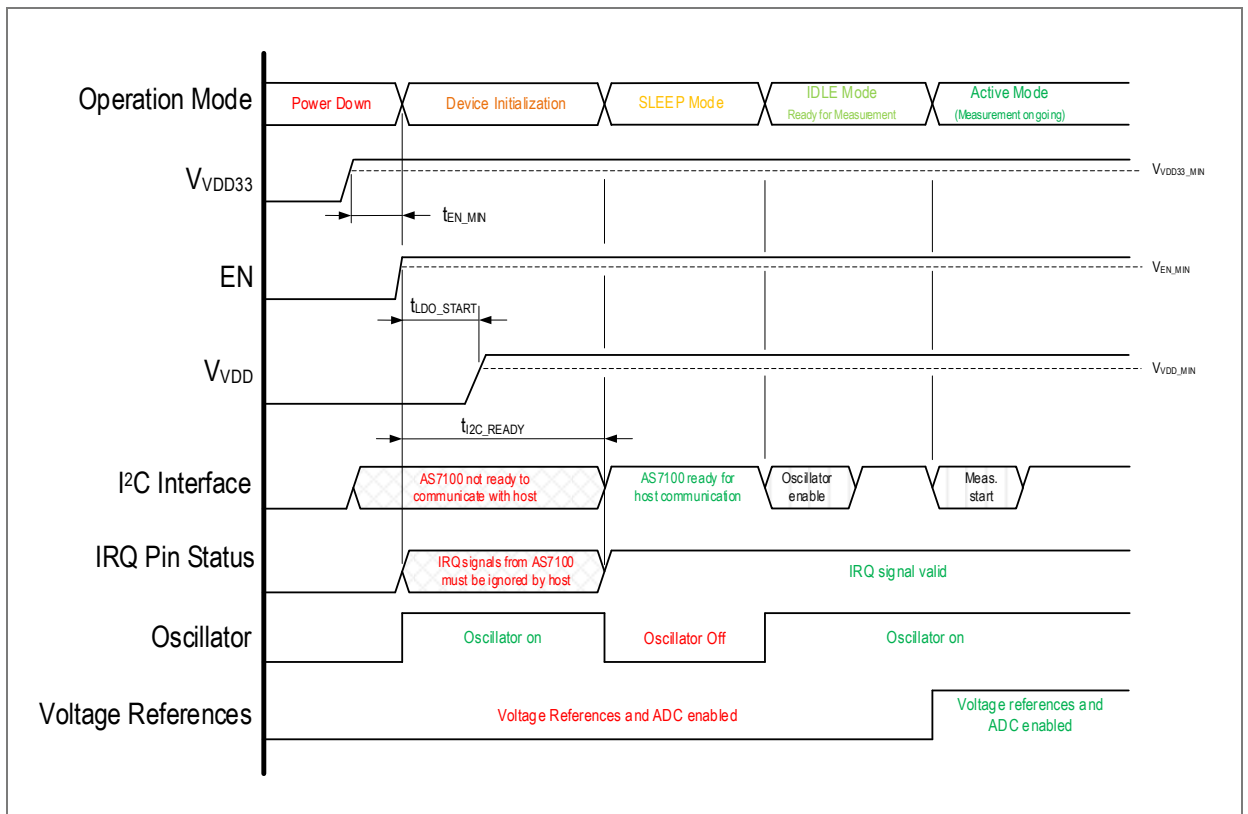
WAKEUP_DELAY ... Register to control standby wakeup time

8.2 Power up

The following chapter describes the power up sequence of AS7100. First step in the power up sequence is that a valid and stable supply voltage is present at VDD33 pin. The voltage level must be at least above V_{VDD33_MIN} as shown in Figure 19. Once the supply is settled the device EN pin can be pulled high to start with the Device Initialization phase of AS7100. During initialization, the device cannot accept I²C transactions and will deterministically send NAK for any I²C requests. All communication with the device must be delayed, and all outputs from the device (i.e. interrupts) must be ignored until device Initialization phase is completed. After successful initialization, the device enters IDLE Operation mode in which the internal oscillator and other circuitry are in default configuration disabled, resulting in low power consumption.

In order to start measurements, the internal oscillator, the references and the measurement setup have to be programmed by the I²C interface to enter device Active operation mode.

Figure 19: AS7100 start up timing diagram



8.2.1 Parameter

Table 7: Startup timing parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{EN_MIN}	EN pin startup delay after VDD33 supply is available		0			μs
t_{I2C_READY}	I ² C startup time				2	ms

8.3 LED driver

AS7100 features an integrated 940nm LED which is internally connected to an LED driver current sink which can support up to 250mA LED driving current with an option to switch to 25mA current range via register **IRANGE**. The LED current for proximity and optical force measurements can be programmed with a 6-bit register depending on application use cases for both measurement subsamples independently via register **LED_ISINK1** and **LED_ISINK2**. This allows for different LED current configuration for both subsamples in order to Address for example with sub-sample one a proximity measurement and with sub sample two an optical force measurement where both measurements typically demand different LED current configuration. In addition to the LED current the block provides also the option to configure the LED on time for a proximity and optical force measurement via register **LED_ON_TIME**. There is also the option to program LED wait time with register **LED_WAIT_TIME**. Please refer to Figure 31 and Figure 33 for more detailed timing diagrams for t_{LED_ON} and t_{LED_WAIT} timings.

8.3.1 LED forward voltage monitoring

During operation of the device there is also an option to switch from chip temperature monitoring (please refer to chapter 8.10 for more details) to LED driver voltage monitoring. In this case the on-chip temperature monitoring is suspended and LED driver voltage is measured instead. In order to enable this function the LED voltage monitoring measurement buffer needs to be enabled via register **EN_VLEDMON**. Furthermore, it is necessary to connect the cathode of the LED to the voltage measurement buffer circuit by setting bit **EN_LED_MON_CONNECT** and switch the multiplexer from temperature input to LED voltage monitoring input with register **ADC_CH2SEL**. The ADC data for the voltage measurement can be read out in **TEMP_DAT_0** and **TEMP_DATA_1** register and need to be combined to a 12 bit value like it is shown Equation 2.

Equation 2: LED voltage monitoring ADC data calculation

$$ADC_{LEDM_DATA} = 256 * TEMP_DATA_1 + TEMP_DATA_0[counts]$$

ADC_{LEDM_DATA} 12 bit LED monitor ADC voltage data

$TEMP_DATA_0$ lower 8 bit voltage measurement data

$TEMP_DATA_1$ upper 4 bit voltage measurement data

The calculation of the resulting LED forward voltage depends on the configuration of the **VLEDMON_IN_SEL** register. In case **VLEDMON_IN_SEL** is set to zero the LED forward voltage is measured directly between VDD33 pin and the LED cathode. In case is **VLEDMON_IN_SEL** set to one the voltage across the LED driver is measured and needs to be subtracted from the LED supply voltage to get the LED forward voltage. Equation 3 shows the LED forward voltage calculation for the direct measurement with **VLEDMON_IN_SEL** register set to zero.

Equation 3: LED voltage calculation with **VLEDMON_IN_SEL** = 0

$$V_{LED} = (ADC_{LEDM_DATA} * 0,000366 + 0,1) * 2 [V]$$

V_{LED} LED forward voltage

ADC_{LEDM_DATA} 12 bit LED monitor ADC voltage data

Equation 4 shows the indirect measurement of the LED forward voltage and its calculation with **VLEDMON_IN_SEL** register set to one.

Equation 4: LED voltage calculation with **VLEDMON_IN_SEL** = 1

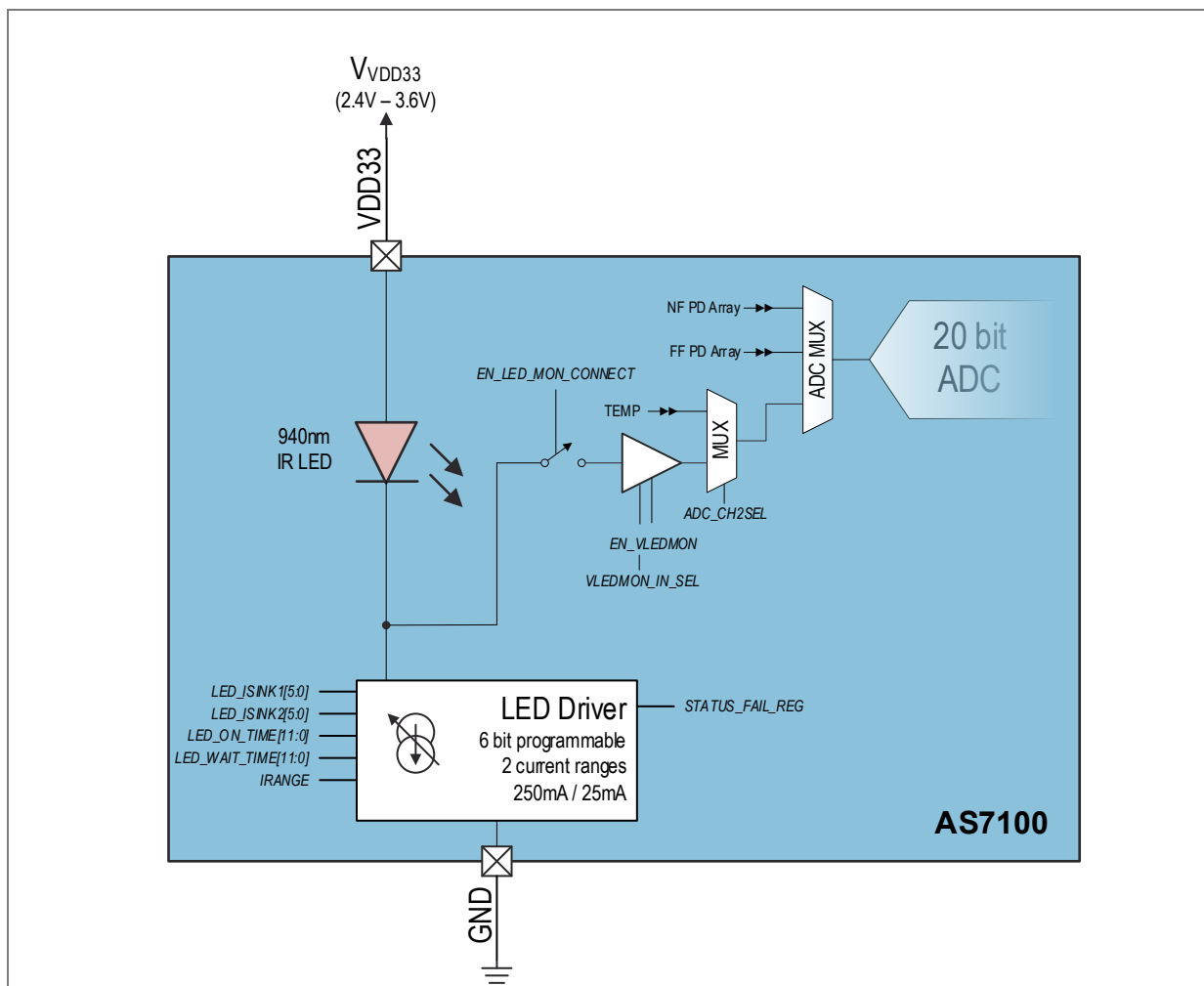
$$V_{LED} = V_{VDD33} - ((ADC_{LEDM_DATA} * 0,000366 + 0,1) * 2) [V]$$

V_{LED} LED forward voltage

ADC_{LEDM_DATA} 12 bit LED monitor ADC voltage data

In addition to the voltage monitoring function there is also an undervoltage detection available which can release an interrupt in case an LED driver undervoltage event occurs. In such case the **STATUS_FAIL_REG** flag is set automatically. The bit is also linked to an interrupt which can be enabled with the **IRQ_EN_MISC** interrupt enable register.

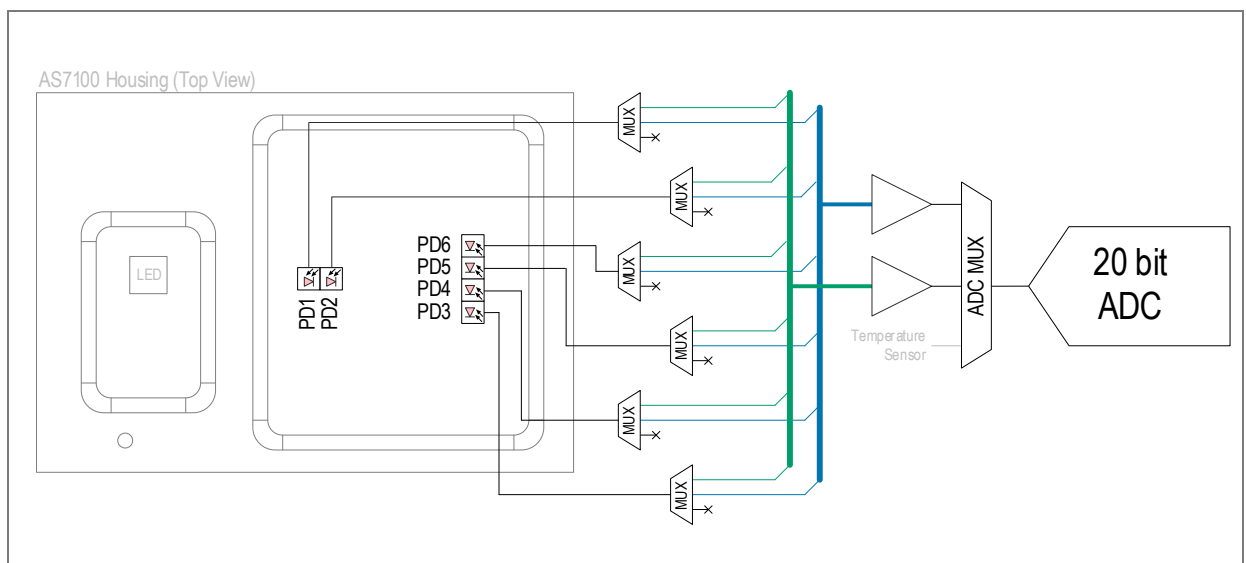
Figure 20: Integrated LED with LED driver circuit



8.4 On-chip photodiodes

AS7100 has in total 6 on-chip photodiodes which can be used for proximity detection measurements and optical force sensing applications. All six photodiodes are covered with an on-chip infrared filter to increase robustness against ambient light conditions. Each of the photodiodes can be connected to any of the two ADC input channels for highest flexibility with regards to optical integration. The photodiodes are automatically connected to the two input amplifiers for both subsamples based on the configuration register settings of **PDSEL_MOD1_SUB1**, **PDSEL_MOD1_SUB2**, **PDSEL_MOD2_SUB1** and **PDSEL_MOD2_SUB2**. Please refer to chapter 8.8 for more information regarding the measurement sequences and its related subsamples for proximity and optical force measurements. The physical location of the six photodiodes as well as a simplified block diagram of the input structure and multiplexers connected to the ADC is shown in Figure 21.

Figure 21: On-chip photodiodes with input multiplexer



Information:

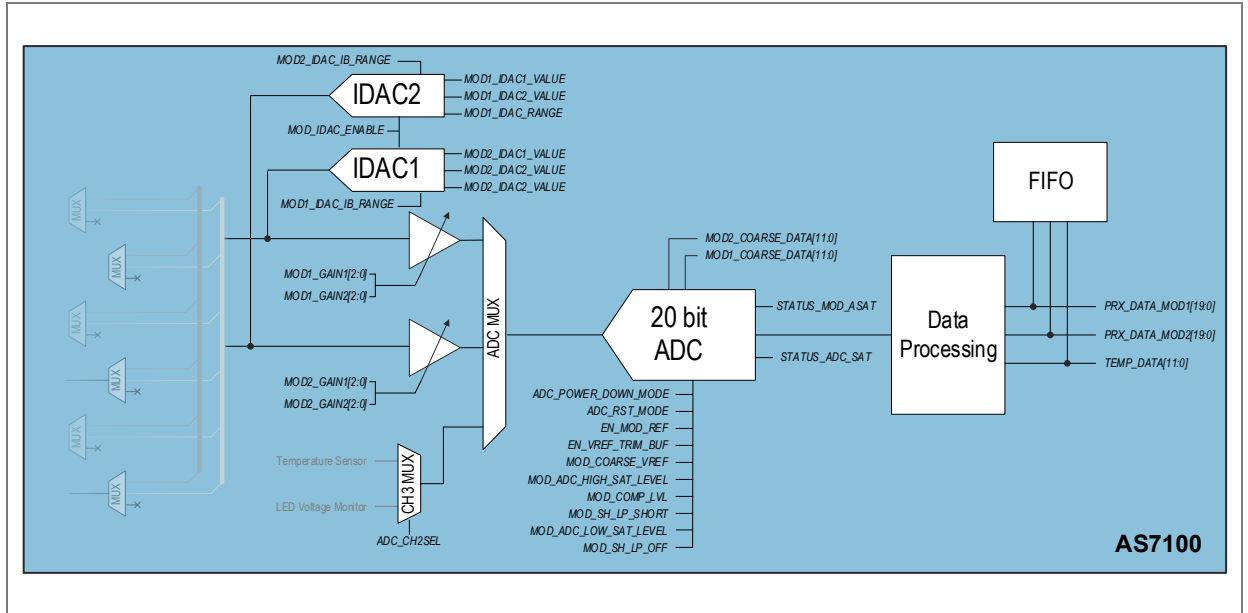
PD6 supports different filter characteristics resulting in lower sensitivity compared to PD1 – PD5.

8.5 Analog to digital converter

The AS7100 features a single ADC converter which performs in a sequential and predefined measurement order, based on the selected sample rate, up to three measurements. The first two measurements in the sequence are photodiode measurements for proximity and optical force detection where all six photodiodes can be assigned freely to one of the two preamplifiers like it is shown in Figure 21. The preamplifier allows for different gain configuration to match the application requirements. Since the device supports an automatic sequencer to organize the measurements (please refer to chapter 8.8 for details) it is possible to assign for each subsample an individual gain setting via register **MOD1_GAIN1** and **MOD2_GAIN1** for subsample number one and **MOD1_GAIN2** and **MOD2_GAIN2** for subsample number two. The third measurement in the automatic ADC measurement sequence is in default configuration the on-chip temperature measurement which is connected via CH3_MUX input multiplexer to the ADC. The device supports also the option to reconfigure the on-chip temperature measurement to a compliance voltage measurement to monitor the LED driver current sink voltage via **ADC_CH2SEL** register. Please refer to chapter 8.3 and Figure 22 for more details to the LED driver voltage measurement. The 20-bit ADC has various configuration registers which are also shown in Figure 21, however for the configuration depending on different use case the ams OSRAM support team can provide reference configuration parameters for the ADC configuration.

In addition to all configuration registers there are also interrupt status registers available which can help to detect saturation of the ADC. It is crucial for a consistent data generation that any saturation indicated by **STATUS_MOD_ASAT** and **STATUS_ADC_SAT** registers is avoided. Saturation can lead to ADC instability and inconsistent data generation. In case saturation occurs during operation it is recommended that affected data is discarded. In order to avoid ADC saturation analog gain (**MOD1_GAINx**, **MOD2_GAINx**) and/or t_{sample} time must be reduced. Host notification via an interrupt is supported and must be enabled via **IRQ_EN_SAT** register.

Figure 22: Analog to digital converter simplified block diagram

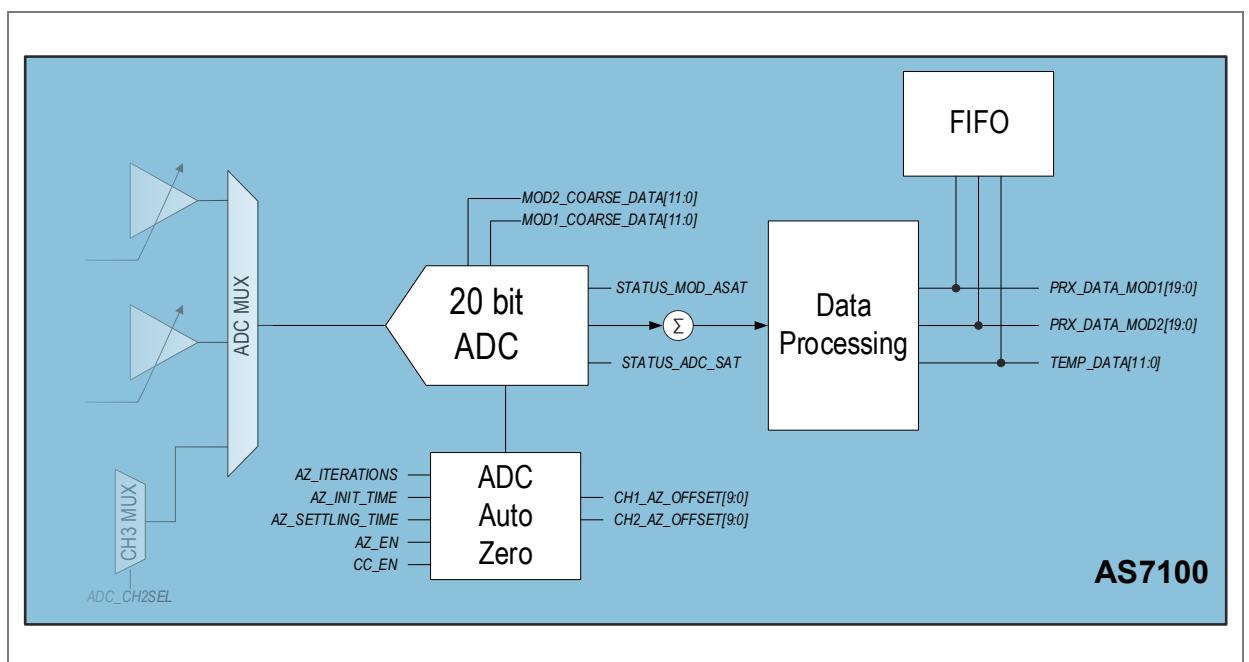


The ADC output data is feed to the data processing block where crosstalk is compensated and additional data manipulation can be configured. Furthermore, data is distributed to the proximity detection function blocks while in parallel the data is also written to the build in FIFO memory. Please refer to chapter 8.6 Data processing for a more detailed explanation. In order to enable also measurements without the utilization of the on-chip FIFO memory the ADC measurement results for proximity and temperature measurements can also be read out via register **PRX_DATA_MOD1**, **PRX_DATA_MOD2** and **TEMP_DATA** register.

8.5.1 Auto zero function

AS7100 analog to digital converters do support an automatic offset compensation feature. The function helps to reduce electrical offset voltages on the ADC measurement channels which would result in a shift of the ADC baseline counts. The auto zero block, like it is shown in Figure 23, features control registers to enable the autozero function as well as control initialization times, averaging function and a settling time.

Figure 23: ADC with auto zero block



The autozero function can be enabled with the two register bits **AZ_EN** and **CC_EN** along with the start of the measurement sequencer start bit **START**. Once the measurement sequencer is started and the auto zero function is enabled there is an initialization time t_{AZ_INIT} which is started in case the **AZ_INIT_TIME** register is set greater than zero like it is shown in the simplified timing diagram at Figure 24. The initialization time can be calculated with Equation 1.

Equation 5: Autozero initialization time t_{AZ_INIT}

$$t_{AZ_INIT} = AZ_INIT_TIME * \frac{1}{700000} [s]$$

t_{STBY_WAKEUP} Auto zero initialization time

AZ_INIT_TIME Control register to configure initialization time

Once the initialization time has finished the actual on chip autozero process is started. The duration of this process depends on the offset voltage which needs to be compensated and therefore varies. However, the time is limited to a maximum time t_{AZ_MAX} which is 65 times the configured autozero settling $t_{AZ_SETTLING}$ time which can be configured via **AZ_SETTLING_TIME** register.

Equation 6: Autozero settling time $t_{AZ_SETTLING}$

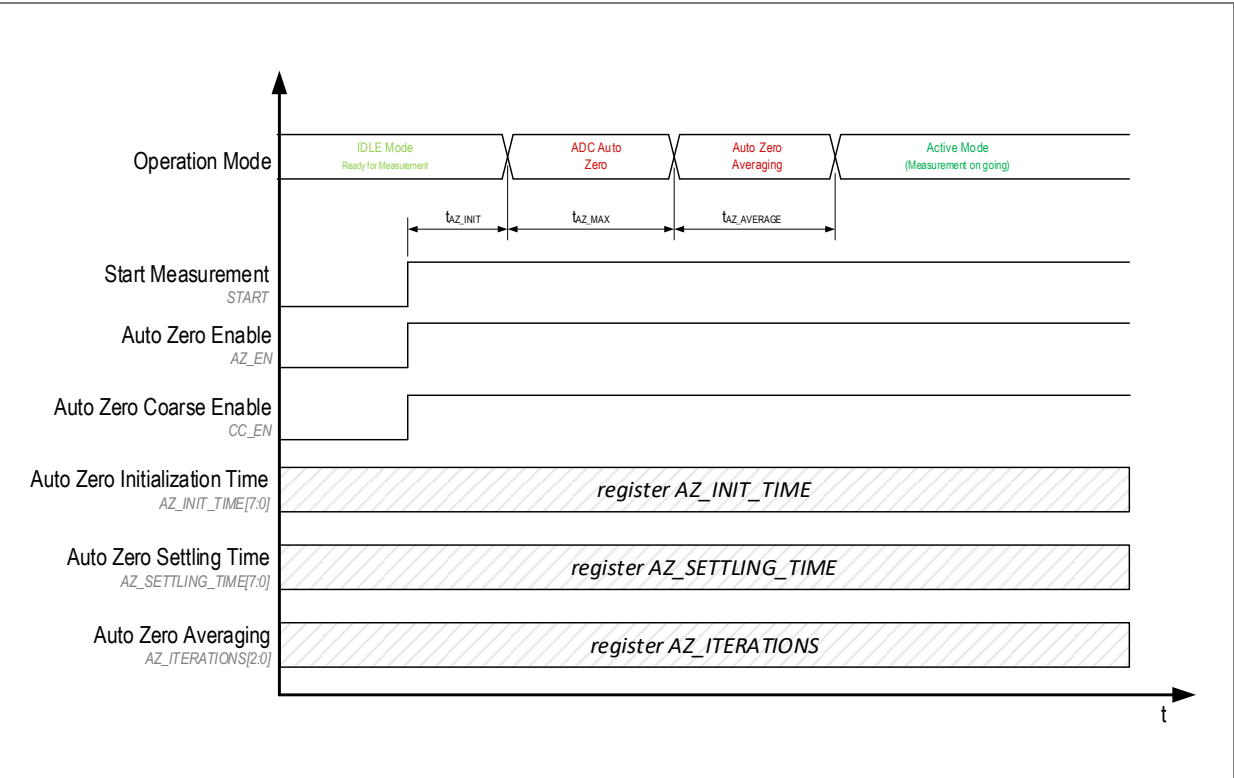
$$t_{AZ_SETTLING} = AZ_SETTLING_TIME * \frac{1}{700000} [s]$$

$t_{AZ_SETTLING}$ Auto zero settling time

$AZ_SETTLING_TIME$ Control register for autozero settling time

After completion of the autozero process there is an optional averaging function which can be enabled with **AZ_ITERATIONS** register.

Figure 24: Auto zero timing diagram



If the 3-bit control register is set to zero the averaging function is disabled. Once the register is set to greater zero an averaging factor up to 64 can be configured. Please refer to the register description of **AZ_ITERATIONS** register inside **AZ_CFG1** register for more detailed information concerning the auto zero averaging factor. The calculation of the auto zero averaging time $t_{AZ_AVERAGE}$ is shown in Equation 7.

Equation 7: Autozero averaging time

$$t_{AZ_AVERAGE} = AZ_AVERAGE_FACTOR * t_{AZ_SETTLING}[s]$$

t_{STBY_WAKEUP} Auto zero initialization time

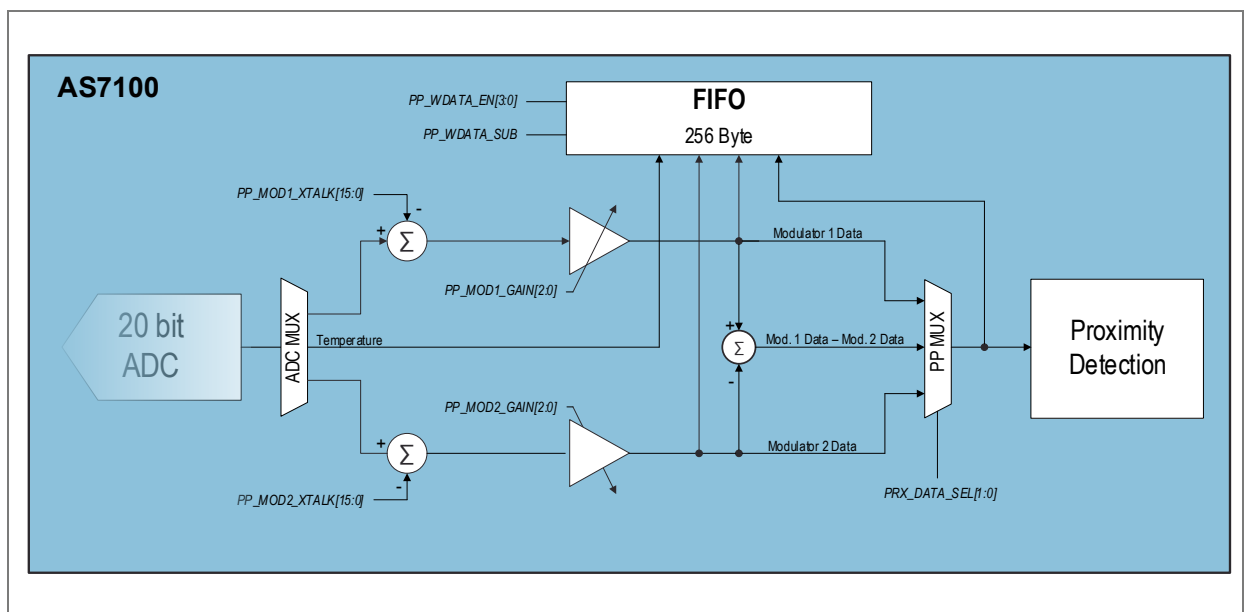
$AZ_AVERAGE_FACTOR$ AZ average factor configured in register $AZ_ITERATIONS$

Please mind that the autozero process, like it is shown in Figure 24, is only started once when the measurement sequencer is enabled. This happens when the **START** bit is set to one. While continuous measurements are ongoing there is no auto zero function activated. A new auto zero calibration is only started once the measurement sequencer is stopped, by clearing the **START** bit, and enabling the sequencer again by setting the **START** bit.

8.6 Data processing

The data processing block can be used for cross talk compensation via **PP_MOD1_XTALK** and **PP_MOD2_XTALK** for the two proximity measurement data channels. In addition to the cross talk data subtraction it is also possible to apply a digital gain with the three-bit registers **PP_MOD1_GAIN** and **PP_MOD2_GAIN** for both measurement channels independently. The modulator data outputs are then fed into the PP-MUX multiplexer in order to select the data which is used for the proximity detection block. Register **PRX_DATA_SEL** register allows to feed in modulator data 1 channel, modulator 2 channel and the difference between both modulator channels to enable a differential measurement. Besides the data preparation for the proximity detection the processed data is also stored to the FIFO memory. The selection which data is eventually stored at the FIFO can be configured with register **PP_WDATA_EN** register. There is also an option to store also the raw measurement data of the ADC rather than then processed measurement data by setting **PP_WDATA_SUB** bit.

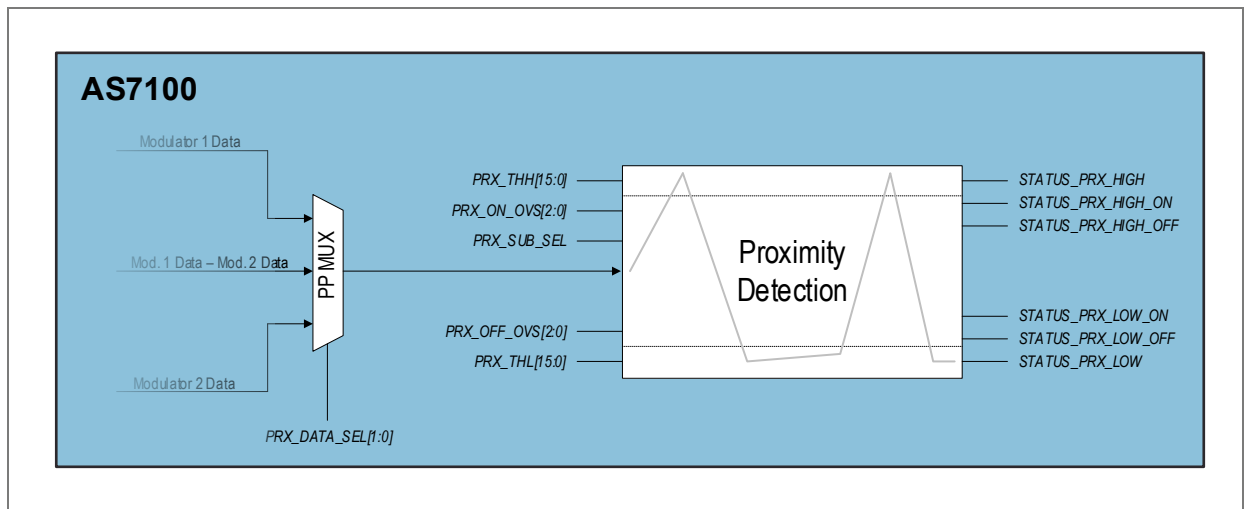
Figure 25: Data processing overview



8.7 Proximity detection

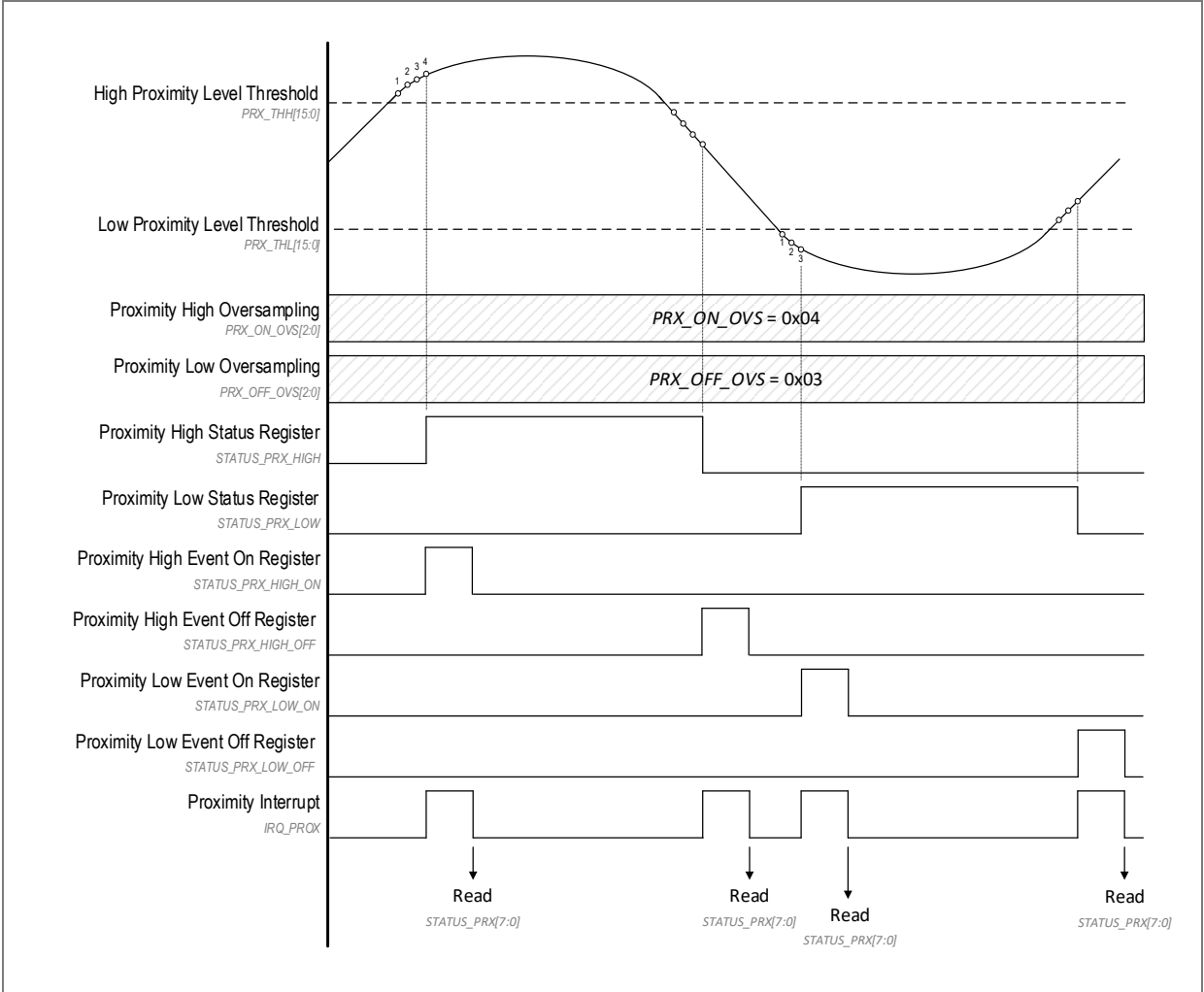
The proximity detection block is used to enable interrupt wakeup of host controlled to avoid continuous data readout of AS7100 measurement data. The block diagram shown in Figure 26 provides an overview of all proximity configuration registers. There are two threshold registers for proximity high level which is configured via **PRX_THH** register and the proximity low level with register **PRX_THL**. To select the correct measurement data which is configured with **PRX_DATA_SEL** register it is also mandatory to configure the correct sub sample with register **PRX_SUB_SEL**. An oversampling filter function to avoid false event detection can also be enabled for the high and low threshold via register **PRX_ON_OVS** and **PRX_OFF_OVS**.

Figure 26: Proximity detection block diagram



The proximity status registers indicate if the ADC input signal exceeds the configured high threshold via **STATUS_PRX_HIGH** registers. Two additional status bit **STATUS_PRX_HIGH_ON** and **STATUS_PRX_HIGH_OFF** allow to distinguish if a rising or falling edge was detected in order to be able to predict the proximity signal. Same status registers are available for the lower threshold with **STATUS_PRX_LOW** register if the ADC value drops below the value configured in **PRX_THL** register with the option to detect a rising for falling edge with **STATUS_PRX_LOW_ON** and **STATUS_PRX_LOW_OFF** registers. All the status registers provide interrupt functionality and can be enabled via **IRQ_EN_PRX** register to avoid polling of the registers. Please refer to Figure 27 for a detailed timing diagram of all proximity related status and interrupt registers.

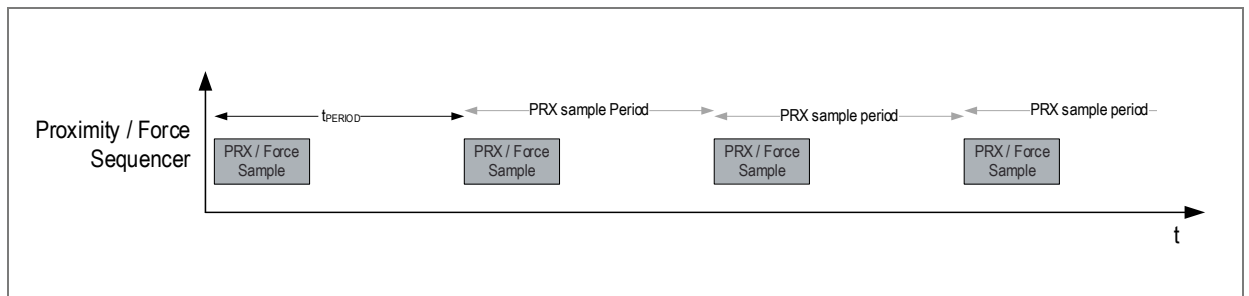
Figure 27: Proximity detection timing diagram



8.8 Measurement sequencer

In order to unload MCU with re-occurring measurement tasks to be triggered and its related timing constraints, AS7100 has a built-in measurement sequencer which controls all relevant proximity blocks which are necessary for a measurement together with its corresponding timings. An overview of the sequencer timing diagram is shown in Figure 28.

Figure 28: Proximity / force sequencer timing diagram



The timing diagram shows the proximity and force measurement samples which are controlled with the on-chip sequencer. The sample period can be configured with the **PRX_PERIOD** register. The proximity sample period t_{PERIOD} can be calculated with the calculation shown in Equation 8.

Equation 8: Proximity measurement period time

$$t_{\text{PERIOD}} = \text{PRX_PERIOD} * \frac{1}{700000} [\text{s}]$$

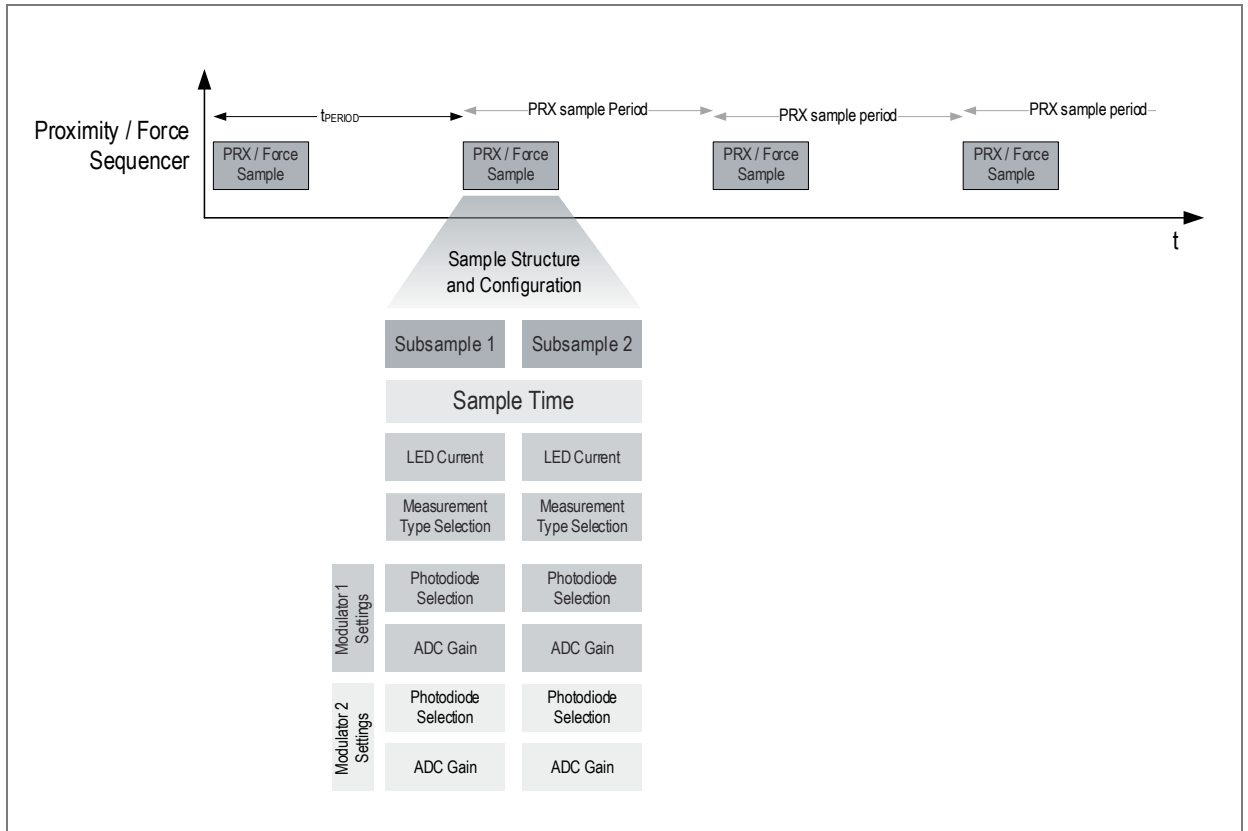
t_{PERIOD} ... Proximity and optical force measurement sample period time

PRX_PERIOD ... Register to control PRX sample period

8.8.1 Proximity / force sample structure

The AS7100 offers high flexibility in programming all the different combinations of the photodiodes. The sequencer divides a measurement into measurement samples according to the programmed sample period time t_{PERIOD} like it is shown in Figure 28. Each measurement sample can contain up to two subsamples, which allow for individual configuration. Subsample one can for example be used for a proximity measurement and subsample two can be reconfigured with its parameters for an optical force measurement. An overview of the configuration options for the two subsamples is shown in Figure 29. There are general settings which affect both subsamples like the LED current for each subsample which can be configured in register **LED_ISINK1** for subsample number 1 and register **LED_ISINK2** for subsample number two. The sample time, which is basically the active measurement time, can be configured via register **SAMPLE_TIME** register and affects both subsamples. Please refer to chapter Measurement types for a more detailed timing diagram of the actual proximity measurement which includes also the measurement sample time. There might also be applications and use cases for AS7100 where there is no need for a second measurement cycle and therefore it is possible to disable subsample 2 in the measurement cycle via register **PRX_SUB_COUNT**. On top of the generic settings there are also specific settings which do allow for further measurement customization of the Modulator 1 and Modulator 2 measurement. It is possible to assign different on-chip photodiodes for ADC Modulator 1 measurement and ADC Modulator 2 measurement for each of the two subsamples. The related software registers are **PDSEL_MOD1_SUB1**, **PDSEL_MOD1_SUB2**, **PDSEL_MOD2_SUB1** and **PDSEL_MOD2_SUB2**. Besides the photodiode selection it is also possible to adjust the ADC gain for each modulator cycle and subsample via register **MOD1_GAIN1** and **MOD2_GAIN1** for subsample number one and **MOD1_GAIN2** and **MOD2_GAIN2** for subsample number two. Since AS7100 supports besides the proximity and force measurement also conventional ambient light measurements it is possible to configure the measurement type for each subsample as well via register **NON_PRX_MEASURE_ON**. Please refer to chapter 8.8.2 for more detailed information regarding the measurement types.

Figure 29: Proximity / force sample structure and configuration options

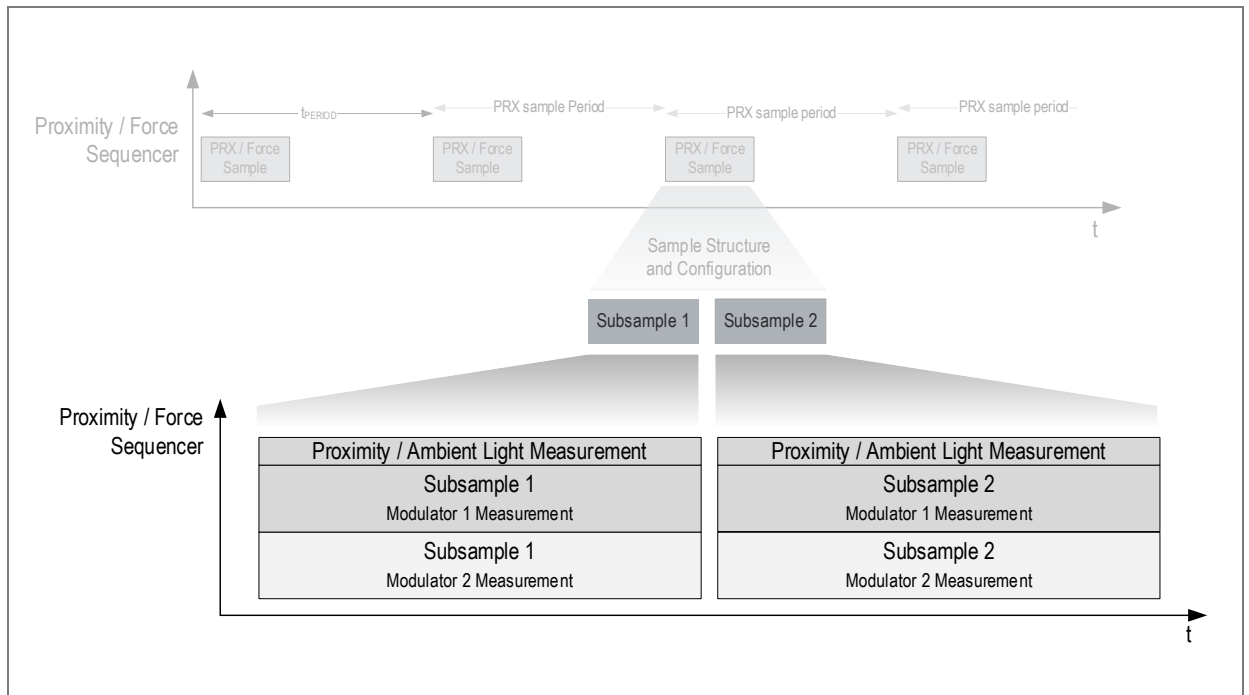


8.8.2 Measurement types

This chapter provides an overview of the available measurement types within a subsample which can be selected and controlled with different registers. There are basically two types of measurements available. The first one is a proximity measurement which can also be used for optical force measurement with different device configuration to match the force measurement requirements. The second supported measurement mode is an ambient light measurement which can also be assigned to one of the two subsamples with register

NON_PRX_MEASURE_ON register. The measurement sequence is hard coded in a state machine to match all timings and is therefore fixed. However, there is still the option to disable measurements as well as subsample two in the sequence which are not necessary in an application. The simplified timing diagram of the measurement sequence where all detailed timing diagrams are based on is shown in Figure 30.

Figure 30: Subsample measurement sequence ($prx_sub_count = 1$; $mod_channel_disable = 0$; $temp_channel_disable = 0$)



The second subsample can be disabled with register **PRX_SUB_COUNT** register. By clearing the bit, the second subsample is disabled in the measurement sequence. The temperature measurement for both subsamples can be disabled with register **TEMP_CHANNEL_DISABLE** register. The modulator one and modulator two measurement can be disabled for both subsamples with register **MOD_CHANNEL_DISABLE**.

8.8.2.1 Proximity measurement without LED pre-phase

The timing diagram of a proximity measurement without wait time between samples is shown in Figure 31. The measurement is divided into different measurement phases which are LED on phase and two times LED off phase. Each of the measurement phases is based on a configurable t_{sample} time base which can be controlled via register **SAMPLE_TIME**. The sample time t_{SAMPLE} can be calculated with Equation 9.

Equation 9: Proximity measurement sample period

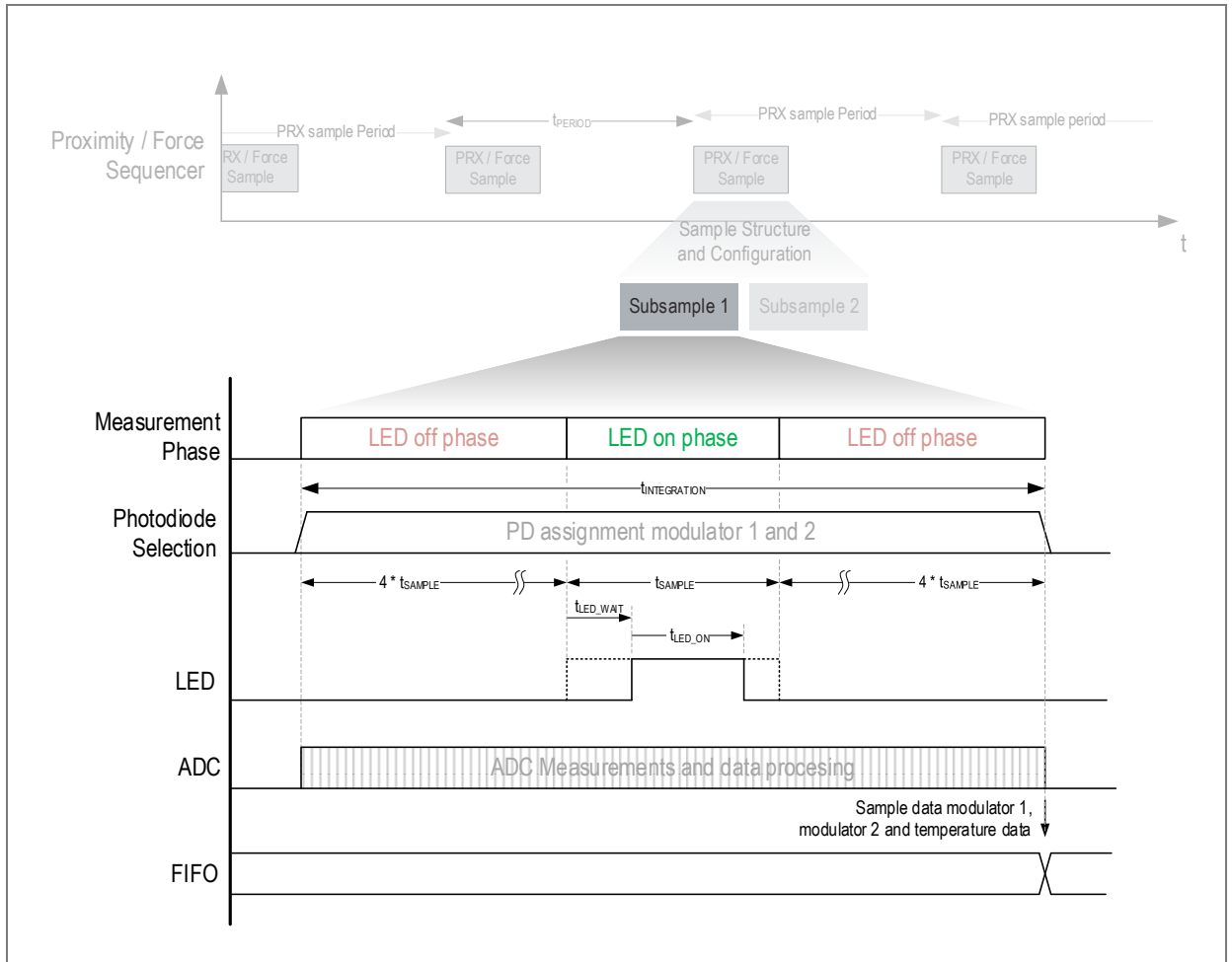
$$t_{SAMPLE} = (SAMPLE_TIME + 1) * \frac{1}{700000} [s]$$

t_{SAMPLE} ... Sample period as basis for all measurement phases

$SAMPLE_TIME$... Register to control sample period

In order to avoid thermal overload of the integrated infrared LED a maximum LED on time of 20% must be guaranteed. Therefore, the LED off phase sample time is a factor 8 higher than the LED on phase like it is also shown in Figure 31.

Figure 31: Proximity subsample timing diagram without pre- and post LED phase
($mod_channel_disable = 0$; $prx_measure_mod = 0$)



There is the option to configure within the LED on measurement phase a LED wait time t_{LED_WAIT} via register **LED_WAIT_TIME** which allows to further delay the LED off phase. If the register is set to zero the LED is switched on right at the start of the LED on measurement phase. The wait time can be calculated with the formula shown in Equation 10.

Equation 10: LED wait time t_{LED_WAIT}

$$t_{LED_WAIT} = LED_WAIT_TIME * \frac{1}{700000} [s]$$

$t_{WAIT_TIME_ON}$ LED wait time within the LED on measurement phase

LED_WAIT_TIME Register to control LED wait time within LED on measurement phase

There is a second LED timing register **LED_ON_TIME** which allows to shorten the LED pulse within the LED on phase. This register defines how long the LED is enabled after the configured LED wait time t_{LED_WAIT} has elapsed. In case it is not desired to shorten the LED pulse it is recommended to program the **LED_ON_TIME** register to its maximum value. The LED pulse is in this case not extended beyond the LED on measurement phase. It will always be switched off at the end of the LED on measurement phase by its internal state machine.

Equation 11: LED on time t_{LED_ON}

$$t_{LED_ON} = LED_ON_TIME * \frac{1}{700000} [s]$$

t_{LED_ON} LED on time within the LED on measurement phase

LED_ON_TIME Register to control LED on time within LED on measurement phase

The total integration time $t_{INTEGRATION}$ of a subsample can be calculated with Equation 12. The equation includes already the processing option of averaging multiple measurement samples which is controlled with **PRX_SAMPE_COUNT1** register for subsample one and **PRX_SAMPLE_COUNT2** register for subsample two. A simplified timing diagram which shows the proximity sampling averaging function is shown in Figure 32.

Equation 12: Integration time $t_{INTEGRATION}$

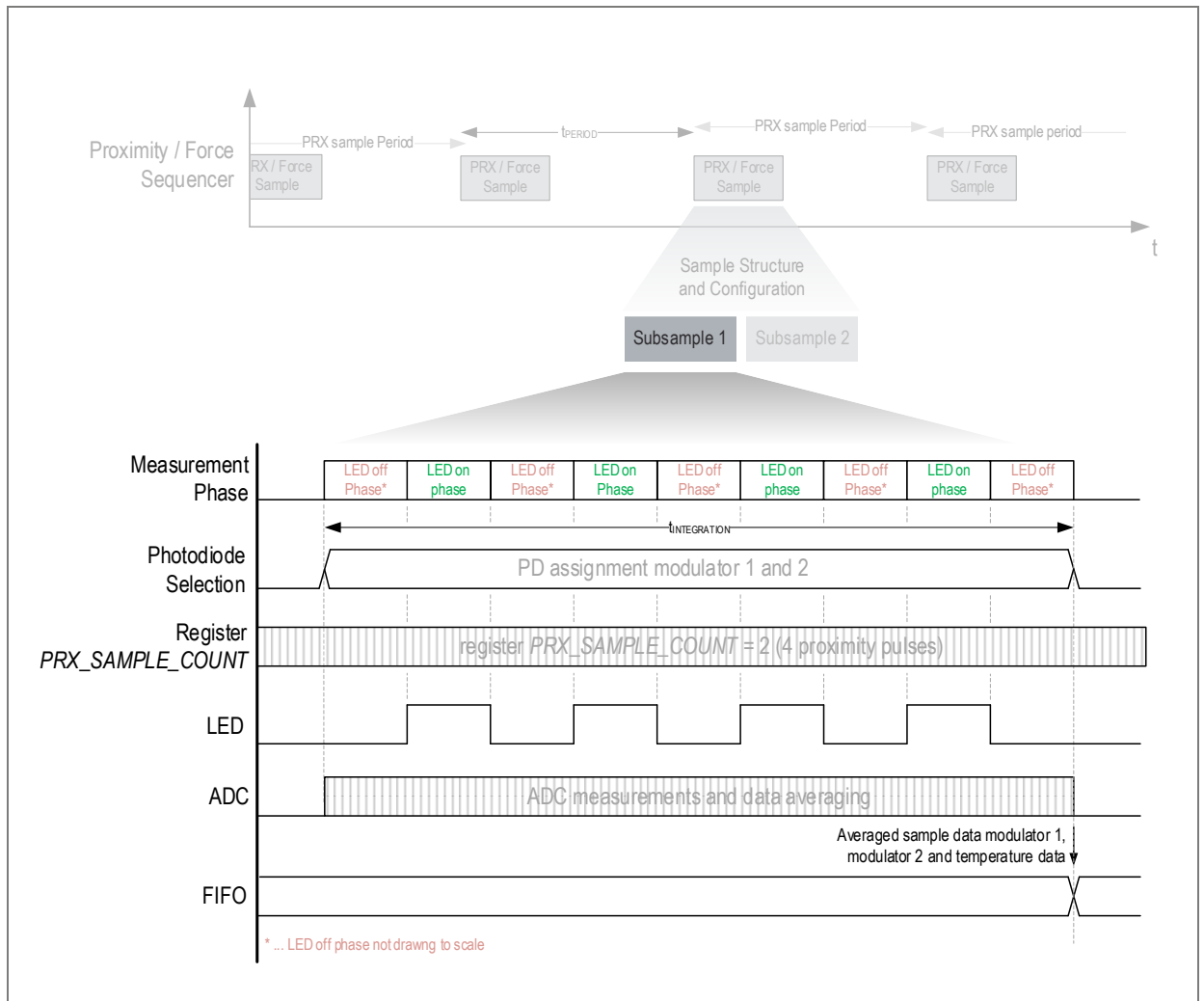
$$t_{INTEGRATION} = ((2^{PRX_SAMPLE_COUNTx} * 5) + 4) * t_{SAMPLE} [s]$$

$t_{INTEGRATION}$ Total measurement time including all measurment phases

t_{SAMPLE} Sample period as basis for all measurement phases

PRX_SAMPLE_COUNTx Control Register for sample averaging

Figure 32: Proximity subsample timing diagram with averaging ($mod_channel_disable = 0$; $prx_measure_mod = 0$; $prx_sample_count1 = 2$)



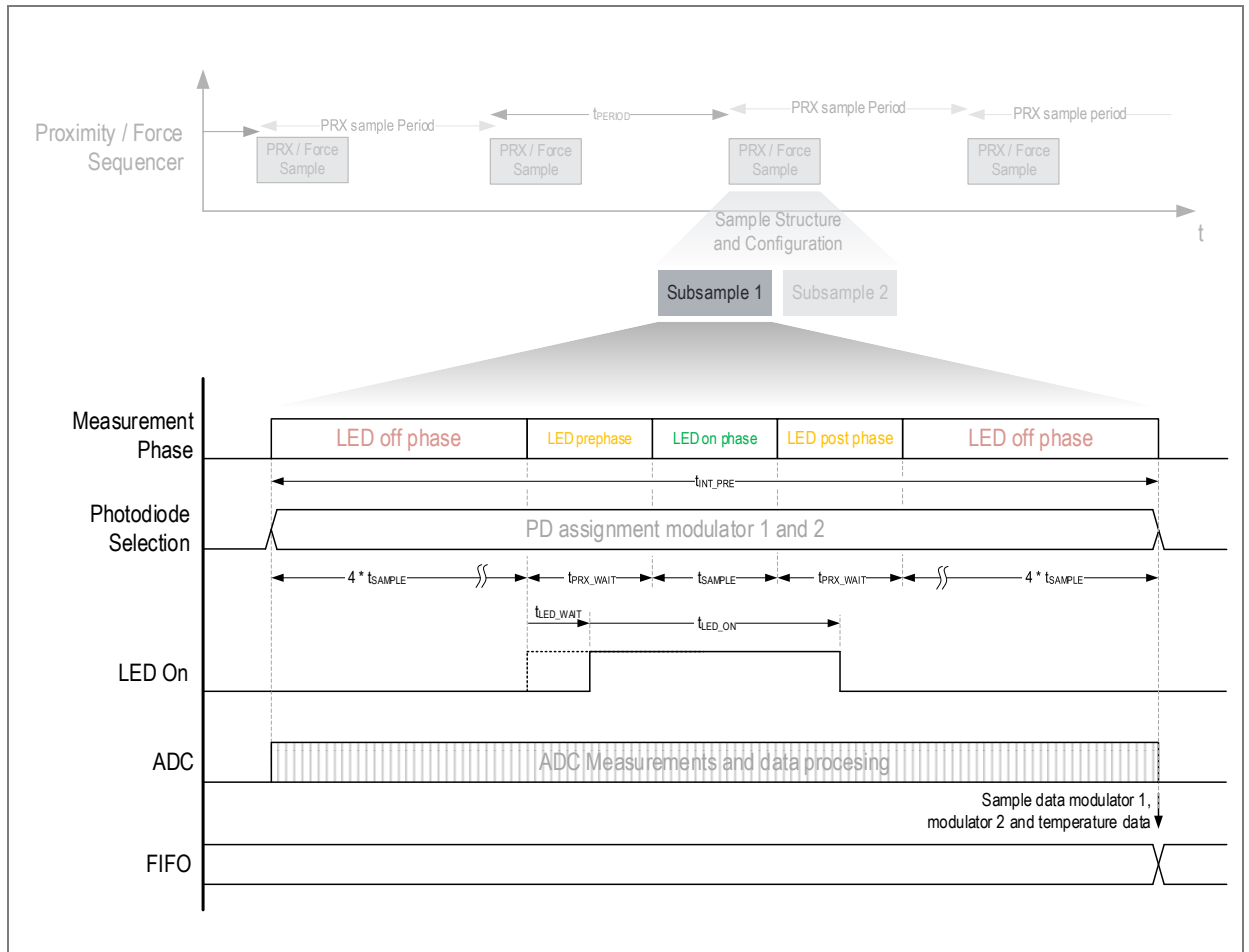
8.8.2.2 Proximity measurement with LED pre-phase

AS7100 supports a second measurement mode which introduces a pre and a post phase to the LED on phase which can be used to have the LED current already settled for the LED on ADC measurement phase. This operation mode can be enabled with register

PRX_MEAS_MODE for both subsamples. The control of the LED wait time t_{LED_WAIT} is implemented with the same control register **LED_WAIT_TIME** like we have it in the proximity measurement without LED pre-phase described in the previous chapter 8.8.2.1.

Please refer to Equation 10 for calculation of the LED wait time. The LED on time t_{LED_ON} is controlled with **LED_ON_TIME** register and can be calculated with Equation 11 which can be found in previous chapter 8.8.2.1.

Figure 33: Proximity subsample timing diagram with LED pre-phase



Important to mention for the LED on time is that even if the time is programmed to a value which would exceed the LED on measurement phase the LED is always switched off at the end of the LED on phase like it is shown in the timing diagram in Figure 33. The time for the newly introduced Led pre-phase and LED wait phase between the subsamples t_{PRX_WAIT} can be controlled with register **PRX_WAIT_TIME** and calculated with Equation 13. The control of the sample time t_{SAMPLE} is also the same and has not changed for this operation mode with register **SAMPLE_TIME** and calculation is done with Equation 9.

Equation 13: LED pre-phase wait time t_{PRX_WAIT}

$$t_{PRX_WAIT} = PRX_WAIT_TIME * \frac{1}{700000} [s]$$

t_{PRX_WAIT} Wait time between measurement samples

PRX_WAIT_TIME Register to control wait time between samples

The integration time t_{INT_PRE} can be calculated with Equation 14.

Equation 14: Integration time with LED pre-phase t_{INT_PRE}

$$t_{INT_PRE} = ((2^{PRX_SAMPLE_COUNTx} * 5) + 4) * t_{SAMPLE} + (2^{PRX_SAMPLE_COUNTx} + 1) * t_{PRX_WAIT} [s]$$

$t_{INTEGRATION}$ Total measurement time including all measurement phases

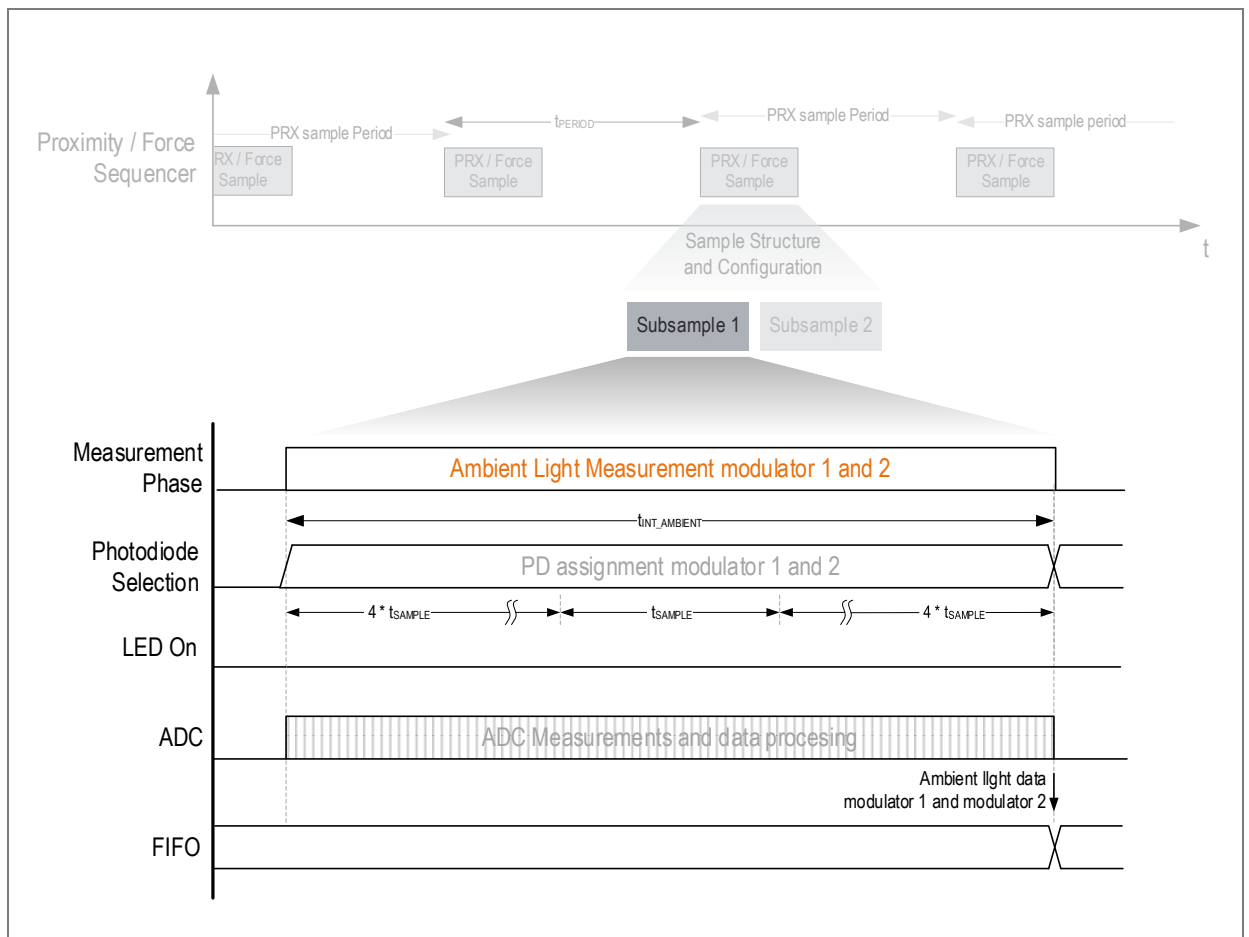
t_{SAMPLE} Sample period as basis for all measurement phases

PRX_SAMPLE_COUNTx Control Register for sample averaging

8.8.2.3 Ambient light measurement

The third measurement type which can be configured is an ambient light measurement mode. This measurement mode can be enabled with register **NON_PRX_MEASURE_ON** for each subsample separately. As soon as this mode is selected the IR LED is not switched on and the registers for controlling the LED current are ignored like it is shown in the timing diagram at Figure 34. Even if there is just one out of the two subsamples configured to ambient light measurement it is not necessary to clear the LED registers **LED_ISINK1** and **LED_ISINK2** for the ambient light measurement.

Figure 34: Ambient light measurement timing diagram



The calculation of the total measurement time $t_{INT_AMBIENT}$ is shown in Equation 15 which is based on the sample time t_{SAMPLE} which can be calculated with Equation 9.

Equation 15: Integration time $t_{INT_AMBIENT}$

$$t_{INTAMBIENT} = ((2^{PRX_SAMPLE_COUNTx} * 5) + 4) * t_{SAMPLE} [s]$$

$t_{INTAMBIENT}$ Total ambient light measurement time

t_{SAMPLE} Sample period as basis for all measurement phases

PRX_SAMPLE_COUNTx Control Register for sample averaging

8.9 Communication interfaces

8.9.1 EN pin

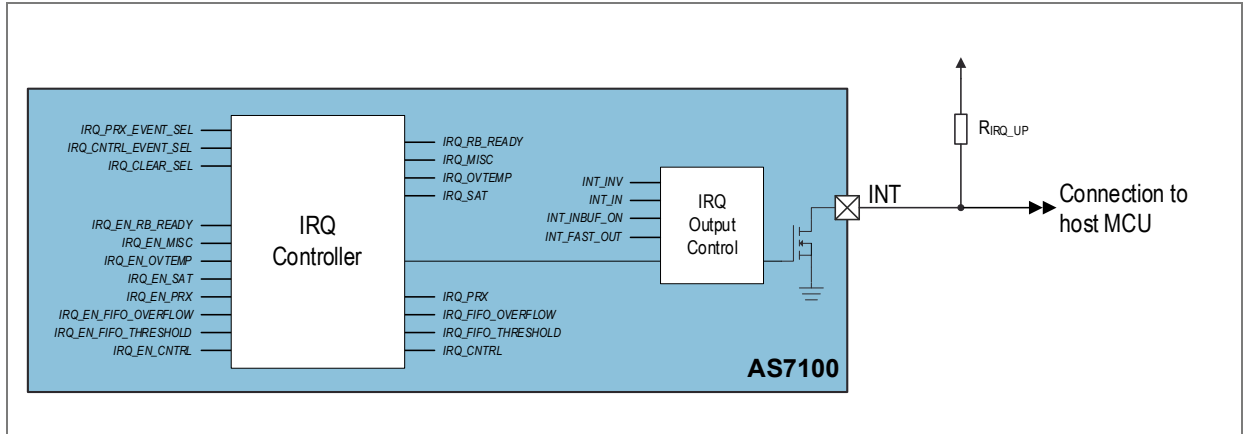
AS7100 features a dedicated enable pin for proper power down on the optical force sensor. The EN pin is active high which means too high signal on the EN input pin powers up the device. If the pin is driven low AS7100 is always forced to power down operation mode and current consumption is typically below 1µA. Please refer to Figure 19 for a detailed startup timing diagram of the EN pin.

8.9.2 Interrupt pin

In order to notify a host MCU about a proximity or force touch event the device supports a dedicated interrupt output pin. The pin is an open drain output which requires always an external pull up resistor R_{IRQ_PU} for proper operation. Its polarity can be changed from active low operation to active high operation with a control register **INT_INV**. The output driving strength of the integrated open drain transistor can be configured with the **INT_FAST_OUT** control bit to increase its strength by a factor of 4. It is also possible to read back to INT pin logic status via **INT_IN** register. Please mind that **INT_INBUF_ON** register needs to be set to enable read out of **INT_IN** register.

The different interrupt sources can be enabled with **IRQ_ENABLE** registers and its behavior is controlled with the **IRQ_CONTROL** register. Important for the interrupt control behavior is the **IRQ_CLEAR_SEL** control register. This register allows to change the interrupt reset behavior. If the bit is set to one it is mandatory to write a one to the released interrupt status register bit to clear the interrupt. If the bit is set to zero the interrupt gets cleared simply by reading out the interrupt status registers **STATUS**, **STATUS_PRX**, **STATUS_SAT**, **STATUS_CNTRL** or **STATUS_MISC**.

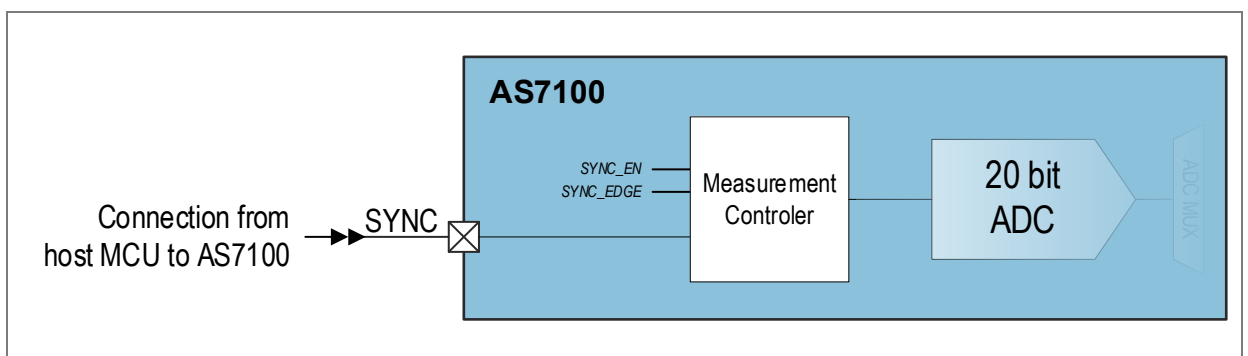
Figure 35: IRQ block diagram



8.9.3 SYNC pin

AS7100 supports the synchronization of the ambient light measurement or optical force measurement with a host MCU via a dedicated synchronization pin SYNC. Rather than using the internal periodical measurement timing which is derived from the on-chip oscillator, the measurement start can be triggered externally. The function is enabled with the control register **SYNC_EN**. Once the function is enabled it is also important that the SYNC input pin buffer is enabled via register **SYNC_INBUF_ON**. This is necessary to connect the SYNC pin signal to the internal measurement controller logic. There is also the option to configure the SYNC pin input pulse polarity via **SYNC_EDGE** register bit.

Figure 36: SYNC block diagram

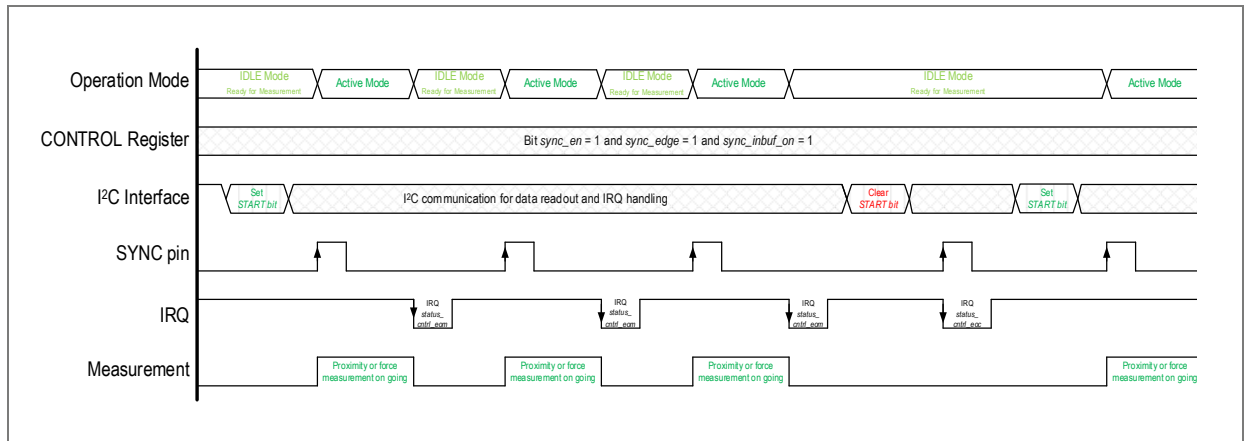


A simplified timing diagram how the SYNC input pin is used together with an external MCU is shown in Figure 37. In order to enable the external synchronization mode, it is necessary to set the **SYNC_EN** and **SYNC_INBUF_ON** bit to one.

Please mind that AS7100 needs to be in IDLE operation mode when these bits are configured. Next step is to set the **START** register to enable the measurement. Please mind that the measurement itself is not started yet.

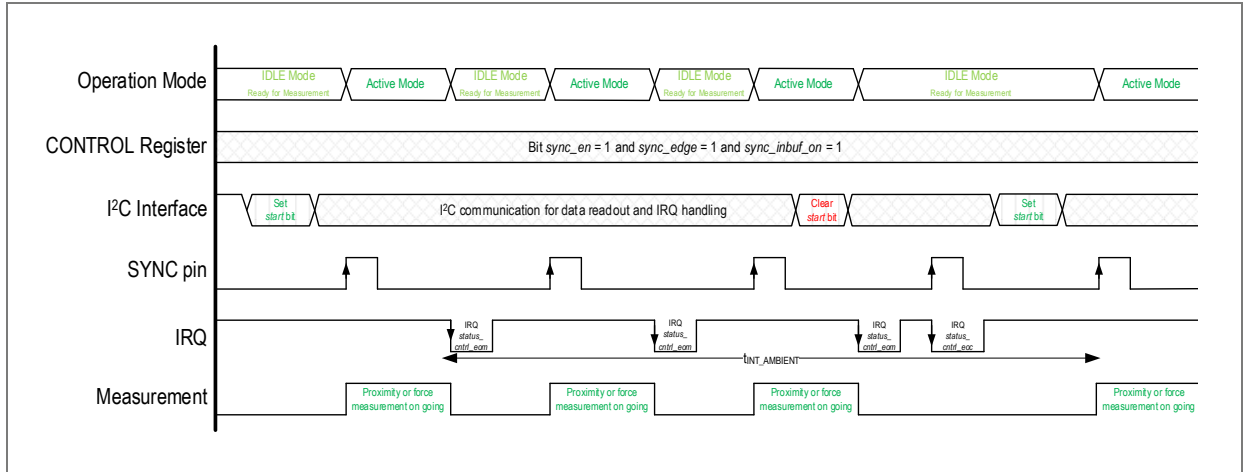
Once the SYNC pin detects a rising edge input signal a measurement is triggered and executed. The device enters automatically active operation mode and once the measurement is finished a **STATUS_CNTRL_EOM** interrupt is released. AS7100 enters right after the measurement IDLE operation mode waiting for the next input pulse on the SYNC input to trigger the next measurement. Please note that once the **START** bit is cleared by its host MCU any input pulse on the SYNC input pin is ignored and no new measurement is triggered like it is also illustrated in Figure 37.

Figure 37: SYNC input functional timing diagram



Please note that if the **START** bit is cleared in active mode while a measurement is ongoing the measurement is finished and a **STATUS_CNTRL_EOM** interrupt is released like it is shown in Figure 38. External synchronization pulses on the SYNC pin get ignored until the **START** bit is set again by the host MCU.

Figure 38: SYNC input functional timing diagram with *start* bit clear during ongoing measurement



8.9.3.1 SYNC delay

If in an application synchronization of multiple AS7100 devices is necessary there is an option to delay the start of a measurement when the measurement start is triggered with the SYNC pin. This feature can help to avoid devices interfering with each other. The delay $t_{\text{SYNC_DELAY}}$ can be controlled with **SYNC_DELAY_0** and **SYNC_DELAY_1** registers and its timing can be calculated with Equation 16.

Equation 16: SYNC delay time $t_{\text{SYNC_DELAY}}$

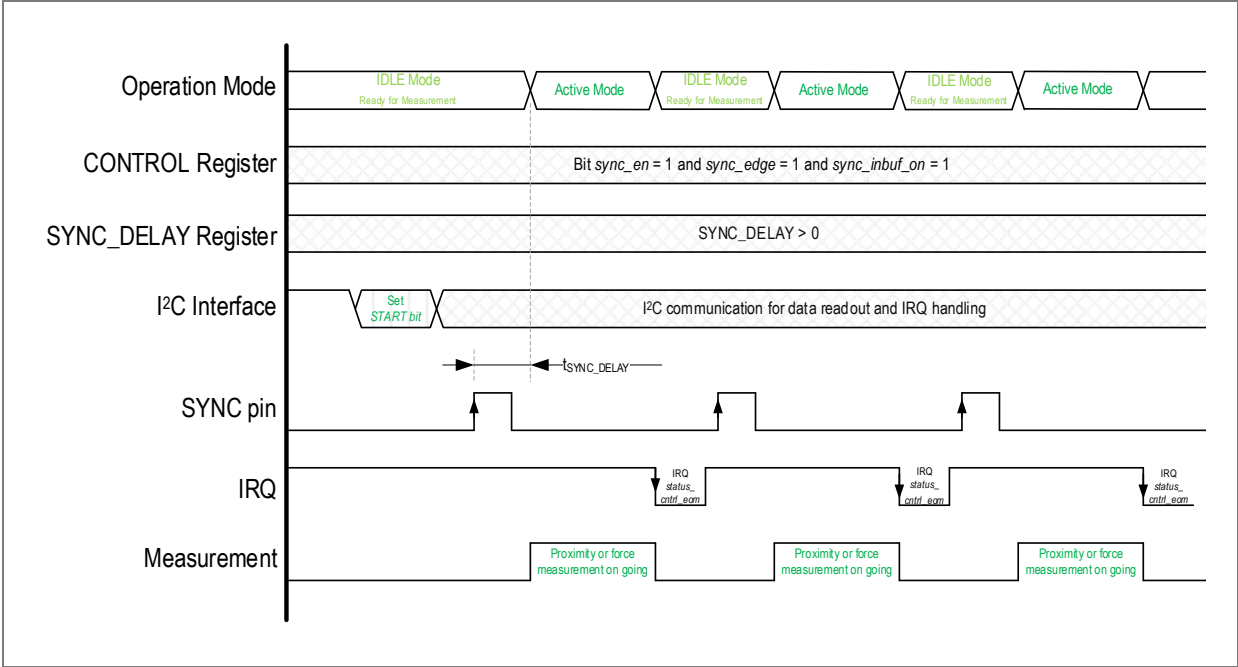
$$t_{\text{SYNC_DELAY}} = \text{SYNC_DELAY} * \frac{1}{700000} [\text{s}]$$

Where

$t_{\text{SYNC_DELAY}}$ SYNC input delay time to delay measurement start

PRX_WAIT_TIME Timing control register for SYNC delay function

Figure 39: SYNC input functional timing diagram with synchronization delay enabled



8.9.4 I²C interface

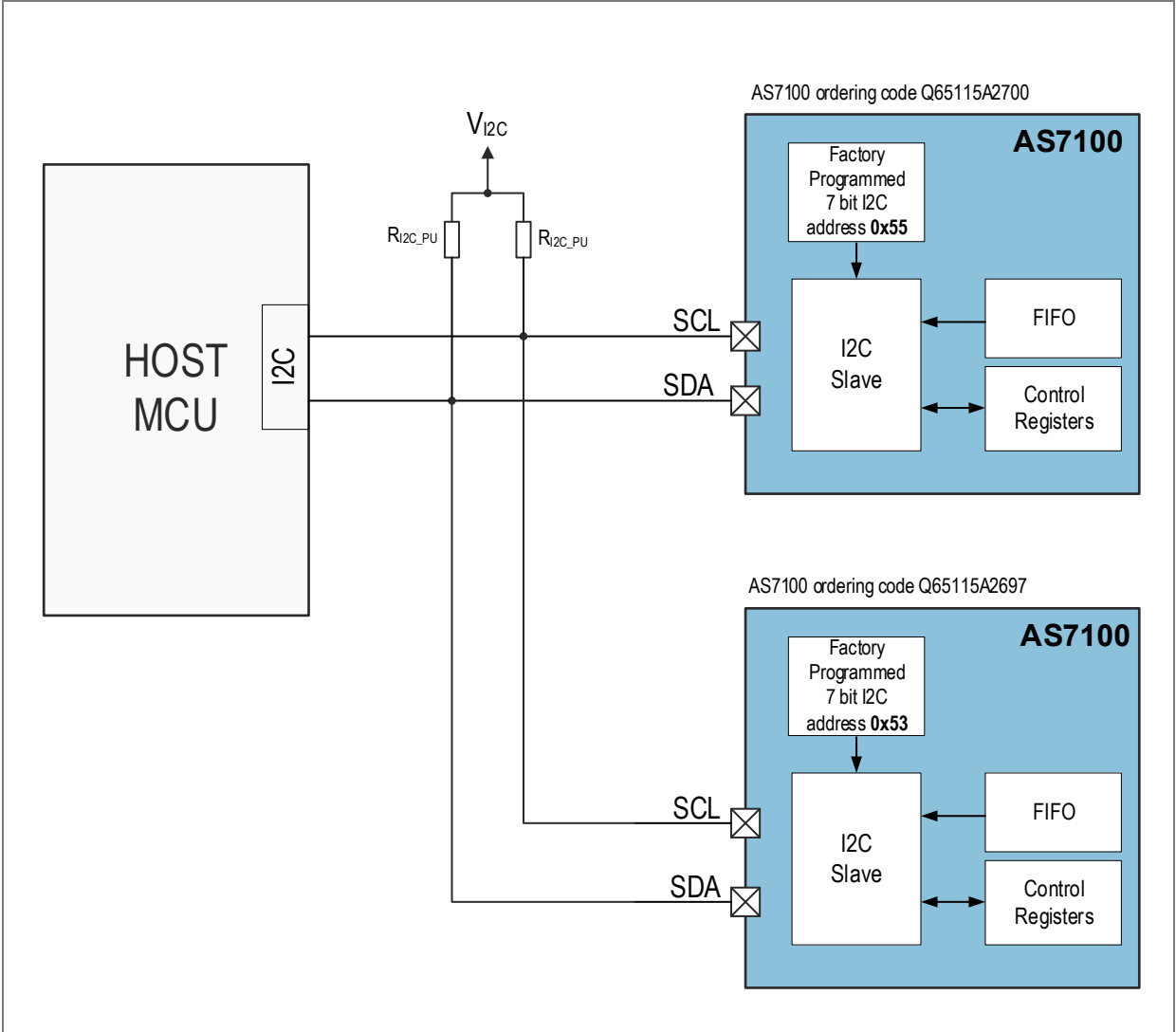
The AS7100 I²C slave uses an I²C Address of 0x55 (7-bit format; R/W bit has to be added) - AAh (8-bit format for writing) and ABh (8-bit format for reading) respectively. It expects external pull-up resistors R_{I2C_PU} on the SDA and SCL pins. The interface supports the following features:

- Fast Mode plus (1 MHz)
- Fast Mode (400 kHz)
- Standard Mode (100 kHz)
- 7+1-bit addressing mode
- Write formats
 - Single-Byte-Write
 - Burst-Write
- Read formats
 - Current-Address-Read
 - Random-Read
 - Sequential-Read
- IEEE standard requirements regarding filtering and timing are implemented.

8.9.4.1 Device address selection

The default 7-bit I²C device Address of AS7100 is 0x55. However, there is in certain applications a demand for multiple AS7100 devices on a single I²C bus master. In order to Address this requirement AS7100 can be ordered with an alternative 7-bit I²C slave addresses which is 0x53. A simplified system block diagram how two AS7100 are connected to a single I²C master is shown in Figure 40. In case more than two different I²C slave Address are need in an application please contact ams OSRAM customer service department.

Figure 40: I²C host connection with two AS7100 connected to a single I²C master



8.9.4.2 I²C protocol

Table 8 shows the symbols used in the coming mode descriptions.

Table 8: I²C symbol definition

Symbol	Definition	R/W	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start	R	1-bit
DW	Device Address for write	R	1010 1010b (AAh)
DR	Device Address for read	R	1010 1011b (ABh)
WA	Word Address	R	8-bit
A	Acknowledge	W	1-bit
N	No acknowledge	R	1-bit
reg_data	Register data/write	R	8-bit
Data (n)	Register data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Increment word Address internally	R	During acknowledge

8.9.4.3 I²C write access

Byte Write and Burst Write formats are used to write data to the slave.

Figure 41: I²C byte write format

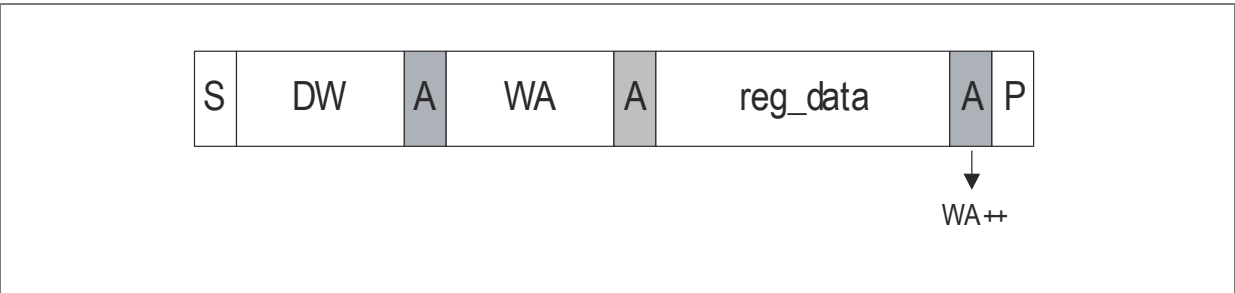
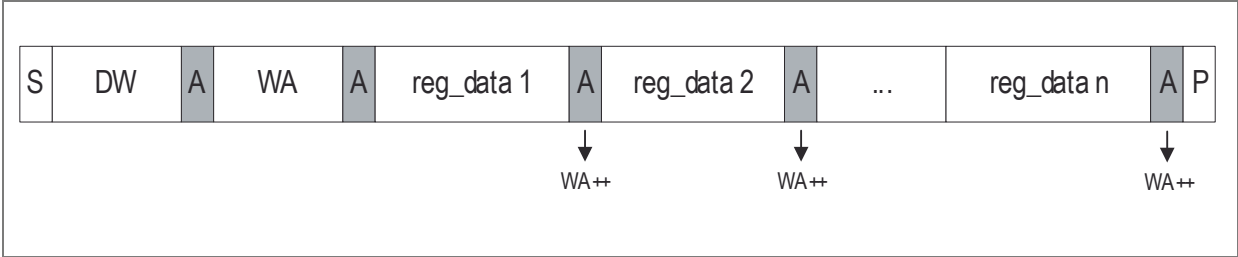


Figure 42: I²C burst write format

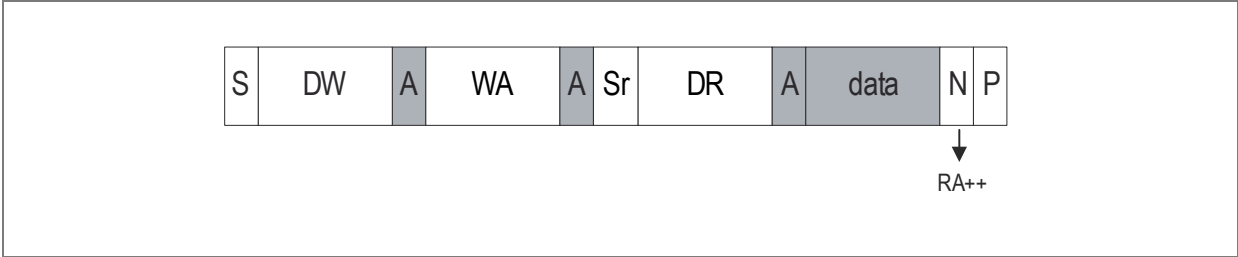


The transmission begins with the START condition, which is generated by the master when the bus is in an IDLE state (the bus is free). The device-write Address is followed by the word Address. After the word Address, any number of data bytes can be sent to the slave. The word Address is incremented internally to write subsequent data bytes on subsequent Address locations.

8.9.4.4 I²C read

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read Address or with a new transmission START followed by the device-read Address when the bus is in an IDLE state. The device-read Address is always followed by the first register byte transmitted from the slave. In Read mode, any number of subsequent register bytes can be read from the slave. The word Address is incremented internally.

Figure 43: I²C random read format

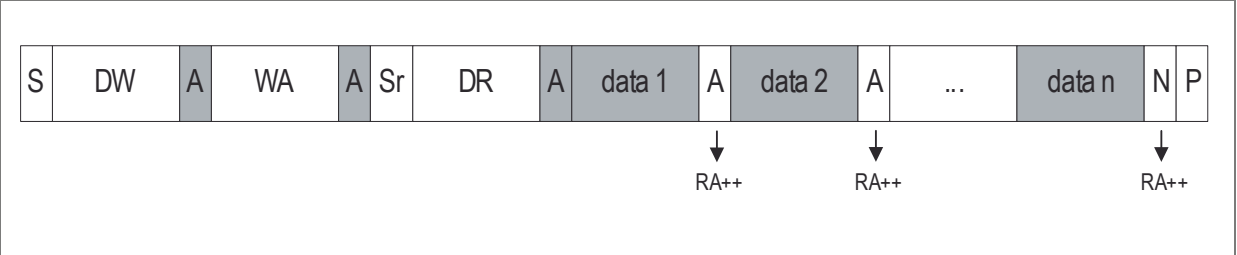


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word Address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write Address and the word Address.

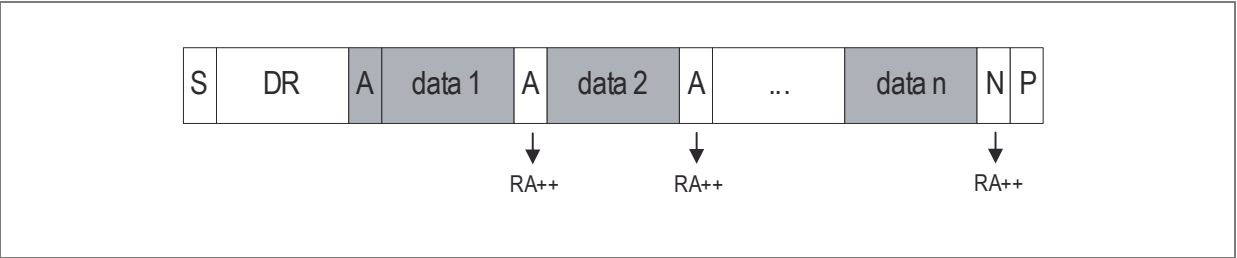
To change the data direction, a repeated START condition is issued on the first SCL pulse after the acknowledge bit of the word Address transfer. After the reception of the device-read Address, the slave becomes the transmitter. In this state, the slave transmits register data located by the previously received word Address vector. The master responds to the data byte with a “not-acknowledge” and issues a STOP condition on the bus.

Figure 44: I²C sequential read format



Sequential Read is the extended form of Random Read, as more than one register-data byte is subsequently transferred. In contrast to the Random Read, an acknowledge from the master is the response for the transferred register-data bytes for a sequential read. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-Address counter). To terminate the transmission, the master must send a “not-acknowledge” following the last data byte and subsequently generate the STOP condition.

Figure 45: I²C current address read format



To keep the access time as small as possible, this format allows read access without the word Address transfer in advance of the data transfer. The bus is idle, and the master issues a START condition, followed by the Device-Read Address. Analogous to Random Read, a single byte transfer is terminated with a “not-acknowledge” after the first register byte. Analogous to Sequential Read, an unlimited number of data bytes can be transferred – where an acknowledge from the master must be the response to the data bytes. For termination of the transmission, the master sends a “not-acknowledge” following the last data byte and a subsequent STOP condition.

8.9.4.5 Timing parameter

Figure 46: I²C timing diagram

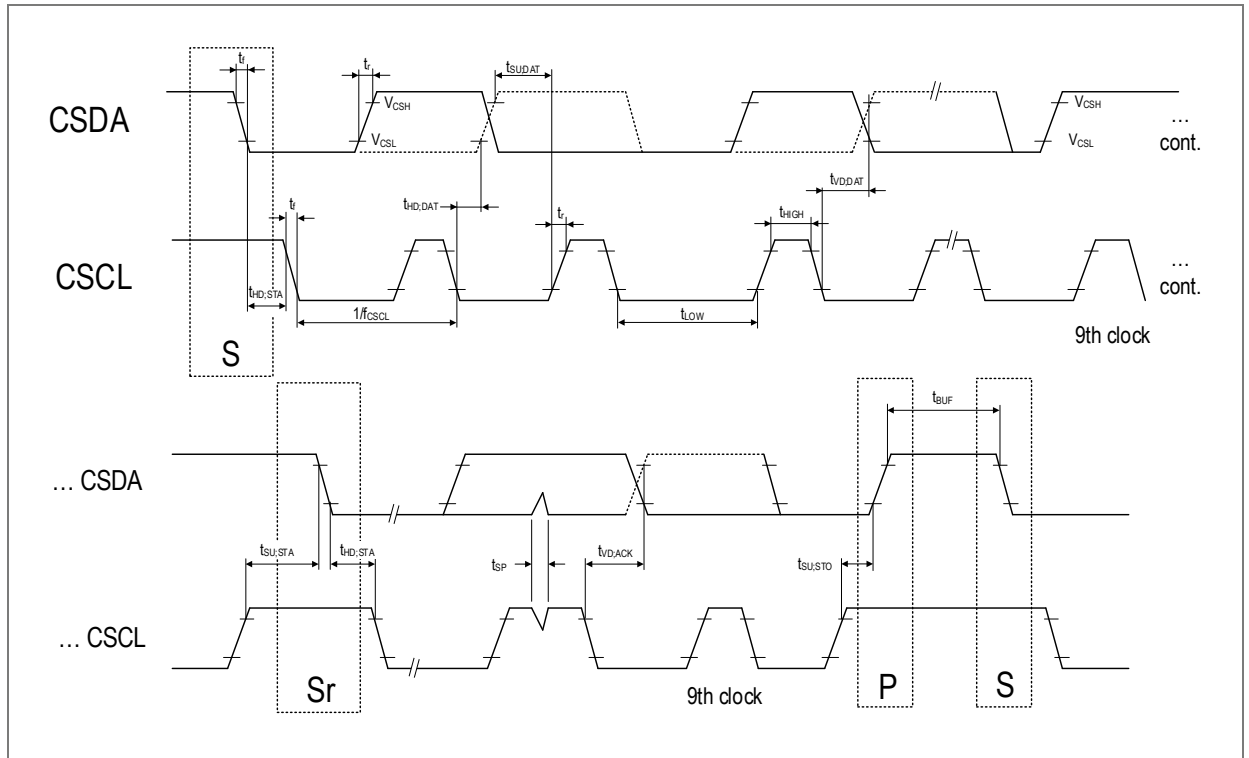


Table 9: Bus timing characteristics of AS7100

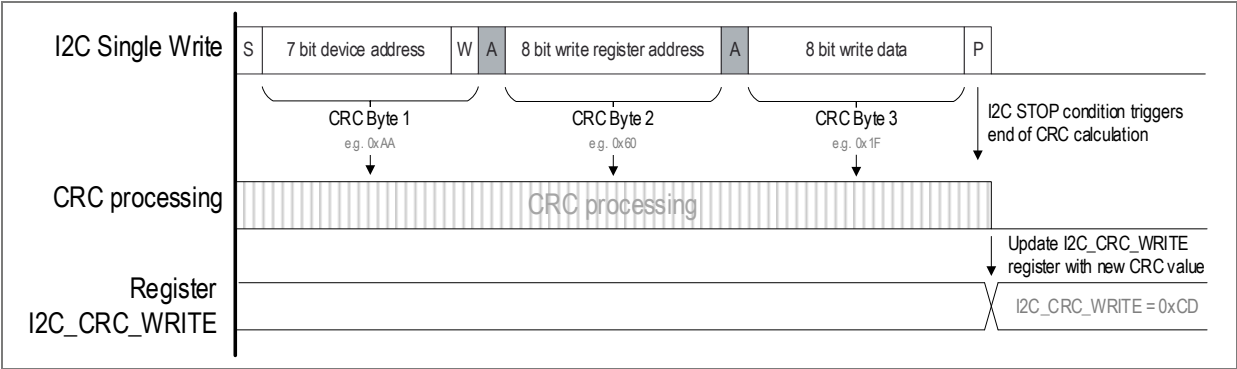
Symbol	Parameter	Min	Typ	Max	Units
Bus timing characteristics for I²C communications					
f_{SCL}	SCL clock frequency	0		400	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3			
$t_{HD,STA}$	Hold time for a (repeated) START condition. After this period, the first clock pulse is generated	0.6			μs
$t_{SU,STA}$	Set-up time for a repeated START condition	0.6			
$t_{SU,STO}$	Set-up time for STOP condition	0.6			
t_{LOW}	SCL clock low period	1.3			
t_{HIGH}	SCL clock high period	0.6			
$t_{HD,DAT}$	Data hold time	0		900	ns

Symbol	Parameter	Min	Typ	Max	Units
$t_{\text{SU,DAT}}$	Data setup time	100			
t_{F}	Fall time of both SDA and SCL signals			300	ns
t_{R}	Rise time of both SDA and SCL signals			300	
t_{SP}	Pulse width of spikes that must be suppressed by the input filter			50	ns

8.9.5 CRC function

AS7100 supports a 8-bit CRC function to secure the I2C data transfer between master and slave device. After each I2C read or write transaction the data bytes containing the device address, read/write address and data bytes are used for the CRC calculation. After each read or write transfer the **CRC_WRITE** and **CRC_READ** registers are updated. It is important to mention that CRC calculation only works if the on-chip oscillator of AS7100 is enabled via register **OSC_ON**. Furthermore, it is important when utilizing the CRC function to monitor data, that the **CRC_WRITE** and **CRC_READ** register must be read out immediately after a read or write access to the device because a new CRC value is calculated after each read and write access which overwrites the previous CRC value.

Figure 47: CRC write transaction (single data byte)



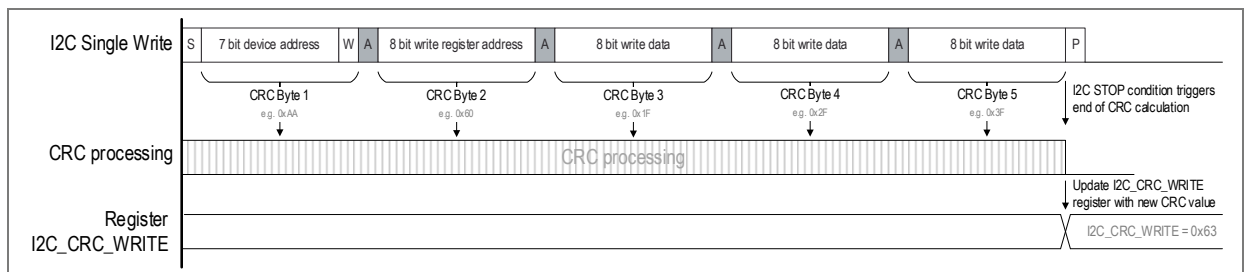
The diagram shown in Figure 47 provides an overview of a CRC monitored write transaction of a single data byte. The first CRC Byte 1 contains the I2C device write address including the write bit which is in the example 0xAA. The second transferred CRC Byte 2 is the write address which is in the example 0x60. The third and last CRC Byte 3 represents the data in the example which is 0x1F. The CRC processing block of AS7100 is continuously processing the CRC value and at the end of the write transaction an I2C Stop condition triggers the update of the **I2C_CRC_WRITE** byte with the value 0xCD as shown in the example in Figure 47.

Table 10: CRC-8 parameters

CRC-8 parameter	Value
CRC Polynomial	0x2F
CRC reset value	0xFF
CRC XOR	0x00

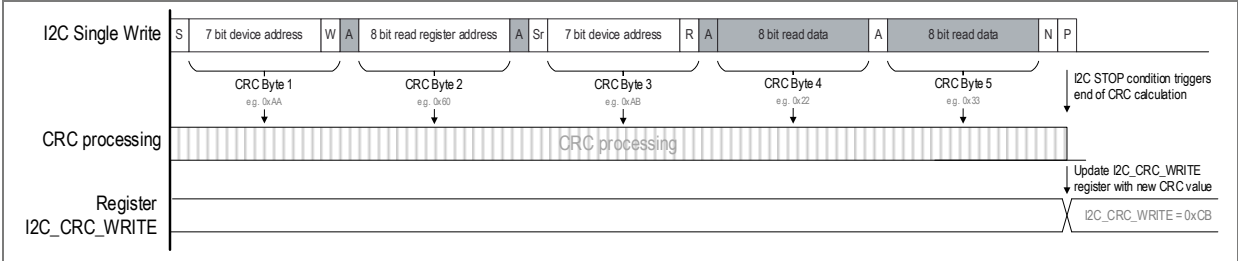
The CRC polynomial as well as the reset start value used for the CRC-8 computation build into AS7100 is shown in Table 10. An additional write example including CRC example values for writing multiple data bytes in a sequential order is shown in Figure 48.

Figure 48: CRC bulk write transaction



In order to get correctly calculated CRC read data it is important to follow the random device read protocol which is shown in Figure 49. It follows basically the I2C random read protocol which is also shown in Figure 43. Important for the CRC computation block is that after sending the device address followed by the read address register a repeated start condition has to be initiated which is then followed again by the device address with the read bit set to one.

Figure 49: CRC random device read

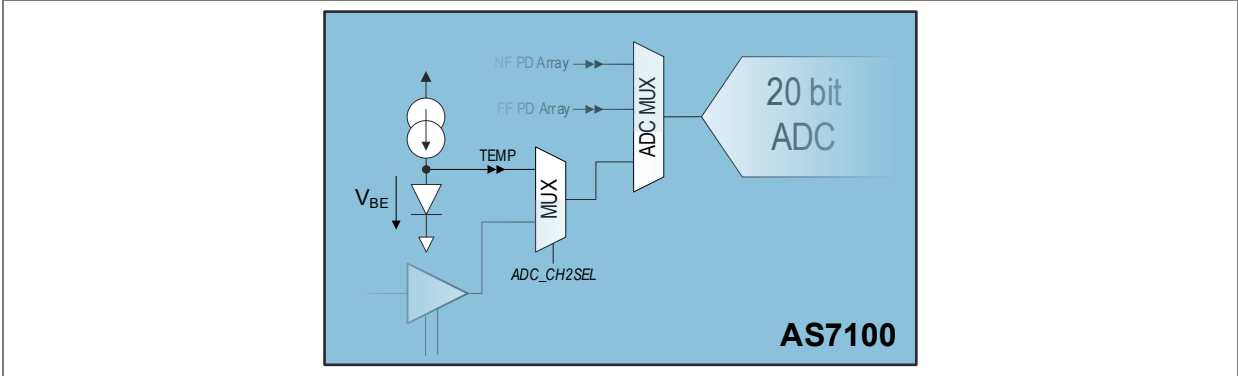


The repeated start condition is important for AS7100 CRC hardware block to recognize that the CRC computation continues for the device address and following data bytes. The read function is then terminated by a not acknowledge by the host device and a stop condition. Once the stop condition is transferred the updated CRC value calculated out of all transferred address and data bytes is stored the **I2C_CRC_READ** register like it is shown in Figure 49.

8.10 On chip temperature measurement

The AS7100 supports a relative on chip temperature measurement function to gather information about self-heating effect as well as ambient temperature conditions of the device. In order to get temperature information a diode forward voltage V_{BE} is monitored whose forward voltage is changing over temperature on average with around 2.1mV/°C. By measuring the voltage change with the ADC this can give information about a temperature change. Since there is no production calibration of the temperature measurement circuit done during mass production of AS7100, please mind that the device can provide relative temperature information only.

Figure 50: On-chip relative temperature measurement circuit



Equation 17: ADC counts per degree Celsius $ADC_{COUNT/DEG}$

$$ADC_{COUNT/DEG} = \frac{V_{TC}}{V_{ADCLSB}} = \frac{-0.00211 \text{ V}/^{\circ}\text{C}}{0.000366 \text{ V/Count}} = -5.77 \frac{\text{counts}}{^{\circ}\text{C}}$$

V_{TC} Temperature coefficient temperature measurement diode

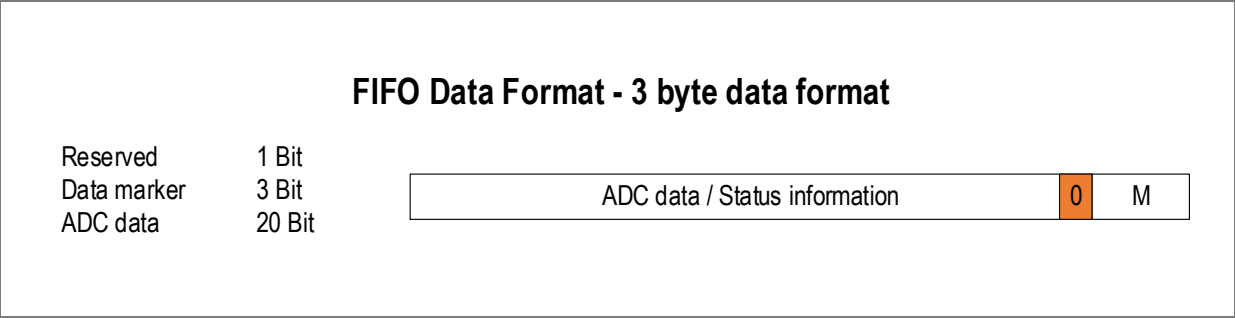
V_{ADCLSB} LSB ADC voltage

The calculation shown in Equation 17 provides an estimate on the expected ADC count change per degree Celsius temperature change which is in the range of -5.77 counts/°C. In order to find out relative temperature changes of the device in an application environment it is recommended to store the raw ADC count value as a reference under controlled ambient temperature conditions. This value is then the starting reference and includes already silicon process variations of the V_{BE} voltage which affects the ADC base line count value even at room temperature. As an example, we assume a typical ADC base line temperate value of e.g. 1400 counts at 25°C room temperature. If the sensor temperature is now rising by e.g. 10 degree Celsius the ADC reading is reduced by -5.77 counts multiplied by factor of 10 resulting at an ADC count value reading of 1342.3 counts at a temperature of approximately 35°C. Please also mind the $ADC_{COUNT/DEG}$ value is just a typical estimated value which is also prone to additional production tolerances.

8.11 FIFO description

The AS7100 contains a 256 byte FIFO register for buffering the measurement data output to an external microcontroller via the I²C. The FIFO buffering allows the external MCU to stay in sleep mode while proximity measurements are ongoing and proximity event data is stored to the FIFO memory. The coding of the data stream is described below in Figure 51. The standard format is 20 bit ADC data value flowed by a reserved bit which is always 0 and a three-bit data marker. The data marker describes the ADC measurement source which belongs to the provided 20 bit ADC data value. An overview of the different data sources and the assigned data marker bits is shown in Table 11 below.

Figure 51: FIFO data format with ECC disabled (*fifo_readmode* = 0)



Since the device supports also ECC data correction there is a second FIFO data format with 4 byte word length which is shown in Figure 52. This data format is active once *fifo_readmode* register set to one and ECC data correction is active.

Figure 52: FIFO data format with ECC enabled (*fifo_readmode* = 1)

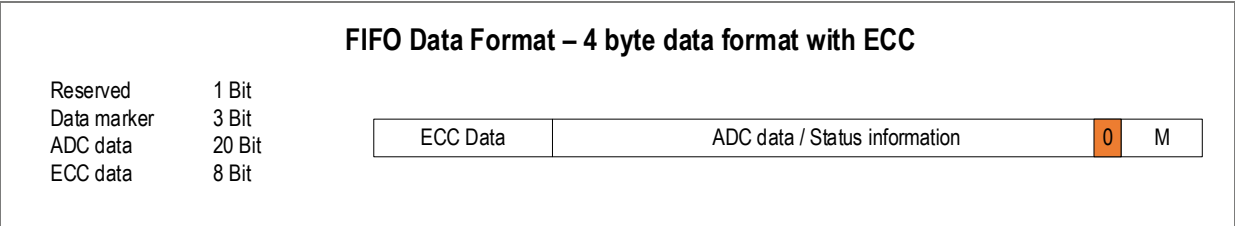


Table 11: FIFO data marker bit description

Data marker bits <2:0>	Description
'b'000	Other sample data of measurement in sub-sample 1 or 2 from modulator 1
'b'001	First sample data of measurement in sub-sample 1 from modulator 1
'b'010	First sample data of measurement in sub-sample 2 from modulator 1
'b'011	Temperature Data; measured by LED Sample
'b'100	Other sample data of measurement in sub-sample 1 or 2 from modulator 2
'b'101	First sample data of measurement in sub-sample 1 from modulator 2
'b'110	First sample data of measurement in sub-sample 2 from modulator 2
'b'111	Proximity data; used by proximity range detection

Table 12: ECC data bit description

7	6	5	4	3	2	1	0
ECC_STATE		PARITY		ECC			

Field	Bits	Description
ECC_STATE	7	The upper two bits of the ECC data contain the ECC state of the data word. 00: FIFO data correct 01: 1 bit error detected with bit error corrected by ECC engine 10: FIFO data with not correctable Failure, >1-bit
	6	
	5	
PARITY	5	This bit represents the even parity bit of the ECC data and 24 bit ADC data including data marker bit.
ECC	4	The lower 5 bits of the ECC data contain ECC hamming data
	3	
	2	
	1	
	0	

Figure 53: FIFO data structure and organization with 3 byte data format (*fifo_readmode* = 0)

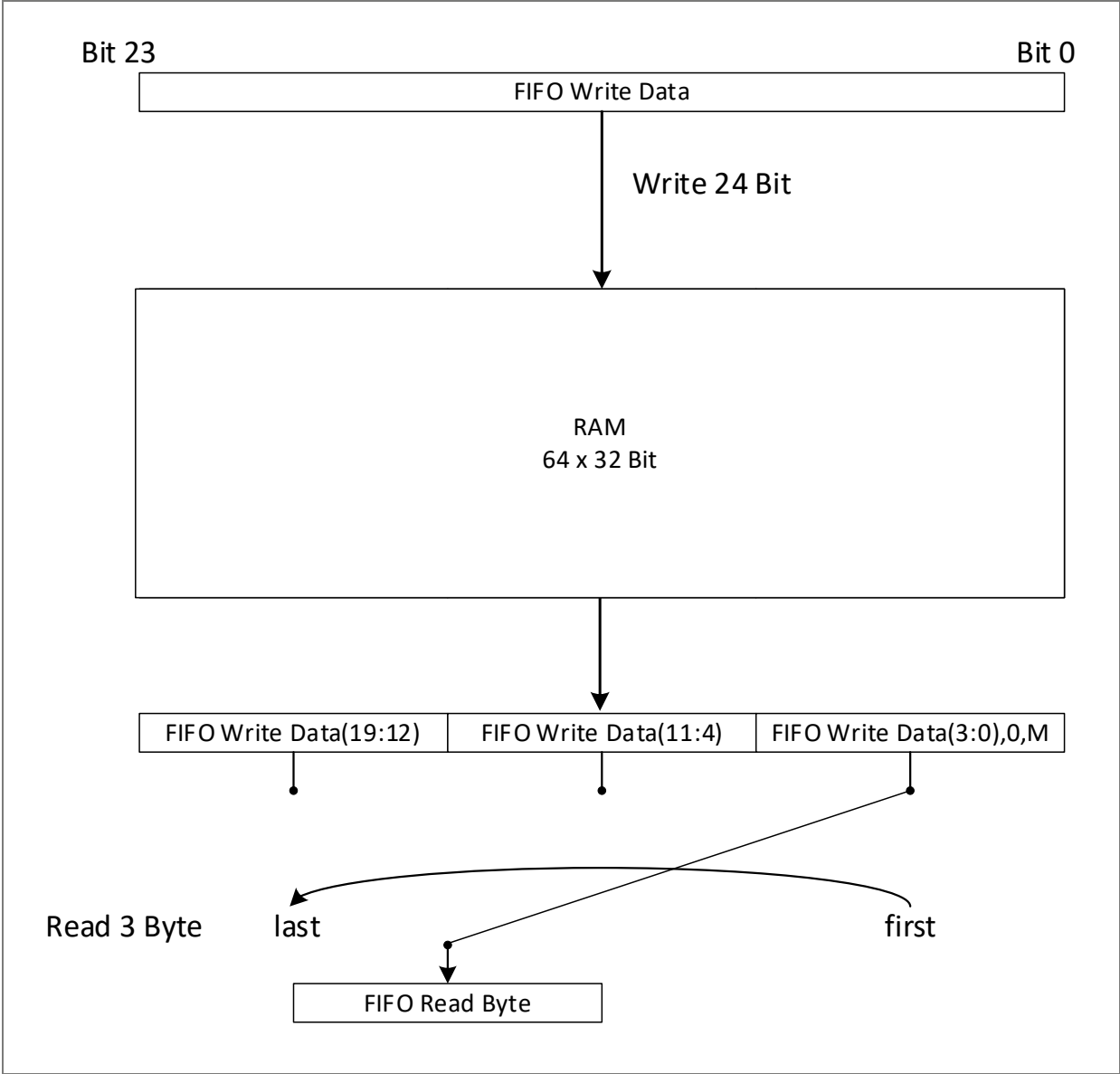
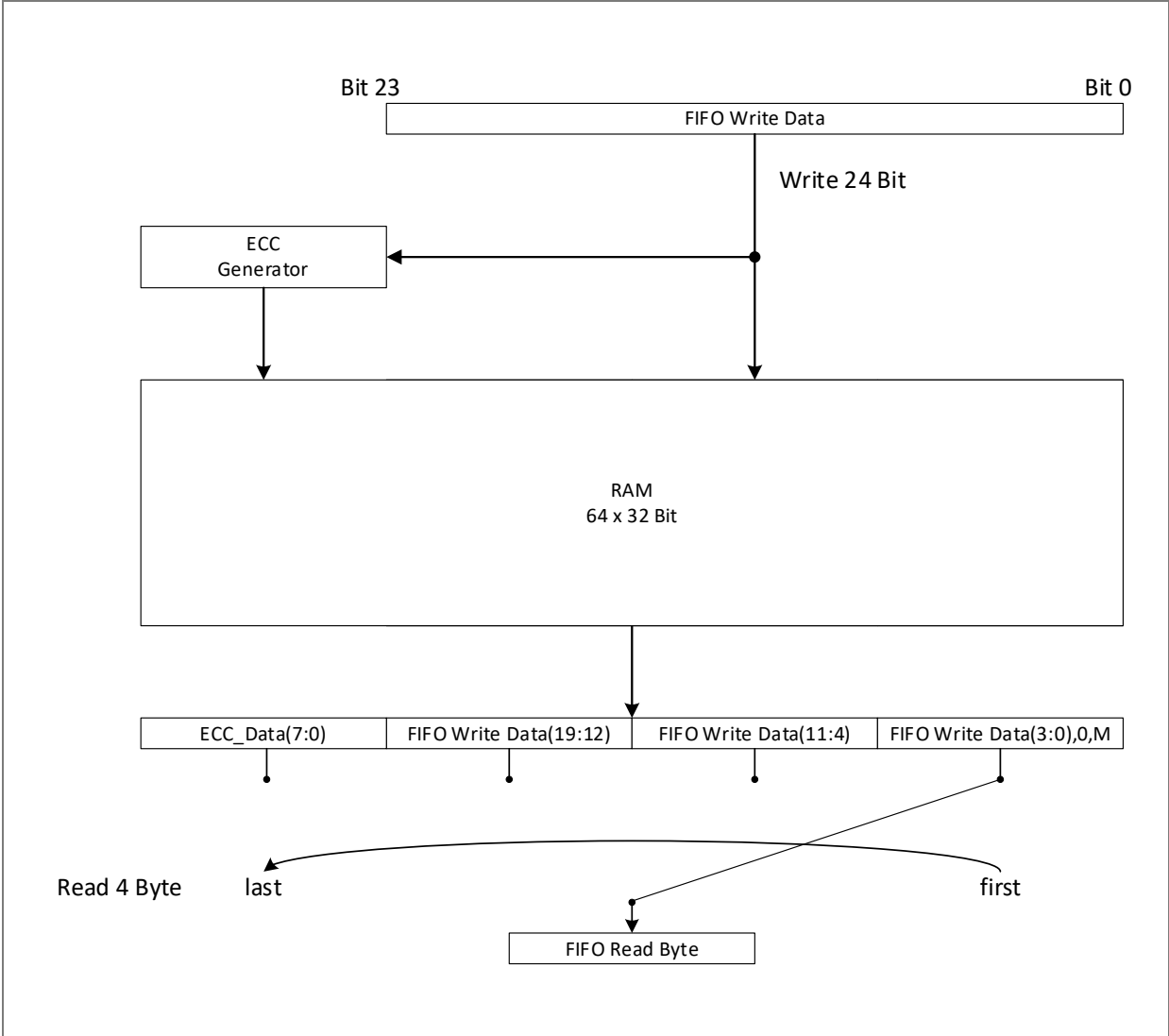


Figure 54: FIFO data structure and organization with 4 byte data format (*fifo_readmode* = 1)



8.11.1 ECC FIFO

The AS7100 supports an Error Correction Code (ECC) function which can detect defective data bits inside the FIFO memory. Furthermore, the ECC block is able to correct up to one defective data bit automatically. The ECC function can be enabled with the FIFO_ECC_EN register. Please mind that for ECC operation the FIFO_READMODE register has to be configured to 4-byte operation mode. Once the FIFO 4-byte operation mode is enabled the FIFO data structure shown in Figure 54 is valid for data readout. The fourth byte in the data word contains the relevant ECC data whose data structure is shown in Table 12.

The lower 5 bytes contain ECC data followed by a parity bit and two status bits which hold the information if the data is error free or if one or more bit errors got detected by the ECC block. In order to avoid constant monitoring of the fourth FIFO data byte AS7100 features an ECC status register **STATUS_RAM_ECC** which supports also interrupt functionality. The **IRQ_EN_MISC** register has to be set to enable interrupt notification if an ECC data error is detected and reported in the **STATUS_MISC** register which contains the **STATUS_RAM_ECC** register. By reading the self-clearing register information is provided if one or more corrupted data bits were detected by the ECC block. Once an interrupt got released and the host is notified the fourth data byte of the FIFO data can be analyzed to identify the corrupted data word. Please mind that up to 1 corrupted data bit is corrected automatically by the ECC block but still reported by setting the **STATUS_RAM_ECC** register to one.

9 Register description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

9.1 Register map

Table 13: AS7100 register overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
UNIQUE ID									
0x00	IC_ID[7:0]					ic_id[7:0]			
0x01	IC_ID[15:8]					ic_id[15:8]			
0x02	IC_ID[23:16]					ic_id[23:16]			
0x03	IC_ID[31:24]					ic_id[31:24]			
0x04	IC_ID[39:32]					ic_id[39:32]			
0x05	IC_ID[47:40]					ic_id[47:40]			
0x06	LED_ID[7:0]					led_id[7:0]			
0x07	LED_ID[15:8]					led_id[15:8]			
DEVICE CONFIGURATION									
0x10	I2C_CFG								i2c_fm_plus
0x11	OSC_CFG						vdd_ok	osc_ok	osc_on
0x12	INT_CFG					int_fast_out	int_inb_uf_on	int_in	int_inv
0x13	SYNC_CFG					sync_inbuff_on			
0x14	IO_CFG		sda_e2	sda_e4	sda_sr				
0x15	REF_CFG1		mod_coarse_vref		en_vref_trim_buf	en_mod_ref	en_vref_filter	mod_comp_lvl	
0x16	REF_CFG2			mod_comp_lvl_calib		trim_100n	en_temp_sensor	precharge_vref_filter	
0x17	LDR_CFG1			irange			trim_tk_i_ptat		
0x18	MOD_CFG1	mod_stop_force	temp_channel_disable	mod_channel_disable		mod_az_range		mod_shlp_short	mod_shlp_offset

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x19	VLEDMON_CFG						vledmon_insel	en_vledmon	en_ledmon_connect
AUTO ZERO CONFIGURATION									
0x20	AZ_CFG1						az_iterations		
0x21	AZ_CFG2	az_init_time							
0x22	AZ_CFG3	az_settling_time							
0x23	CH1_AZ_OFFSET_0	ch1_az_offset[7:0]							
0x24	CH1_AZ_OFFSET_1							ch1_az_offset[9:8]	
0x25	CH2_AZ_OFFSET_0	ch2_az_offset[7:0]							
0x26	CH2_AZ_OFFSET_1							ch2_az_offset[9:8]	
ADC CONFIGURATION									
0x30	LTFADC_CFG1				mod_strobe_clk_suppress	mod_clear_clk_position		mod_divider_select	
0x31	LTFADC_CFG2	adc_settling				adc_pre_settling			
0x32	LTFADC_CFG3						adc_ch2sel	adc_rst_mode	adc_power_down_mode
0x33	LTFADC_CFG4	mod_divider_select_calib		mod_clear_clk_position_calib			idac_mod_gain		
0x34	LTFADC_CFG5		mod1_gain2					mod1_gain1	
0x35	LTFADC_CFG6		mod2_gain2					mod2_gain1	
0x36	LTFADC_CFG7		mod_compensation_manual	mod_compensation2			mod_compensation1		
0x37	LTFADC_CFG8				mod_calib_coarse_average	sample_time_value_for_mod_coarse_count_suppress			
0x38	LTFADC_CFG9	mod_adc_low_sat_level					mod_adc_high_sat_level		
0x40	MOD1_IDAC1_VALUE		mod1_idac1_value						
0x41	MOD1_IDAC2_VALUE		mod1_idac2_value						
0x42	MOD2_IDAC1_VALUE		mod2_idac1_value						
0x43	MOD2_IDAC2_VALUE		mod2_idac2_value						
0x44	MOD_IDAC_CFG1	mod2_idac_ib_range		mod2_idac_range		mod1_idac_ib_range		mod1_idac_range	
0x45	MOD_IDAC_CFG2								mod_idac_enable
MODULATOR DATA									
0x48	MOD1_COARSE_DATA1_0	mod1_coarse_data1[7:0]							
0x49	MOD1_COARSE_DATA1_1						mod1_coarse_data1[11:8]		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x4A	MOD1_COARSE_DATA2_0				mod1_coarse_data2[7:0]				
0x4B	MOD1_COARSE_DATA2_1				mod1_coarse_data2[11:8]				
0x4C	MOD2_COARSE_DATA1_0				mod2_coarse_data1[7:0]				
0x4D	MOD2_COARSE_DATA1_1				mod2_coarse_data1[11:8]				
0x4E	MOD2_COARSE_DATA2_0				mod2_coarse_data2[7:0]				
0x4F	MOD2_COARSE_DATA2_1				mod2_coarse_data2[11:8]				
PROXIMITY CONFIGURATION									
0x50	PRX_CFG1					non_prx_measur e_on	prx_m easure _mod	prx_su b_coun t	
0x51	PRX_CFG2					prx_sample_ count2	prx_sample_ count1		
0x52	PRX_CFG3				prx_measure_count				
0x53	PRX_PERIOD_0				prx_period[7:0]				
0x54	PRX_PERIOD_1				prx_period[15:8]				
0x55	PRX_PERIOD_2				prx_period[19:16]				
0x56	PRX_WAIT_TIME				prx_wait_time				
PROXIMITY DATA									
0x57	PRX_DATA_MOD1_0				prx_data_mod1[7:0]				
0x58	PRX_DATA_MOD1_1				prx_data_mod1[15:8]				
0x59	PRX_DATA_MOD1_2				prx_data_mod1[19:16]				
0x5A	PRX_DATA_MOD2_0				prx_data_mod2[7:0]				
0x5B	PRX_DATA_MOD2_1				prx_data_mod2[15:8]				
0x5C	PRX_DATA_MOD2_2				prx_data_mod2[19:16]				
LED CONTROL									
0x60	LED_ISINK1				led_isink1				
0x61	LED_ISINK2				led_isink2				
0x62	LED_WAIT_TIME_0				led_wait_time[7:0]				
0x63	LED_WAIT_TIME_1				led_wait_time[11:8]				
0x64	LED_ON_TIME_0				led_on_time[7:0]				
0x65	LED_ON_TIME_1				led_on_time[11:8]				
PD SELECTION									
0x68	PDSEL_MOD1_SUB1				pdsel_mod1_sub1				
0x69	PDSEL_MOD1_SUB2				pdsel_mod1_sub2				
0x6A	PDSEL_MOD2_SUB1				pdsel_mod2_sub1				
0x6B	PDSEL_MOD2_SUB2				pdsel_mod2_sub2				
SAMPLE TIME									
0x70	SAMPLE_TIME_0				sample_time[7:0]				
0x71	SAMPLE_TIME_1				sample_time[10:8]				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
PROXIMITY CONFIGURATION									
0x78	PP_MOD1_XTALK_0					pp_mod1_xtalk[7:0]			
0x79	PP_MOD1_XTALK_1					pp_mod1_xtalk[15:8]			
0x7A	PP_MOD2_XTALK_0					pp_mod2_xtalk[7:0]			
0x7B	PP_MOD2_XTALK_1					pp_mod2_xtalk[15:8]			
0x7C	PP_MOD_GAIN		pp_mod2_gain					pp_mod1_gain	
0x7D	PP_DATA_WRITE					pp_wd ata_su b	pp_wdata_en		
0x80	PRX_SEL						prx_su b_sel	prx_data_sel	
0x81	PRX_OVS		prx_on_ovs					prx_off_ovs	
0x82	PRX_THH_0					prx_thh[7:0]			
0x83	PRX_THH_1					prx_thh[15:8]			
0x84	PRX_THL_0					prx_thl[7:0]			
0x85	PRX_THL_1					prx_thl[15:8]			
TEMPERATURE DATA									
0x88	TEMP_DATA_0					temp_data[7:0]			
0x89	TEMP_DATA_1					temp_data[11:8]			
IRQ CONTROL									
0x8E	IRQ_CONTROL	irq_prx_event_sel				irq_cntrl_event_sel			irq_cle ar_sel
0x8F	IRQ_ENABLE	irq_en _rb_re ady	irq_en _misc	irq_en _ovtem p	irq_en _sat	irq_en _prx	irq_en _fifo_o verflow	irq_en _fifo_th reshold	irq_en _cntrl
CRC									
0xC0	I2C_CRC_READ					crc_read			
0xC1	I2C_CRC_WRITE					crc_write			
0xC2	I2C_CRC_CTRL							crc_cle ar_writ e	crc_cle ar_rea d
FIFO CONTROL									
0xD0	FIFO_THRESHOLD				fifo_threshold				
0xD1	FIFO_CTRL	fifo_cle ar	fifo_rin gbuffer _en	fifo_ec c_en	fifo_re admod e	fifo_rin gbuffer _stop			
0xD2	RINGBUF_CTRL	prx_ev ent_cle ar	prx_ev ent_re ady	ringbuf_thr					
CHIP ID									
0xED	SILICON_ID					silicon_id			
0xEE	REVISION					rev_id			

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
DEVICE CONTROL									
0xEF	CHIP_CTRL								chip_re set
0xF0	CONTROL		sync_e n	sync_e dge	prx_en	ic_en	cc_en	az_en	start
SYNC CONTROL									
0xF1	SYNC_DELAY_0	sync_delay[7:0]							
0xF2	SYNC_DELAY_1	sync_delay[15:8]							
WAKEUP CONTROL									
0xF3	WAKEUP_DELAY	wakeup_delay							
STANDBY CONTROL									
0xF4	STANDBY_EN				enab_t emp_s ensor	enab_ mod_r ef	enab_v ref_tri m_buf	en_vle dmon	mod_e nable
STATUS REGISTERS									
0xF5	STATUS_MISC			status_ fail_reg	status_ram_ecc		status_ otp_crc 8	status_otp_ecc	
0xF6	STATUS_CNTRL						status_ cntrl_m freq	status_ cntrl_e om	status_ cntrl_e oc
0xF7	STATUS_SAT		status_adc_sat			status_pp_dsat		status_mod_asat	
0xF8	STATUS_PRX		status_ prx_hig h_on	status_ prx_hig h_off	status_ prx_hig h		status_ prx_lo w_on	status_ prx_lo w_off	status_ prx_lo w
0xF9	STATUS	irq_rb_ ready	irq_mis c	irq_ovt emp	irq_sat	irq_prx	irq_fifo_ _overfl ow	irq_fifo_ _thres hold	irq_cnt rl
FIFO									
0XFA	FIFO_LEVEL0		fifo_level						
0XFB	FIFO_LEVEL1					fifo_em pty	fifo_full	fifo_ov erflow	
0XFC	FIFO0	fifo0							
0XFD	FIFO1	fifo1							
0XFE	FIFO2	fifo2							
0XFF	FIFO3	fifo3							

9.2 Detailed register description

9.2.1 IC_ID[7:0] register (Address 0x00)

Table 14: IC_ID[7:0] register

Addr: 0x00		IC_ID[7:0]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ic_id[7:0]</i>	0x00	R/W	Unique device ID [7:0]

9.2.2 IC_ID[15:8] register (Address 0x01)

Table 15: IC_ID[15:8] register

Addr: 0x01		IC_ID[15:8]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ic_id[15:8]</i>	0x00	R/W	Unique device ID [15:8]

9.2.3 IC_ID[23:16] register (Address 0x02)

Table 16: IC_ID[23:16] register

Addr: 0x02		IC_ID[23:16]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ic_id[23:16]</i>	0x00	R/W	Unique device ID [23:16]

9.2.4 IC_ID[31:24] register (Address 0x03)

Table 17: IC_ID[31:24] register

Addr: 0x03		IC_ID[31:24]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ic_id[31:24]</i>	0x00	R/W	Unique device ID [31:24]

9.2.5 IC_ID[39:32] register (Address 0x04)

Table 18: IC_ID[39:32] register

Addr: 0x04		IC_ID[39:32]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ic_id[39:32]</i>	0x00	R/W	Unique device ID [39:32]

9.2.6 IC_ID[47:40] register (Address 0x05)

Table 19: IC_ID[47:40] register

Addr: 0x05		IC_ID[47:40]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ic_id[47:40]</i>	0x00	R/W	Unique device ID [47:40]

9.2.7 LED_ID[7:0] register (Address 0x06)

Table 20: LED_ID[7:0] register

Addr: 0x06		LED_ID[7:0]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led_id[7:0]</i>	0x00	R/W	Byte1 reserved for identification of the LED.

9.2.8 LED_ID[15:8] register (Address 0x07)

Table 21: LED_ID[15:8] register

Addr: 0x07		LED_ID[15:8]		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led_id[15:8]</i>	0x00	R/W	Byte2 reserved for identification of the LED

9.2.9 I2C_CFG register (Address 0x10)

Table 22: I2C_CFG register

Addr: 0x10		I2C_CFG		
Bit	Bit name	Default	Access	Bit description
0	<i>i2c_fm_plus</i>	0x00	R/W	This is the control register to enable I ² C fast mode plus with 1MHz. 0: Fast mode plus disabled 1: Fast mode plus enabled

9.2.10 OSC_CFG register (Address 0x11)

Table 23: OSC_CFG register

Addr: 0x11		OSC_CFG		
Bit	Bit name	Default	Access	Bit description
2	<i>vdd_ok</i>	0x00	R/W	This is the VDD undervoltage status bit. In case VDD voltages below 1.6V is detected the status bit is set to one. 0: VDD ok, no undervoltage detected 1: VDD undervoltage detected
1	<i>osc_ok</i>	0x00	R/W	This is the oscillator status bit which indicates if the oscillator is up and running. 0: Oscillator not running 1: Oscillator ok
0	<i>osc_on</i>	0x00	R/W	This is the internal on chip oscillator control bit which is necessary for measurements and standby mode operation. 0: Oscillator disabled 1: Oscillator enabled

9.2.11 INT_CFG register (Address 0x12)

Table 24: INT_CFG register

Addr: 0x12		INT_CFG		
Bit	Bit name	Default	Access	Bit description
3	<i>int_fast_out</i>	0x00	R/W	This register allows to increase the speed of the INT output pin by a factor of four. 0: Normal driving strength 1: Increased 4x driving strength
2	<i>int_inbuf_on</i>	0x00	R/W	This bit enables the INT pin input readback buffer which is necessary to read back INT pin status via register <i>int_in</i> . 0: INT input buffer disabled 1: INT input buffer enabled
1	<i>int_in</i>	0x00	RO	This is the INT pin status register which allows readback of the INT pin level for debugging purpose. Please mind that this register provides only valid result if <i>int_inbuf_on</i> bit is enabled. 0: INT pin low 1: INT pin high
0	<i>int_inv</i>	0x00	R/W	This is the control bit to invert the IRQ output pin. 0: IRQ normal output 1: IRQ inverted output enabled

9.2.12 SYNC_CFG register (Address 0x13)

Table 25: SYNC_CFG register

Addr: 0x13		SYNC_CFG		
Bit	Bit name	Default	Access	Bit description
2	<i>sync_inbuf_on</i>	0x00	R/W	This register enables the input buffer for the SYNC pin. This register must be enabled if the external synchronization via SYNC pin is used an application. 0: SYNC input buffer disabled 1: SYNC input buffer enabled

9.2.13 IO_CFG register (Address 0x14)

Table 26: IO_CFG register

Addr: 0x14		IO_CFG		
Bit	Bit name	Default	Access	Bit description
6	<i>sda_e2</i>	0x00	R/W	This bit controls the output driving strength together with <i>sda_e4</i> bit of the I ² C SDA pin. 0: 2 mA normal SDA pin driving strength (<i>sda_e4</i> = 0) 1: 4 mA increased SDA driving strength (<i>sda_e4</i> = 0)
5	<i>sda_e4</i>	0x00	R/W	This bit controls the output driving strength together with <i>sda_e2</i> bit of the I ² C SDA pin. 0: 2mA normal SDA pin driving strength (<i>sda_e2</i> = 0) 1: 4 mA increased SDA driving strength for <i>sda_e2</i> = 0 and 6mA SDA driving strength for <i>sda_e2</i> = 1
4	<i>sda_sr</i>	0x00	R/W	This bit controls the slew rate of the I ² C SDA pin. 0: Normal SDA slew rate 1: Increased SDA pin slew rate

9.2.14 REF_CFG1 register (Address 0x15)

Table 27: REF_CFG1 register

Addr: 0x15		REF_CFG1		
Bit	Bit name	Default	Access	Bit description
7:5	<i>mod_coarse_vref</i>	0x00	R/W	This is a trim register for the ADC modulator. Please do use register value provided by ams OSRAM support team. 0: 460mV / 0% 1: 485mV / 7% 2: 502mV / 15% 3: 555mV / 22.5% 4: 415mV / 7.5% 5: 380mV / 15% 6: 345mV / 22.5% 7: 310mV / 30%
4	<i>en_vref_trim_buf</i>	0x00	R/W	This bit enables the reference voltage buffer which is mandatory for ADC measurements. 0: Buffer disabled 1: Buffer enabled
3	<i>en_mod_ref</i>	0x00	R/W	This register enabled the voltage references which are necessary to operate the ADC modulators. 0: Voltage reference disabled 1: Voltage reference enabled
2	<i>en_vref_filter</i>	0x00	R/W	This register enables an on-chip noise filter for the internal voltage references. 0: Filter disabled 1: Filter enabled
1:0	<i>mod_comp_lvl</i>	0x01	R/W	This register allows control of the ADC modulator voltage comparator level. Please do use register value provided by ams OSRAM support team. 0: 1.2V comparator level 1: 1.3V comparator level 2: 1.4V comparator level 3: 1.5V comparator level

9.2.15 REF_CFG2 register (Address 0x16)

Table 28: REF_CFG2 register

Addr: 0x16		REF_CFG2		
Bit	Bit name	Default	Access	Bit description
5:4	<i>mod_comp_lv_calib</i>	0x2	R/W	This register allows to change internal voltage levels during the device calibration. Please do not change this register unless instructed by ams OSRAM support team. 0: 1.2V comparator level 1: 1.3V comparator level 2: 1.4V comparator level 3: 1.5V comparator level
3	<i>trim_100n</i>	0x00	R/W	This is a configuration bit to enable increased reference currents. Please do not change this register unless instructed by ams OSRAM support team. 0: Default reference current 1: 100nA increased reference current
2	<i>en_temp_sensor</i>	0x00	R/W	This bit enables the on-chip temperature sensor of AS7100. 0: Temperature sensor disabled 1: Temperature sensor enabled
1	<i>precharge_vref_filter</i>	0x00	R/W	This bit enables a faster settling time for the on-chip reference voltage noise filter. 0: Pre-charge filter disabled 1: Pre-charge filter enabled

9.2.16 LDR_CFG1 register (Address 0x17)

Table 29: LDR_CFG1 register

Addr: 0x17		LDR_CFG1		
Bit	Bit name	Default	Access	Bit description
5	<i>irange</i>	0x00	RW	This register allows to configure the on-chip LED driver current range which can be 25mA or 250mA depending on this register setting. 0: LED driver current range 0-250mA 1: LED driver current range 0-25mA
4:0	<i>trim_tk_i_ptat</i>	0x00	RW	This register contains temperature coefficient value for the LED driver. Please do not change this register. In case on chip LED temperature compensation is demanded please contact ams OSRAM service for support.

9.2.17 MOD_CFG1 register (Address 0x18)

Table 30: MOD_CFG1 register

Addr: 0x18		MOD_CFG1		
Bit	Bit name	Default	Access	Bit description
7	<i>mod_stop_force</i>	0x00	R/W	In case this bit is set to one the ADC is internally connected to a reference node. 0: Normal ADC operation 1: ADC connected to internal reference node
6	<i>temp_channel_disable</i>	0x00	R/W	Disables temperature channel measurement in case not needed in an application. 0: Temperature measurement disabled 1: Temperature measurement enabled
5:4	<i>mod_channel_disable</i>	0x00	R/W	These bits disable the ADC modulator measurement channel one and two. The bit position is equivalent to the modulator channel. 00: ADC modulator Channel 1 and 2 enabled 01: Channel 1 disabled; Channel 2 enabled 10: Channel 1 enabled; Channel 2 disabled 11: Channel 1 disabled; Channel 2 disabled Note: Modulator autozero is always done for all channels.
3:2	<i>mod_az_range</i>	0x00	R/W	This register allows you to adjust the autozero LSB voltage level. Please do not change this register unless instructed by ams OSRAM support team. 0: 28 μ V LSB voltage 1: 19 μ V LSB voltage 2: 10 μ V LSB voltage 3: 5 μ V LSB voltage
1	<i>mod_sh_lp_short</i>	0x00	R/W	This bit enables the low pass filter option between ADC modulator and ADC input. Please do not change this register unless instructed by ams OSRAM support team. 0: Modulator low pass filter enabled 1: Modulator low pass filter disabled
0	<i>mod_sh_lp_off</i>	0x00	R/W	This bit configures the low pass filter cut off frequency of the filter between ADC modulator and ADC input. Please do not change this register unless instructed by ams OSRAM support team. 0: 1 MHz 1: 6.5 MHz

9.2.18 VLEDMON_CFG register (Address 0x19)

Table 31: VLEDMON_CFG register

Addr: 0x19		VLEDMON_CFG		
Bit	Bit name	Default	Access	Bit description
2	<i>vledmon_in_sel</i>	0x00	R/W	This bit selects which voltage reference source is used for the LED driver voltage measurement. Please refer to Figure 20 in chapter 8.3 which shows a block diagram of the internal connections with the related registers. 0: Voltage measured between VDD and I/C pin 1: Voltage measured between I/C and GND pin
1	<i>en_vledmon</i>	0x00	R/W	This bit enables the LED driver voltage monitor function. Please mind that on chip temperature monitoring function is paused while voltage monitoring is enabled. Please refer to Figure 20 in chapter 8.3 which shows a block diagram of the internal connections with the related registers. 0: LED driver voltage monitoring disabled 1: LED driver voltage monitoring enabled
0	<i>en_led_mon_connect</i>	0x00	R/W	This bit enables the I/C node/pin to be connected to the LED voltage measurement input buffer. Please refer to Figure 20 in chapter 8.3 which shows a block diagram of the internal connections with the related registers. 0: VLED monitor buffer disconnected 1: VLED monitor buffer connected for voltage measurement

9.2.19 AZ_CFG1 register (Address 0x20)

Table 32: AZ_CFG1 register

Addr: 0x20		AZ_CFG1		
Bit	Bit name	Default	Access	Bit description
2:0	<i>az_iterations</i>	0x05	R/W	This register controls the number of averaging iterations during ADC modulator autozero calibration process. 0: Autozero averaging disabled 1: 1 autozero averaging iterations 2: 2 autozero averaging iterations 3: 4 autozero averaging iterations 4: 8 autozero averaging iterations 5: 16 autozero averaging iterations 6: 32 autozero averaging iterations 7: 64 autozero averaging iterations

9.2.20 AZ_CFG2 register (Address 0x21)

Table 33: AZ_CFG2 register

Addr: 0x21		AZ_CFG2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>az_init_time</i>	0x05	R/W	This register controls the initialization time for the autozero function. The initialization time is calculated with the register value multiplied by 1.429 μs. 0: 0 μs 1: 1.429 μs 2: 2.858 μs ... 254: 362.966 μs 255: 364.395 μs

9.2.21 AZ_CFG3 register (Address 0x22)

Table 34: AZ_CFG3 register

Addr: 0x22		AZ_CFG3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>az_settling_time</i>	0x07	R/W	This register controls the settling time for the autozero function. The settling time is calculated with the register value multiplied by 1.429 μs. 0: 0 μs 1: 1.429 μs 2: 2.858 μs ... 254: 362.966 μs 255: 364.395 μs

9.2.22 CH1_AZ_OFFSET_0 register (Address 0x23)

Table 35: CH1_AZ_OFFSET_0 register

Addr: 0x23		CH1_AZ_OFFSET_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ch1_az_offset[7:0]</i>	0x00	R/W_SM	This register holds the 8 lower bits of the autozero offset value for ADC channel 1. The register content is overwritten automatically by the auto zero mechanism but can also be overwritten externally. The autozero value is 10-bit wide and comes in a signed magnitude format with the upper two bits in the register CH1_AZ_OFFSET_1. The MSB of CH1_AZ_OFFSET_1 controls the sign with zero representing a positive number and with one a negative number. The remaining 9 bits which are assembled with the LSB from CH1_AZ_OFFSET_1 and 8-bit from CH1_AZ_OFFSET_0 register contain the autozero magnitude value.

9.2.23 CH1_AZ_OFFSET_1 register (Address 0x24)

Table 36: CH1_AZ_OFFSET_1 register

Addr: 0x24		CH1_AZ_OFFSET_1		
Bit	Bit name	Default	Access	Bit description
1:0	<i>ch1_az_offset[9:8]</i>	0x00	R/W_SM	This register holds the upper two bits of the 10-bit autozero offset value for ADC channel 1. The MSB of this register is the sign bit with zero representing a positive number and with one representing a negative number. The LSB of this register represents the MSB of the magnitude value together with CH1_AZ_OFFSET_0 register.

9.2.24 CH2_AZ_OFFSET_0 register (Address 0x25)

Table 37: CH2_AZ_OFFSET_0 register

Addr: 0x25		CH2_AZ_OFFSET_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>ch2_az_offset[7:0]</i>	0x00	R/W_SM	This register holds the 8 lower bits of the autozero offset value for ADC channel 2. The register content is overwritten automatically by the auto zero mechanism but can also be overwritten externally. The autozero value is 10-bit wide and comes in signed magnitude format with the upper two bits in the register CH2_AZ_OFFSET_1 . The MSB of CH2_AZ_OFFSET_1 controls the sign with zero representing a positive number and with one a negative number. The remaining 9 bits which are assembled with the LSB from CH2_AZ_OFFSET_1 and 8-bit from CH2_AZ_OFFSET_0 register contain the autozero magnitude value.

9.2.25 CH2_AZ_OFFSET_1 register (Address 0x26)

Table 38: CH2_AZ_OFFSET_1 register

Addr: 0x26		CH2_AZ_OFFSET_1		
Bit	Bit name	Default	Access	Bit description
1:0	<i>ch2_az_offset[9:8]</i>	0x00	R/W_SM	This register holds the upper two bits of the 10-bit autozero offset value for ADC channel 2. The MSB of this register is the sign bit with zero representing a positive number and with one representing a negative number. The LSB of this register represents the MSB of the magnitude value together with CH2_AZ_OFFSET_0 register.

9.2.26 LTFADC_CFG1 register (Address 0x30)

Table 39: LTFADC_CFG1 register

Addr: 0x30		LTFADC_CFG1		
Bit	Bit name	Default	Access	Bit description
5:4	<i>mod_strobe_clk_suppress</i>	0x03	R/W	This is another ADC modulator configuration register for clock control. Please do not change this register from its default value unless instructed by ams OSRAM support team.
3:2	<i>mod_clear_clk_position</i>	0x00	R/W	These bits control the clear position with respect to its modulator clocks. Please do not change this register from its default value unless instructed by ams OSRAM support team.
1:0	<i>mod_divider_select</i>	0x00	R/W	These bits control the modulator clock divider. Please do not change this from its default value register unless instructed by ams OSRAM support team. 0: 1428.571 ns 1: 2857.143 ns 2: 5714.286 ns 3: 11428.571 ns

9.2.27 LTFADC_CFG2 register (Address 0x31)

Table 40: LTFADC_CFG2 register

Addr: 0x31		LTFADC_CFG2		
Bit	Bit name	Default	Access	Bit description
7:5	<i>adc_settling</i>	0x00	R/W	These bits allow the configuration of the ADC settling time to compensate for effects when photodiodes are connected to the ADC and measurement is started. Please do not change this from its default value register unless instructed by ams OSRAM support team.
				0: 0 μ s ADC settling time
				1: 2 μ s ADC settling time
				2: 4 μ s ADC settling time
				3: 8 μ s ADC settling time
				4: 16 μ s ADC settling time
				5: 32 μ s ADC settling time
				6: 64 μ s ADC settling time
4:2	<i>adc_pre_settling</i>	0x00	R/W	These bits allow the configuration of the ADC pre-settling time to compensate for effects when connecting the photodiodes to the ADC. Please do not change this from its default value register unless instructed by ams OSRAM support team.
				0: 0 μ s ADC pre-settling time
				1: 2 μ s ADC pre-settling time
				2: 4 μ s ADC pre-settling time
				3: 8 μ s ADC pre-settling time
				4: 16 μ s ADC pre-settling time
				5: 32 μ s ADC pre-settling time
				6: 64 μ s ADC pre-settling time
				7: 128 μ s ADC pre-settling time

9.2.28 LTFADC_CFG3 register (Address 0x32)

Table 41: LTFADC_CFG3 register

Addr: 0x32		LTFADC_CFG3		
Bit	Bit name	Default	Access	Bit description
3:2	<i>adc_ch2sel</i>	0x00	R/W	These bits control the input source for the third ADC measurement channel. There is the option to select between a temperature measurement or the LED driver forward voltage measurement. Please refer to Figure 20 in chapter 8.3 which shows a block diagram of the internal connections with the related registers. 00: LED driver monitor measurement selected 01: Temperature measurement selected 10: Do not use 11: Do not use
1	<i>adc_rst_mode</i>	0x00	R/W	This bit allows to reset the ADC between measurement samples. Please do not change this from its default value register unless instructed by ams OSRAM support team. 0: ADC power down disabled 1: ADC power down enabled
0	<i>adc_power_down_mode</i>	0x00	R/W	This bit allows for power down of the ADC between measurement samples. Please do not change this from its default value register unless instructed by ams OSRAM support team. 0: ADC power down disabled 1: ADC power down enabled

9.2.29 LTFADC_CFG4 register (Address 0x33)

Table 42: LTFADC_CFG4 register

Addr: 0x33		LTFADC_CFG4		
Bit	Bit name	Default	Access	Bit description
7:6	<i>idac_mod_gain</i>	0x00	R/W	Used modulator gain during modulator IDAC calibration in case of Modulator-Based-Proximity. Recommended operation value for this register is 0x01.
5:4	<i>mod_clear_clk_position_calib</i>	0x03	R/W	Selection of modulator clear clock position during coarse calibration and modulator IDAC calibration. Please do not change this from its default value register unless instructed by ams OSRAM support team.
2:0	<i>mod_divider_select_calib</i>	0x00	R/W	Selection of modulator divider during coarse calibration and modulator IDAC calibration. Please do not change this from its default value register unless instructed by ams OSRAM support team.

9.2.30 LTFADC_CFG5 register (Address 0x34)

Table 43: LTFADC_CFG5 register

Addr: 0x34		LTFADC_CFG5		
Bit	Bit name	Default	Access	Bit description
6:4	mod1_gain2	0x00	R/W	This is the analog gain control register for modulator 1 for subsample 2 measurement.
				0: 1 x gain
				1: 2 x gain
				2: 4 x gain
				3: 8 x gain
				4: 16 x gain
				5: 32 x gain
				6: 64 x gain
2:0	mod1_gain1	0x00	R/W	7: 128 x gain
				This is the analog gain control register for modulator 1 for subsample 1 measurement.
				0: 1 x gain
				1: 2 x gain
				2: 4 x gain
				3: 8 x gain
				4: 16 x gain
				5: 32 x gain
				6: 64 x gain
				7: 128 x gain

9.2.31 LTFADC_CFG6 register (Address 0x35)

Table 44: LTFADC_CFG6 register

Addr: 0x35		LTFADC_CFG6		
Bit	Bit name	Default	Access	Bit description
6:4	mod2_gain2	0x00	R/W	This is the analog gain control register for modulator 2 for subsample 2 measurement.
				0: 1 x gain
				1: 2 x gain
				2: 4 x gain
				3: 8 x gain
				4: 16 x gain
				5: 32 x gain
				6: 64 x gain
2:0	mod2_gain1	0x00	R/W	7: 128 x gain
				This is the analog gain control register for modulator 2 for subsample 1 measurement.
				0: 1 x gain
				1: 2 x gain
				2: 4 x gain
				3: 8 x gain
				4: 16 x gain
				5: 32 x gain
				6: 64 x gain
				7: 128 x gain

9.2.32 LTFADC_CFG7 register (Address 0x36)

Table 45: LTFADC_CFG7 register

Addr: 0x36		LTFADC_CFG7		
Bit	Bit name	Default	Access	Bit description
6	<i>mod_compensation_manual</i>	0x00	R/W	This bit enables the manual compensation of ADC modulator. Please do not change this from its default value register unless instructed by ams OSRAM support team. 0: Disables manual modulator compensation 1: Enabled manual modulator compensation
5:3	<i>mod_compensation2</i>	0x01	R/W	This register contains the manual modulator compensation value for ADC channel 2. Please do not change this from its default value register unless instructed by ams OSRAM support team.
2:0	<i>mod_compensation1</i>	0x01	R/W	This register contains the manual modulator compensation value for ADC channel 1. Please do not change this from its default value register unless instructed by ams OSRAM support team.

9.2.33 LTFADC_CFG8 register (Address 0x37)

Table 46: LTFADC_CFG8 register

Addr: 0x37		LTFADC_CFG8		
Bit	Bit name	Default	Access	Bit description
5:4	<i>mod_calib_coarse_average</i>	0x00	R/W	This register defines the number of coarse calibration cycles for the ADC modulators. Please do not change this from its default value register unless instructed by ams OSRAM support team. 0: 1 calibration cycle 1: 2 calibration cycles with averaging 2: 4 calibration cycles with averaging 3: 8 calibration cycles with averaging
3:0	<i>sample_time_value_for_mod_coarse_count_suppress</i>	0x01	R/W	This is an ADC control register for internal coarse count clock suppression. Please do not change this from its default value register unless instructed by ams OSRAM support team.

9.2.34 LTFADC_CFG9 register (Address 0x38)

Table 47: LTFADC_CFG9 register

Addr: 0x38		LTFADC_CFG9		
Bit	Bit name	Default	Access	Bit description
7:4	<i>mod_adc_low_sat_level</i>	0x00	R/W	This register defines the lower threshold limit of the ADC saturation. The control register affects the lowest 16 codes of the ADC value. If the ADC value is smaller or equal the configured threshold ADC saturation is released. There is also a dedicated interrupt register STATUS_SAT linked to a ADC saturation events which can be enabled <i>irq_en_sat</i> register. 0: 0x000 1: 0x001 2: 0x002 ... 14: 0x00e 15: 0x00f
3:0	<i>mod_adc_high_sat_level</i>	0x00	R/W	This register defines the upper threshold limit of the ADC saturation. The control register affects the highest 16 codes of the ADC value. If the ADC value is bigger or equal to the configured threshold ADC saturation is released. There is also a dedicated interrupt register STATUS_SAT linked to a ADC saturation events which can be enabled <i>irq_en_sat</i> register. 0: 0xFF0 1: 0xFF1 2: 0xFF2 ... 14: 0xFFe 15: 0xFFf

9.2.35 MOD1_IDAC1_VALUE register (Address 0x40)

Table 48: MOD1_IDAC1_VALUE register

Addr: 0x40		MOD1_IDAC1_VALUE		
Bit	Bit name	Default	Access	Bit description
6:0	<i>mod1_idac1_value</i>	0x00	R/W	This 7-bit register controls the IDAC current of ADC1 for Subsample 1.

9.2.36 MOD1_IDAC2_VALUE register (Address 0x41)

Table 49: MOD1_IDAC2_VALUE register

Addr: 0x41		MOD1_IDAC2_VALUE		
Bit	Bit name	Default	Access	Bit description
6:0	<i>mod1_idac2_value</i>	0x00	R/W	This 7-bit register controls the IDAC current of ADC1 for Subsample 2.

9.2.37 MOD2_IDAC1_VALUE register (Address 0x42)

Table 50: MOD2_IDAC1_VALUE register

Addr: 0x42		MOD2_IDAC1_VALUE		
Bit	Bit name	Default	Access	Bit description
6:0	<i>mod2_idac1_value</i>	0x00	R/W	This 7-bit register controls the IDAC current of ADC2 for Subsample 1.

9.2.38 MOD2_IDAC2_VALUE register (Address 0x43)

Table 51: MOD2_IDAC2_VALUE register

Addr: 0x43		MOD2_IDAC2_VALUE		
Bit	Bit name	Default	Access	Bit description
6:0	<i>mod2_idac2_value</i>	0x00	R/W	This 7-bit register controls the IDAC current of ADC2 for Subsample 2.

9.2.39 MOD_IDAC_CFG1 register (Address 0x44)

Table 52: MOD_IDAC_CFG1 register

Addr: 0x44		MOD_IDAC_CFG1		
Bit	Bit name	Default	Access	Bit description
7:6	<i>mod2_idac_ib_range</i>	0x00	R/W	This register controls the IDAC bias range of ADC 2.
5:4	<i>mod2_idac_range</i>	0x00	R/W	This register controls the IDAC current range of ADC 2.
3:2	<i>mod1_idac_ib_range</i>	0x00	R/W	This register controls the IDAC bias range of ADC 1.
1:0	<i>mod1_idac_range</i>	0x00	R/W	This register controls the IDAC current range of ADC 1.

9.2.40 MOD_IDAC_CFG2 register (Address 0x45)

Table 53: MOD_IDAC_CFG2 register

Addr: 0x45		MOD_IDAC_CFG2		
Bit	Bit name	Default	Access	Bit description
0	<i>mod_idac_enable</i>	0x00	R/W	This register enables the IDAC function for ADC1 and ADC 2. 0: IDAC function disabled 1: IDAC function enabled

9.2.41 MOD1_COARSE_DATA1_0 register (Address 0x48)

Table 54: MOD1_COARSE_DATA1_0 register

Addr: 0x48		MOD1_COARSE_DATA1_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod1_coarse_data1[7:0]</i>	0x00	R/W_SM	This register contains the lower byte of the ADC coarse calibration data for sub-sample 1 of modulator 1. This register is informal only. This register must not be changed by users.

9.2.42 MOD1_COARSE_DATA1_1 register (Address 0x49)

Table 55: MOD1_COARSE_DATA1_1 register

Addr: 0x49		MOD1_COARSE_DATA1_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>mod1_coarse_data1[11:8]</i>	0x00	R/W_SM	This register contains the upper nibble of the ADC coarse calibration data for sub-sample 1 of modulator 1. This register is informal only. This register must not be changed by users.

9.2.43 MOD1_COARSE_DATA2_0 register (Address 0x4A)

Table 56: MOD1_COARSE_DATA2_0 register

Addr: 0x4A		MOD1_COARSE_DATA2_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod1_coarse_data2[7:0]</i>	0x00	R/W_SM	This register contains the lower byte of the ADC coarse calibration data for sub-sample 2 of modulator 1. This register is informal only. This register must not be changed by users.

9.2.44 MOD1_COARSE_DATA2_1 register (Address 0x4B)

Table 57: MOD1_COARSE_DATA2_1 register

Addr: 0x4B		MOD1_COARSE_DATA2_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>mod1_coarse_data2[11:8]</i>	0x00	R/W_SM	This register contains the upper nibble of the ADC coarse calibration data for sub-sample 2 of modulator 1. This register is informal only. This register must not be changed by users.

9.2.45 MOD2_COARSE_DATA1_0 register (Address 0x4C)

Table 58: MOD2_COARSE_DATA1_0 register

Addr: 0x4C		MOD2_COARSE_DATA1_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod2_coarse_data1[7:0]</i>	0x00	R/W_SM	This register contains the lower byte of the ADC coarse calibration data for sub-sample 1 of modulator 2. This register is informal only. This register must not be changed by users.

9.2.46 MOD2_COARSE_DATA1_1 register (Address 0x4D)

Table 59: MOD2_COARSE_DATA1_1 register

Addr: 0x4D		MOD2_COARSE_DATA1_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>mod2_coarse_data1[11:8]</i>	0x00	R/W_SM	This register contains the upper nibble of the ADC coarse calibration data for sub-sample 1 of modulator 2. This register is informal only. This register must not be changed by users.

9.2.47 MOD2_COARSE_DATA2_0 register (Address 0x4E)

Table 60: MOD2_COARSE_DATA2_0 register

Addr: 0x4E		MOD2_COARSE_DATA2_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>mod2_coarse_data2[7:0]</i>	0x00	R/W_SM	This register contains the lower byte of the ADC coarse calibration data for sub-sample 2 of modulator 2. This register is informal only. This register must not be changed by users.

9.2.48 MOD2_COARSE_DATA2_1 register (Address 0x4F)

Table 61: MOD2_COARSE_DATA2_1 register

Addr: 0x4F		MOD2_COARSE_DATA2_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>mod2_coarse_data2[11:8]</i>	0x00	R/W_SM	This register contains the upper nibble of the ADC coarse calibration data for sub-sample 2 of modulator 2. This register is informal only. This register must not be changed by users.

9.2.49 PRX_CFG1 register (Address 0x50)

Table 62: PRX_CFG1 register

Addr: 0x50		PRX_CFG1		
Bit	Bit name	Default	Access	Bit description
3:2	<i>non_prx_measure_on</i>	0x00	R/W	This bit controls the measurement mode for sub-sample 1 and sub-sample 2 which can be either a proximity measurement or an ambient light measurement. Bit 0 in this register controls measurement mode for sub-sample 1 and bit 1 controls measurement mode for sub-sample 2. Please refer to chapter 8.8.2 Measurement types for more information about the measurement modes. 00: Sub 1 proximity mode / Sub 2 proximity mode 01: Sub 1 ambient mode / Sub 2 proximity mode 10: Sub 1 proximity mode / Sub 2 ambient mode 11: Sub 1 ambient mode / Sub 2 ambient mode
1	<i>prx_measure_mod</i>	0x00	R/W	If this bit is set to one a wait time t_{PRX_WAIT} between the measurement samples and prior to the LED on phase is enabled whose timing can be controlled via register PRX_WAIT_TIME. Please refer to chapter 10 and Figure 33 which shows the timing diagram of a proximity measurement including t_{PRX_WAIT}. 0: Proximity wait time t_{PRX_WAIT} disabled 1: Proximity wait time t_{PRX_WAIT} enabled
0	<i>prx_sub_count</i>	0x00	R/W	This bit enables the second sub-sample in a proximity measurement. Please refer to chapter 8.8.1 for more details regarding proximity sample structure. 0: Sub-sample 2 disabled for measurement 1: Sub-sample 2 enabled for measurement

9.2.50 PRX_CFG2 register (Address 0x51)

Table 63: PRX_CFG2 register

Addr: 0x51		PRX_CFG2		
Bit	Bit name	Default	Access	Bit description
3:2	<i>prx_sample_count2</i>	0x00	R/W	This register configures the proximity sampling repetition rate per proximity sample, which is also known as proximity pulses per proximity sample, for subsample 2. By increasing the number of pulses, the sampling process of the ambient light (LED off phase) and proximity pulse (LED on phase) is repeated by the selected number. The proximity pulse measurements are then average for further signal processing. 0: 1 proximity pulse 1: 2 proximity pulses 2: 4 proximity pulses 3: 8 proximity pulses
1:0	<i>prx_sample_count1</i>	0x00	R/W	This register configures the proximity sampling repetition rate per proximity sample, which is also known as proximity pulses per proximity sample, for subsample 1. By increasing the number of pulses, the sampling process of the ambient light (LED off phase) and proximity pulse (LED on phase) is repeated by the selected number. The proximity pulse measurements are then average for further signal processing. 0: 1 proximity pulse 1: 2 proximity pulses 2: 4 proximity pulses 3: 8 proximity pulses

9.2.51 PRX_CFG3 register (Address 0x52)

Table 64: PRX_CFG3 register

Addr: 0x52		PRX_CFG3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_measure_count</i>	0x00	R/W	This register controls the number of proximity measurements which are measured. If this register is set to zero the device is in continuous measurement mode. Please refer to Figure 17 in chapter 8.1 Operation modes which show a flow chart and the effect of this register.
				0: Continuous measurements
				1: 1 proximity / light measurement
				2: 2 proximity / light measurements
				3: 3 proximity / light measurements
				...
				254: 254 proximity / light measurements
				255: 255 proximity / light measurements

9.2.52 PRX_PERIOD_0 register (Address 0x53)

Table 65: PRX_PERIOD_0 register

Addr: 0x53		PRX_PERIOD_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_period[7:0]</i>	0x77	R/W	This register is the lower byte of the proximity period control register which allows for the configuration of the sample time t_{PERIOD} together with PRX_PERIOD_1 and PRX_PERIOD_2 register. The 20-bit register enables samples rates from 700 kHz down to 0.67 Hz. Please refer to Equation 8 in chapter 8.8 for the calculation and definition of t_{PERIOD} .

9.2.53 PRX_PERIOD_1 register (Address 0x54)

Table 66: PRX_PERIOD_1 register

Addr: 0x54		PRX_PERIOD_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_period[15:8]</i>	0x05	R/W	This register is the second byte of the proximity period control register which allows for the configuration of the sample time t_{PERIOD} together with PRX_PERIOD_0 and PRX_PERIOD_2 register. The 20-bit register enables samples rates from 700 kHz down to 0.67 Hz. Please refer to Equation 8 in chapter 8.8 for the calculation and definition of t_{PERIOD} .

9.2.54 PRX_PERIOD_2 register (Address 0x55)

Table 67: PRX_PERIOD_2 register

Addr: 0x55		PRX_PERIOD_2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_period[19:16]</i>	0x00	R/W	This register is the upper nibble of the proximity period control register which allows for the configuration of the sample time t_{PERIOD} together with PRX_PERIOD_0 and PRX_PERIOD_1 register. The 20-bit register enables samples rates from 700 kHz down to 0.67 Hz. Please refer to Equation 8 in chapter 8.8 for the calculation and definition of t_{PERIOD} .

9.2.55 PRX_WAIT_TIME register (Address 0x56)

Table 68: PRX_WAIT_TIME register

Addr: 0x56		PRX_WAIT_TIME		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_wait_time</i>	0x00	R/W	This is the control register for the proximity wait time $t_{\text{PRX_WAIT}}$ between measurement samples. Please refer to Equation 13 for the calculation of $t_{\text{PRX_WAIT}}$.

9.2.56 PRX_DATA_MOD1_0 register (Address 0x57)

Table 69: PRX_DATA_MOD1_0 register

Addr: 0x57		PRX_DATA_MOD1_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_data_mod1[7:0]</i>	0x00	RO	This is the lower proximity data byte of modulator 1.

9.2.57 PRX_DATA_MOD1_1 register (Address 0x58)

Table 70: PRX_DATA_MOD1_1 register

Addr: 0x58		PRX_DATA_MOD1_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_data_mod1[15:8]</i>	0x00	RO	This is the middle proximity data byte of modulator 1.

9.2.58 PRX_DATA_MOD1_2 register (Address 0x59)

Table 71: PRX_DATA_MOD1_2 register

Addr: 0x59		PRX_DATA_MOD1_2		
Bit	Bit name	Default	Access	Bit description
3:0	<i>prx_data_mod1[19:16]</i>	0x00	RO	This is the upper proximity data nibble of modulator 1.

9.2.59 PRX_DATA_MOD2_0 register (Address 0x5A)

Table 72: PRX_DATA_MOD2_0 register

Addr: 0x5A		PRX_DATA_MOD2_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_data_mod2[7:0]</i>	0x00	RO	This is the lower proximity data byte of modulator 2.

9.2.60 PRX_DATA_MOD2_1 register (Address 0x5B)

Table 73: PRX_DATA_MOD2_1 register

Addr: 0x5B		PRX_DATA_MOD2_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_data_mod2[15:8]</i>	0x00	RO	This is the middle proximity data byte of modulator 2.

9.2.61 PRX_DATA_MOD2_2 register (Address 0x5C)

Table 74: PRX_DATA_MOD2_2 register

Addr: 0x5C		PRX_DATA_MOD2_2		
Bit	Bit name	Default	Access	Bit description
3:0	<i>prx_data_mod2[19:16]</i>	0x00	RO	This is the upper proximity data nibble of modulator 2.

9.2.62 LED_ISINK1 register (Address 0x60)

Table 75: LED_ISINK1 register

Addr: 0x60		LED_ISINK1		
Bit	Bit name	Default	Access	Bit description
5:0	<i>led_isink1</i>	0x00	R/W	This is the 6-bit wide IR LED current control register for sub-sample one. If the register is set to zero the LED is disabled. The internal current sink supports two different operating current ranges which are 25mA and 250mA which can be controlled via IRANGE register. Depending on the IRANGE configuration the LSB value of this current control register is changing. The table below provides therefore both current values for 25 mA and 250 mA LED driver range. 0: LED off 1: 0.397 mA / 3.97 mA 2: 0.794 mA / 7.94 mA 3: 1.19 mA / 11.9mA ... 63: 25 mA / 250 mA

9.2.63 LED_ISINK2 register (Address 0x61)

Table 76: LED_ISINK2 register

Addr: 0x61		LED_ISINK2		
Bit	Bit name	Default	Access	Bit description
5:0	<i>led_isink2</i>	0x00	R/W	This is the 6-bit wide IR LED current control register for sub-sample two. If the register is set to zero the LED is disabled. The internal current sink supports two different operating current ranges which are 25mA and 250mA which can be controlled via IRANGE register. Depending on the IRANGE configuration the LSB value of this current control register is changing. The table below provides therefore both current values for 25 mA and 250 mA LED driver range. 0: LED off 1: 0.397 mA / 3.97 mA 2: 0.794 mA / 7.94 mA 3: 1.19 mA / 11.9mA ... 63: 25 mA / 250 mA

9.2.64 LED_WAIT_TIME_0 register (Address 0x62)

Table 77: LED_WAIT_TIME_0 register

Addr: 0x62		LED_WAIT_TIME_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led_wait_time[7:0]</i>	0x00	R/W	This is the lower byte of LED wait time control register which allows you to delay the LED start during the LED on phase. Please refer to Equation 10 for the exact calculation of t_{LED_WAIT} time. The timing diagram which shows t_{LED_WAIT} is shown in Figure 31 and Figure 33. 0: No LED wait time; LED starts immediately 1: 1.43 μs 2: 2.86 μs 3: 4.29 μs ... 4095: 5.85 ms

9.2.65 LED_WAIT_TIME_1 register (Address 0x63)

Table 78: LED_WAIT_TIME_1 register

Addr: 0x63		LED_WAIT_TIME_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>led_wait_time[11:8]</i>	0x00	R/W	This is the upper nibble of LED wait time control register which allows you to delay the LED start during the LED on phase. Please refer to Equation 10 for the exact calculation of t_{LED_WAIT} time. The timing diagram which shows t_{LED_WAIT} is shown in Figure 31 and Figure 33. 0: No LED wait time; LED starts immediately 1: 1.43 μs 2: 2.86 μs 3: 4.29 μs ... 4095: 5.85 ms

9.2.66 LED_ON_TIME_0 register (Address 0x64)

Table 79: LED_ON_TIME_0 register

Addr: 0x64		LED_ON_TIME_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>led_on_time[7:0]</i>	0x00	R/W	This is the lower byte of LED on time control register which allows you to define the LED on time pulse length during the LED on phase. Please refer to Equation 11 for the exact calculation of t_{LED_ON} time. The timing diagram which shows t_{LED_ON} is shown in Figure 31 and Figure 33. 0: 1.43 μs 1: 2.86 μs 2: 4.29 μs ... 4095: 5.85 ms

9.2.67 LED_ON_TIME_1 register (Address 0x65)

Table 80: LED_ON_TIME_1 register

Addr: 0x65		LED_ON_TIME_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>led_on_time[11:8]</i>	0x00	R/W	This is the lower byte of LED on time control register which allows you to define the LED on time pulse length during the LED on phase. Please refer to Equation 11 for the exact calculation of t_{LED_ON} time. The timing diagram which shows t_{LED_ON} is shown in Figure 31 and Figure 33. 0: 1.43 μs 1: 2.86 μs 2: 4.29 μs ... 4095: 5.85 ms

9.2.68 PDSEL_MOD1_SUB1 register (Address 0x68)

Table 81: PDSEL_MOD1_SUB1 register

Addr: 0x68		PDSEL_MOD1_SUB1		
Bit	Bit name	Default	Access	Bit description
4:0	<i>pdsel_mod1_sub1</i>	0x00	R/W	This register assigns the on-chip photodiodes to modulator 1 during sub-sample 1 measurement phase. Each bit represents one photodiode. If a bit is set to one the assigned photodiode is connected to modulator 1 during the measurement. The physical location of the photodiodes on AS7100 is shown in Figure 21. Bit 0 Photodiode 1 Bit 1 Photodiode 2 Bit 2 Photodiode 3 Bit 3 Photodiode 4 Bit 4 Photodiode 5 Bit 5 Photodiode 6

9.2.69 PDSEL_MOD1_SUB2 register (Address 0x69)

Table 82: PDSEL_MOD1_SUB2 register

Addr: 0x69		PDSEL_MOD1_SUB2		
Bit	Bit name	Default	Access	Bit description
				This register assigns the on-chip photodiodes to modulator 1 during sub-sample 2 measurement phase. Each bit represents one photodiode. If a bit is set to one the assigned photodiode is connected to modulator 1 during the measurement. The physical location of the photodiodes on AS7100 is shown in Figure 21.
4:0	<i>pdsel_mod1_sub2</i>	0x00	R/W	Bit 0 Photodiode 1 Bit 1 Photodiode 2 Bit 2 Photodiode 3 Bit 3 Photodiode 4 Bit 4 Photodiode 5 Bit 5 Photodiode 6

9.2.70 PDSEL_MOD2_SUB1 register (Address 0x6A)

Table 83: PDSEL_MOD2_SUB1 register

Addr: 0x6A		PDSEL_MOD2_SUB1		
Bit	Bit name	Default	Access	Bit description
				This register assigns the on-chip photodiodes to modulator 2 during sub-sample 1 measurement phase. Each bit represents one photodiode. If a bit is set to one the assigned photodiode is connected to modulator 2 during the measurement. The physical location of the photodiodes on AS7100 is shown in Figure 21.
4:0	<i>pdsel_mod2_sub1</i>	0x00	R/W	Bit 0 Photodiode 1 Bit 1 Photodiode 2 Bit 2 Photodiode 3 Bit 3 Photodiode 4 Bit 4 Photodiode 5 Bit 5 Photodiode 6

9.2.71 PDSEL_MOD2_SUB2 register (Address 0x6B)

Table 84: PDSEL_MOD2_SUB2 register

Addr: 0x6B		PDSEL_MOD2_SUB2		
Bit	Bit name	Default	Access	Bit description
4:0	<i>pdsel_mod2_sub2</i>	0x00	R/W	This register assigns the on-chip photodiodes to modulator 2 during sub-sample 2 measurement phase. Each bit represents one photodiode. If a bit is set to one the assigned photodiode is connected to modulator 2 during the measurement. The physical location of the photodiodes on AS7100 is shown in Figure 21. Bit 0 Photodiode 1 Bit 1 Photodiode 2 Bit 2 Photodiode 3 Bit 3 Photodiode 4 Bit 4 Photodiode 5 Bit 5 Photodiode 6

9.2.72 SAMPLE_TIME_0 register (Address 0x70)

Table 85: SAMPLE_TIME_0 register

Addr: 0x70		SAMPLE_TIME_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sample_time[7:0]</i>	0xAE	R/W	This is the lower register byte of t_{SAMPLE} time register. Please refer to Equation 9 for calculation of t_{SAMPLE}. The timing is shown in Figure 31 and Figure 33. 0: 1.429 μs sample time 1: 2.875 μs sample time 2: 4.286 μs sample time ... 2047: 2.924 ms sample time

9.2.73 SAMPLE_TIME_1 register (Address 0x71)

Table 86: SAMPLE_TIME_1 register

Addr: 0x71		SAMPLE_TIME_1		
Bit	Bit name	Default	Access	Bit description
2:0	<i>sample_time[10:8]</i>	0xAE	R/W	This is the upper nibble of t_{SAMPLE} time register. Please refer to Equation 9 for calculation of t_{SAMPLE}. The timing is shown in Figure 31 and Figure 33. 0: 1.429 μs sample time 1: 2.875 μs sample time 2: 4.286 μs sample time ... 2047: 2.924 ms sample time

9.2.74 PP_MOD1_XTALK_0 register (Address 0x78)

Table 87: PP_MOD1_XTALK_0 register

Addr: 0x78		PP_MOD1_XTALK_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>pp_mod1_xtalk[7:0]</i>	0x00	R/W	This is the lower byte of the digital crosstalk offset register for modulator one. Please refer to chapter 8.6 Data processing and Figure 25 for more details regarding the digital proximity data stream and how the cross talk value is processed as part of the overall signal processing. Please mind that the configured register value of this register features a multiplication factor of 16 which is used for signal processing. Thus, if the register is configured to register value of e.g. 5, a crosstalk value of 80 is used for crosstalk signal processing. Please refer to Figure 25 for details regarding crosstalk signal processing.

9.2.75 PP_MOD1_XTALK_1 register (Address 0x79)

Table 88: PP_MOD1_XTALK_1 register

Addr: 0x79		PP_MOD1_XTALK_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>pp_mod1_xtalk[15:8]</i>	0x00	R/W	This is the upper byte of the digital crosstalk offset register for modulator one. Please refer to chapter 8.6 Data processing and Figure 25 for more details regarding the digital proximity data stream and how the cross talk value is processed as part of the overall signal processing. Please mind that the configured register value of this register features a multiplication factor of 16 which is used for signal processing. Thus, if the register is configured to register value of e.g. 5, a crosstalk value of 80 is used for crosstalk signal processing. Please refer to Figure 25 for details regarding crosstalk signal processing.

9.2.76 PP_MOD2_XTALK_0 register (Address 0x7A)

Table 89: PP_MOD2_XTALK_0 register

Addr: 0x7A		PP_MOD2_XTALK_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>pp_mod2_xtalk[7:0]</i>	0x00	R/W	This is the lower byte of the digital crosstalk offset register for modulator two. Please refer to chapter 8.6 Data processing and Figure 25 for more details regarding the digital proximity data stream and how the cross talk value is processed as part of the overall signal processing. Please mind that the configured register value of this register features a multiplication factor of 16 which is used for signal processing. Thus, if the register is configured to register value of e.g. 5, a crosstalk value of 80 is used for crosstalk signal processing. Please refer to Figure 25 for details regarding crosstalk signal processing.

9.2.77 PP_MOD2_XTALK_1 register (Address 0x7B)

Table 90: PP_MOD2_XTALK_1 register

Addr: 0x7B		PP_MOD2_XTALK_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>pp_mod2_xtalk[15:8]</i>	0x00	R/W	This is the upper byte of the digital crosstalk offset register for modulator two. Please refer to chapter 8.6 Data processing and Figure 25 for more details regarding the digital proximity data stream and how the cross talk value is processed as part of the overall signal processing. Please mind that the configured register value of this register features a multiplication factor of 16 which is used for signal processing. Thus, if the register is configured to register value of e.g. 5, a crosstalk value of 80 is used for crosstalk signal processing. Please refer to Figure 25 for details regarding crosstalk signal processing.

9.2.78 PP_MOD_GAIN register (Address 0x7C)

Table 91: PP_MOD_GAIN register

Addr: 0x7C		PP_MOD_GAIN		
Bit	Bit name	Default	Access	Bit description
6:4	<i>pp_mod2_gain</i>	0x03	R/W	This is the digital gain register for modulator two. Please refer to chapter 8.6 Data processing and Figure 25 for more details regarding the digital modulator gain. 0: 0.25 gain factor 1: 0.50 gain factor 2: 0.75 gain factor 3: 1.00 gain factor 4: 1.25 gain factor 5: 1.50 gain factor 6: 1.75 gain factor 7: 2.00 gain factor
2:0	<i>pp_mod1_gain</i>	0x03	R/W	This is the digital gain register for modulator one. Please refer to chapter 8.6 Data processing and Figure 25 for more details regarding the digital modulator gain. 0: 0.25 gain factor 1: 0.50 gain factor 2: 0.75 gain factor 3: 1.00 gain factor 4: 1.25 gain factor 5: 1.50 gain factor 6: 1.75 gain factor 7: 2.00 gain factor

9.2.79 PP_DATA_WRITE register (Address 0x7D)

Table 92: PP_DATA_WRITE register

Addr: 0x7D		PP_DATA_WRITE		
Bit	Bit name	Default	Access	Bit description
4	<i>pp_wdata_sub</i>	0x00	R/W	This register defines which ADC modulator data is written to the FIFO memory. 0: Calculated proximity measurement value 1: Raw data samples of LED off phase and LED on phase stored to FIFO. Minimum of 3 samples and a maximum of 17 sample
3:0	<i>pp_wdata_en</i>	0x00	R/W	This register defines which data sources are written to the FIFO memory. Each bit represents an individual data source which can be enabled and disabled for writing to the FIFO. Bit 0: Enable ADC Modulator 1 data for FIFO writing Bit 1: Enable ADC Modulator 2 data for FIFO writing Bit 2: Enable temperature data for FIFO writing Bit 3: Enable input data from proximity range detection for FIFO writing

9.2.80 PRX_SEL register (Address 0x80)

Table 93: PRX_SEL register

Addr: 0x80		PRX_SEL		
Bit	Bit name	Default	Access	Bit description
3:2	<i>prx_sub_sel</i>	0x00	R/W	This register defines which sub-sample is used for the proximity detection function. It is possible to enable both subsamples for proximity detection. In case both are enabled they are processed sequentially. Bit 0: Sub-sample 1 used for proximity detection Bit 1: Sub-sample 2 used for proximity detection
1:0	<i>prx_data_sel</i>	0x00	R/W	This register selects the input source for the proximity detection function. Please refer to chapter 8.7 Proximity detection for more information regarding the input source selection. 0: Modulator 1 selected as proximity input source 1: Modulator 2 selected as proximity input source 2: Modulator 1 – Modulator 2 as proximity input source

9.2.81 PRX_OVS register (Address 0x81)

Table 94: PRX_OVS register

Addr: 0x81		PRX_OVS		
Bit	Bit name	Default	Access	Bit description
6:4	<i>prx_on_ovs</i>	0x00	R/W	This register enables the digital oversampling function for the proximity up detection. If the register is set to zero the oversampling function is disabled. Once the register is set to e.g. 2, the proximity measurement value must be at least three times in a row above or below the PRX_THH register value to trigger a proximity event. Please refer to chapter 8.7 Proximity detection and Figure 27 for a detailed timing diagram.
				0: No oversampling
				1: 1 x oversampling
				2: 2 x oversampling
				3: 3 x oversampling
				4: 4 x oversampling
				5: 5 x oversampling
				6: 6 x oversampling
2:0	<i>prx_off_ovs</i>	0x00	R/W	7: 7 x oversampling
				This register enables the digital oversampling function for the proximity low detection. If the register is set to zero the oversampling function is disabled. Once the register is set to e.g. 2, the proximity measurement value must be at least three times in a row below or above the PRX_THL register value to trigger a proximity event. Please refer to chapter 8.7 Proximity detection and Figure 27 for a detailed timing diagram.
				0: No oversampling
				1: 1 x oversampling
				2: 2 x oversampling
				3: 3 x oversampling
				4: 4 x oversampling
				5: 5 x oversampling
				6: 6 x oversampling
				7: 7 x oversampling

9.2.82 PRX_THH_0 register (Address 0x82)

Table 95: PRX_THH_0 register

Addr: 0x82		PRX_THH_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_thh[7:0]</i>	0xFF	R/W	This is the lower byte of the proximity high threshold register. Please refer to chapter 8.7 Proximity detection and Figure 27 for a graphical explanation of this register.

9.2.83 PRX_THH_1 register (Address 0x83)

Table 96: PRX_THH_1 register

Addr: 0x83		PRX_THH_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_thh[15:8]</i>	0xFF	R/W	This is the high byte of the proximity high threshold register. Please refer to chapter 8.7 Proximity detection and Figure 27 for a graphical explanation of this register.

9.2.84 PRX_THL_0 register (Address 0x84)

Table 97: PRX_THL_0 register

Addr: 0x84		PRX_THL_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_thl[7:0]</i>	0x00	R/W	This is the lower byte of the proximity low threshold register. Please refer to chapter 8.7 Proximity detection and Figure 27 for a graphical explanation of this register.

9.2.85 PRX_THL_1 register (Address 0x85)

Table 98: PRX_THL_1 register

Addr: 0x85		PRX_THL_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>prx_thl[15:8]</i>	0x00	R/W	This is the high byte of the proximity low threshold register. Please refer to chapter 8.7 Proximity detection and Figure 27 for a graphical explanation of this register.

9.2.86 TEMP_DATA_0 register (Address 0x88)

Table 99: TEMP_DATA_0 register

Addr: 0x88		TEMP_DATA_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>temp_data[7:0]</i>	0x00	RO	This register contains the lower eight bit of the 12-bit temperature measurement data in case temperature measurement is enabled.

9.2.87 TEMP_DATA_1 register (Address 0x89)

Table 100: TEMP_DATA_1 register

Addr: 0x89		TEMP_DATA_1		
Bit	Bit name	Default	Access	Bit description
3:0	<i>temp_data[11:8]</i>	0x00	RO	This register contains the upper nibble of the 12-bit temperature measurement data in case temperature measurement is enabled.

9.2.88 IRQ_CONTROL register (Address 0x8E)

Table 101: IRQ_CONTROL register

Addr: 0x8E		IRQ_CONTROL		
Bit	Bit name	Default	Access	Bit description
7:4	<i>irq_prx_event_sel</i>	0x00	R/W	This is the interrupt enable register for the proximity events. Each bit of this register enables a different proximity interrupt. Once an interrupt is enabled by setting it to one the status can be read out at the STATUS_PRX registers. Please refer also to Figure 27 for a timing diagram which describes all interrupt status registers. Bit 0: Proximity low on Bit 1: Proximity low off Bit 2: Proximity high off Bit 3: Proximity high on
3:1	<i>irq_cntrl_event_sel</i>	0x00	R/W	This is an interrupt control register to enable different interrupt sources. Each bit of this register enables a different interrupt function. Writing a one to the corresponding bit enables the interrupt. The EoC interrupt is released after every ADC conversion. The EoM can be used to trigger an interrupt if a series of measurements was configured and the number of defined measurements got finished. The MFREQ register interrupt is released if $t_{\text{INTEGRATION}}$ is longer than t_{PERIOD}. In such case t_{PERIOD} must be reconfigured. Bit 0: EoC (End of ADC conversion) Bit 1: EoM (End of measurement) Bit 2: MFREQ
0	<i>irq_clear_sel</i>	0x00	R/W	This is the control register to select the event for clearing an interrupt status register. There are two options available. First option is by a readout of the entire interrupt register all interrupts in the register are cleared automatically. The second options is that the host MCU needs to write explicitly a 1 to the respective interrupt register bit to clear the interrupt. 0: Reading the interrupt register clears all interrupts in and interrupt register 1: Writing a 1 to the respective bit position clears the interrupt

9.2.89 IRQ_ENABLE register (Address 0x8F)

Table 102: IRQ_ENABLE register

Addr: 0x8F		IRQ_ENABLE		
Bit	Bit name	Default	Access	Bit description
7	<i>irq_en_rb_ready</i>	0x00	R/W	This is the interrupt enable register for the ring-buffer to release an interrupt once it is fully filled and ready for readout. The ring buffer status can be read out from STATUS register. 0: Ring-buffer ready interrupt disabled 1: Ring-buffer ready interrupt enabled
6	<i>irq_en_misc</i>	0x00	R/W	This is the interrupt enable register for miscellaneous device functions. Its status is available in the STATUS_MISC register. 0: Miscellaneous interrupt disabled 1: Miscellaneous interrupt enabled
5	<i>irq_en_ovtemp</i>	0x00	R/W	This is the interrupt enable register for on chip overtemperature detection. Once an interrupt is released the status can be read out from STATUS register. 0: Overtemperature interrupt disabled 1: Overtemperature interrupt enabled
4	<i>irq_en_sat</i>	0x00	R/W	This is the interrupt enable register for ADC saturation. Once an interrupt is released the saturation status can be read out from STATUS register. 0: ADC saturation interrupt disabled 1: ADC saturation interrupt enabled
3	<i>irq_en_prx</i>	0x00	R/W	This is the interrupt enable register for the proximity events. Once an interrupt is released the status can be read out from STATUS_PRX register. 0: Proximity interrupts disabled 1: Proximity interrupts enabled
2	<i>irq_en_fifo_overflow</i>	0x00	R/W	This is the interrupt enable register for the FIFO overflow. In case a FIFO overflow occurs an interrupt is released. Once an interrupt is released the FIFO overflow status can be read out from STATUS register. 0: FIFO threshold interrupt disabled 1: FIFO threshold interrupt enabled
1	<i>irq_en_fifo_threshold</i>	0x00	R/W	This is the interrupt enable register for the FIFO threshold. In case the configured FIFO threshold is reached an interrupt is released. Once an interrupt is released the FIFO threshold status can be read out from STATUS register. 0: FIFO threshold interrupt disabled 1: FIFO threshold interrupt enabled

Addr: 0x8F		IRQ_ENABLE		
Bit	Bit name	Default	Access	Bit description
0	<i>irq_en_cntrl</i>	0x00	R/W	This is the interrupt enable register for various control functions which can be further enabled in the IRQ_CONTROL register. 0: Interrupt control disabled 1: Interrupt control enabled

9.2.90 I2C_CRC_READ register (Address 0xC0)

Table 103: I2C_CRC_READ register

Addr: 0xC0		I2C_CRC_READ		
Bit	Bit name	Default	Access	Bit description
7:0	<i>crc_read</i>	0x00	R/W_SM	This is the CRC8 register for read transaction.

9.2.91 I2C_CRC_WRITE register (Address 0xC1)

Table 104: I2C_CRC_WRITE register

Addr: 0xC1		I2C_CRC_WRITE		
Bit	Bit name	Default	Access	Bit description
7:0	<i>crc_write</i>	0x00	R/W_SM	This is the CRC8 register for write transaction.

9.2.92 I2C_CRC_CTRL register (Address 0xC2)

Table 105: I2C_CRC_CTRL register

Addr: 0xC2		I2C_CRC_CTRL		
Bit	Bit name	Default	Access	Bit description
1	<i>crc_clear_write</i>	0x00	PUSH1	CRC8 clear read CRC and internal CRC register.
0	<i>crc_clear_read</i>	0x00	PUSH1	CRC8 clear write CRC and internal CRC register.

9.2.93 FIFO_THRESHOLD register (Address 0xD0)

Table 106: FIFO_THRESHOLD register

Addr: 0xD0		FIFO_THRESHOLD		
Bit	Bit name	Default	Access	Bit description
				This is the FIFO threshold register. In case the FIFO threshold interrupt is enabled in IRQ_ENABLE register and the FIFO level is higher than the configured threshold value an interrupt is released.
				0: 1.56 % of full FIFO
				1: 3.13 % of full FIFO
				2: 4.69% of full FIFO
				...
				16: 25% of full FIFO (default value)
				...
				63: 100% of full FIFO

9.2.94 FIFO_CTRL register (Address 0xD1)

Table 107: FIFO_CTRL register

Addr: 0xD1		FIFO_CTRL		
Bit	Bit name	Default	Access	Bit description
7	<i>fifo_clear</i>	0x00	PUSH	This is a self-clearing register. Once this register is written to one the FIFO read and write pointers are cleared.
6	<i>fifo_ringbuffer_en</i>	0x00	R/W	This is the control register for the FIFO to enable ring buffer operation mode. 0: FIFO operation mode 1: Ring buffer operation mode
5	<i>fifo_ecc_en</i>	0x00	R/W	This register enables the FIFO ECC correction. 0: ECC correction off 1: ECC correction enabled
4	<i>fifo_readmode</i>	0x00	R/W	This is the FIFO configuration register for the burst reading word length. The 3 byte burst length is default for communication. Reconfiguring to 4 byte burst length gets also the ECC data byte out of the FIFO. Please refer to chapter 8.10 for more details. 0: 3 byte 1: 4 byte
3	<i>fifo_ringbuffer_stop</i>	0x00	R/W	This is the control bit for the ring buffer stop function once a proximity event is detected to make sure ring buffer data is not overwritten and the proximity event measurement data are stored in the FIFO memory. 0: No measurement stop after proximity event 1: Measurement stop after proximity detection after number of measurements defined in <i>ringbuf_thr</i> register.

9.2.95 RINGBUF_CTRL register (Address 0xD2)

Table 108: RINGBUF_CTRL register

Addr: 0xD2		RINGBUF_CTRL		
Bit	Bit name	Default	Access	Bit description
7	<i>prx_event_clear</i>	0x00	PUSH	This is the proximity event clear register. By setting this bit to one the <i>prx_event_ready</i> flag is cleared.
6	<i>prx_event_ready</i>	0x00	RO	This is a ring-buffer status register which indicates that the ring buffer is filled and data is ready for readout. 0: No ring-buffer data not read 1: Ring-buffer data ready for readout
5:0	<i>ringbuf_thr</i>	0x20	R/W	In case the ring-buffer threshold interrupt is enabled in IRQ_ENABLE register and a proximity measurement threshold is reached this register defines how many measurement samples are written after the IRQ event to the ring buffer. The interrupt is released after the defined number of measurements are written to the FIFO. 0: 1 samples written to FIFO after IRQ release 1: 2 samples written to FIFO after IRQ release 2: 3 samples written to FIFO after IRQ release 3: 4 samples written to FIFO after IRQ release ... 32: 31 samples written to FIFO after IRQ release ... 63: 63 samples written to FIFO after IRQ release

9.2.96 SILICON_ID register (Address 0xED)

Table 109: SILICON_ID register

Addr: 0xED		SILICON_ID		
Bit	Bit name	Default	Access	Bit description
7:0	<i>silicon_id</i>	0xE2	RO	This is ams OSRAM silicon identification number of AS7100.

9.2.97 REVISION register (Address 0xEE)

Table 110: REVISION register

Addr: 0xEE		REVISION		
Bit	Bit name	Default	Access	Bit description
3:0	<i>rev_id</i>	0x01	RO	This is the revision identification number of AS7100. 0: Device version 1v0 1: Device version 2v0

9.2.98 CHIP_CTRL register (Address 0xEF)

Table 111: CHIP_CTRL register

Addr: 0xEF		CHIP_CTRL		
Bit	Bit name	Default	Access	Bit description
0	<i>chip_reset</i>	0x00	PUSHPOP	This is reset register for the device. Setting this register bit to one has the same effect like a power on reset. Once this function is used please mind that the startup timings become valid shown in Figure 19 and I2C communication will be interrupted during for a maximum of t_{I2C_READY} defined in Table 7. The register is set back to zero after device reset.

9.2.99 CONTROL register (Address 0xF0)

Table 112: CONTROL register

Addr: 0xF0		CONTROL		
Bit	Bit name	Default	Access	Bit description
6	<i>sync_en</i>	0x00	R/W	This is the control bit to enable a measurement start with the SYNC pin to in order to synchronize the measurement start with multiple devices. 0: Internal measurement trigger from on chip oscillator and configured sample time 1: Start measurement with external trigger on SYNC pin
5	<i>sync_edge</i>	0x00	R/W	This register selects the positive or negative edge control for the SYNC input pin. 0: Negative synchronization edge for SYNC pin 1: Positive synchronization edge for SYNC pin
4	<i>prx_en</i>	0x00	R/W	This is the enable register for the proximity measurement. 0: Proximity measurement disabled 1: Proximity measurement enabled
3	<i>ic_en</i>	0x00	R/W	This is the enable register for the IDAC calibration. 0: IDAC calibration disabled 1: IDAC calibration enabled
2	<i>cc_en</i>	0x00	R/W	This is the enable register for the coarse count calibration. 0: Coarse count calibration disables 1: Coarse count calibration enabled
1	<i>az_en</i>	0x00	R/W	This is the control register to enable the auto zero function. 0: Auto zero disabled 1: Auto zero enabled
0	<i>start</i>	0x00	R_PUSH	This register controls the automatic measurements sequencer for proximity and ambient light measurements. Setting this register to one starts the measurement sequencer. Once the register is read back it returns the actual state of the measurement sequencer and reports if the sequencer is running or stopped. 0: Measurement stopped 1: Measurement started

9.2.100 SYNC_DELAY_0 register (Address 0xF1)

Table 113: SYNC_DELAY_0 register

Addr: 0xF1		SYNC_DELAY_0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sync_delay[7:0]</i>	0x00	R/W	This is the lower byte of the 16-bit synchronization delay register for a measurement start via the SYNC input pin. The delay is calculated with the register value multiplied by a factor of 1.42857µs. In case the register is set to zero the synchronization delay is disabled. 0: 1.429 µs synchronization delay 1: 2.875 µs synchronization delay 2: 4.286 µs synchronization delay ... 65535: 93.621 ms synchronization delay

9.2.101 SYNC_DELAY_1 register (Address 0xF2)

Table 114: SYNC_DELAY_1 register

Addr: 0xF2		SYNC_DELAY_1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>sync_delay[15:8]</i>	0x00	R/W	This is the upper byte of the 16-bit synchronization delay register for a measurement start via the SYNC input pin. The delay is calculated with the register value multiplied by a factor of 1.42857µs. In case the register is set to zero the synchronization delay is disabled. 0: 1.429 µs synchronization delay 1: 2.875 µs synchronization delay 2: 4.286 µs synchronization delay ... 65535: 93.621 ms synchronization delay

9.2.102 WAKEUP_DELAY register (Address 0xF3)

Table 115: WAKEUP_DELAY register

Addr: 0xF3		WAKEUP_DELAY		
Bit	Bit name	Default	Access	Bit description
7:0	wakeup_delay	0xFF	R/W	This is the standby mode wakeup delay register. In case the standby mode is activated this register defines the time, prior to the actual measurement start, where all analog blocks get started for the proximity measurement. This setup time is calculated with the register value multiplied by a factor of 1.42857µs. In case the register is set to zero the synchronization delay is disabled. 0: 0 µs standby setup time 1: 1.429 µs standby setup time 2: 2.875 µs standby setup time 3: 4.286 µs standby setup time ... 255: 364.3µs standby setup time

9.2.103 STANDBY_EN register (Address 0xF4)

Table 116: STANDBY_EN register

Addr: 0xF4		STANDBY_EN		
Bit	Bit name	Default	Access	Bit description
7:0	standby_en	0x00	R/W	This is the standby enable register. Each bit inside this 8-bit register represents a individual block of AS7100 which can be power down during standby operation mode. In case a bit is set to one the related block is powered down during standby mode operation. Please refer to chapter 8.1 Operation modes for more details concerning the different device operation modes. Bit 0: ADC Modulators standby mode control Bit 1: LED voltage monitor standby mode control Bit 2: Voltage reference buffer standby mode control Bit 3: Voltage reference standby mode control Bit 4: Temperature sensor standby mode control

9.2.104 STATUS_MISC register (Address 0xF5)

Table 117: STATUS_MISC register

Addr: 0xF5		STATUS_MISC		
Bit	Bit name	Default	Access	Bit description
5	<i>status_fail_reg</i>	0x00	PUSHPOP	Status Input fail_reg Status of FIFO data read from RAM 00: FIFO data correct
4:3	<i>status_ram_ecc</i>	0x00	PUSHPOP	01: FIFO data with correctable Failure, 1-bit 10: FIFO data with not correctable Failure, >1-bit Note: Not all errors >1-bit can be detected!
2	<i>status_otp_crc8</i>	0x00	RO	This is the CRC status bit for the OTP memory. 0: CRC status ok 1: CRC status failure
1:0	<i>status_otp_ecc</i>	0x00	RO	This is the ECC register for the I ² C register Address. 00: I ² C Address correct 01: I ² C Address with correctable failure 10: I ² C Address with not correctable failure

9.2.105 STATUS_CNTRL register (Address 0xF6)

Table 118: STATUS_CNTRL register

Addr: 0xF6		STATUS_CNTRL		
Bit	Bit name	Default	Access	Bit description
2	<i>status_cntrl_mfreq</i>	0x00	PUSHPOP	This is the status register for the measurement frequency. 0: Measurement frequency ok 1: Measurement frequency too high for configured integration time $t_{\text{INTEGRATION}}$. Please increase measurement time t_{PERIOD} .
1	<i>status_cntrl_eom</i>	0x00	PUSHPOP	This is the status bit for the EoM (End of Measurement) indication. 0: Measurement on going 1: End of measurement
0	<i>status_cntrl_eoc</i>	0x00	PUSHPOP	This is the status bit for the End of Conversion. 0: Measurement on going 1: End of ADC conversion

9.2.106 STATUS_SAT register (Address 0xF7)

Table 119: STATUS_SAT register

Addr: 0xF7		STATUS_SAT		
Bit	Bit name	Default	Access	Bit description
6:4	<i>status_adc_sat</i>	0x00	PUSHPOP	This is the ADC saturation status register. The threshold for saturation can be configured with register MOD_ADC_LOW_SAT_LEVEL and MOD_ADC_HIGH_SAT_LEVEL. Bit 0: ADC 1 saturation Bit 1: ADC 2 saturation Bit 3: Temperature / VLED saturation
3:2	<i>status_pp_dsat</i>	0x00	PUSHPOP	This is the digital post processing saturation status register. Bit 0: Modulator 1 post processing saturation Bit 1: Modulator 2 post processing saturation
1:0	<i>status_mod_asat</i>	0x00	PUSHPOP	This is the analog modulator saturation status register. Bit 0: Modulator 1 analog saturation Bit 1: Modulator 2 analog saturation

9.2.107 STATUS_PRX register (Address 0xF8)

Table 120: STATUS_PRX register

Addr: 0xF8		STATUS_PRX		
Bit	Bit name	Default	Access	Bit description
6	<i>status_prx_high_on</i>	0x00	PUSHPOP	This is the proximity interrupt status register for the high proximity detection. 0: No proximity event occurred 1: Change of <i>status_prx_high</i> bit from 0 to 1
5	<i>status_prx_high_off</i>	0x00	PUSHPOP	This is the proximity interrupt status register for the high proximity detection. 0: No proximity event occurred 1: Change of <i>status_prx_high</i> bit from 1 to 0
4	<i>status_prx_high</i>	0x00	RO	This is a proximity detection high status register. This register is not linked to an interrupt register. It provides only information about the proximity position. 0: Proximity value $\leq$ Proximity threshold high 1: Proximity value $>$ Proximity threshold low
2	<i>status_prx_low_on</i>	0x00	PUSHPOP	This is the proximity interrupt status register for the low proximity detection. 0: No proximity event occurred 1: Change of <i>status_prx_low</i> bit from 0 to 1
1	<i>status_prx_low_off</i>	0x00	PUSHPOP	This is the proximity interrupt status register for the low proximity detection. 0: No proximity event occurred 1: Change of <i>status_prx_low</i> bit from 1 to 0
0	<i>status_prx_low</i>	0x00	RO	This is a proximity detection low status register. This register is not linked to an interrupt register. It provides only information about the proximity position. 0: Proximity value $\geq$ Proximity threshold low 1: Proximity value $<$ Proximity threshold low

9.2.108 STATUS register (Address 0xF9)

Table 121: STATUS register

Addr: 0xF9		STATUS		
Bit	Bit name	Default	Access	Bit description
7	<i>irq_rb_ready</i>	0x00	PUSHPOP	This is the ring buffer interrupt register. This register is cleared automatically after readout. Please mind that this bit is only triggered when <i>irq_en_rb_ready</i> = 1 and <i>fifo_ringbuffer_stop</i> = 1. If these bits are not set interrupt will not be raised and FIFO data will be overwritten. 0: No ring buffer ready event 1: Ring buffer ready interrupt event
6	<i>irq_misc</i>	0x00	RO	This is the miscellaneous interrupt register. Please refer to STATUS_MISC register to determine which interrupt got released. In order to delete the <i>irq_misc</i> interrupt the STATUS_MISC register must be read if <i>irq_clear_sel</i> = 0 or write a 1 on bit position if <i>irq_clear_sel</i> = 1. 0: No miscellaneous event 1: Miscellaneous interrupt event
5	<i>irq_ovtemp</i>	0x00	PUSHPOP	This is the overtemperature interrupt register. This register is cleared automatically after readout. 0: No overtemperature event 1: Overtemperature interrupt event
4	<i>irq_sat</i>	0x00	RO	This is the ADC saturation interrupt register. Please refer to STATUS_SAT register to determine which interrupt got released. In order to delete the <i>irq_sat</i> interrupt the STATUS_SAT register must be read if <i>irq_clear_sel</i> = 0 or write a 1 on bit position if <i>irq_clear_sel</i> = 1. 0: No ADC saturation event 1: ADC saturation interrupt event
3	<i>irq_prx</i>	0x00	RO	This is the proximity interrupt register. Please refer to STATUS_PRX register to determine which interrupt got released. In order to delete the <i>irq_prx</i> interrupt the STATUS_PRX register must be read if <i>irq_clear_sel</i> = 0 or write a 1 on bit position if <i>irq_clear_sel</i> = 1. 0: No proximity IRQ event 1: Proximity IRQ event
2	<i>irq_fifo_overflow</i>	0x00	PUSHPOP	This is the FIFO overflow interrupt registers. This register is cleared automatically after readout. 0: No FIFO overflow 1: FIFO overflow; samples lost
1	<i>irq_fifo_threshold</i>	0x00	RO	This is the interrupt register for the FIFO threshold. This interrupt cannot be deleted manually. Interrupt can only be deleted by lowering the FIFO level.

Addr: 0xF9		STATUS		
Bit	Bit name	Default	Access	Bit description
				0: No FIFO threshold interrupt active 1: FIFO threshold interrupt active
0	<i>irq_cntrl</i>	0x00	RO	This is the interrupt control status register. Please refer to STATUS_CNTRL register to determine which interrupt got released. In order to delete the <i>irq_cntrl</i> interrupt the STATUS_CNTRL register must be read if <i>irq_clear_sel</i> = 0 or write a 1 on bit position if <i>irq_clear_sel</i> = 1. 0: Control interrupt not active 1: Control interrupt active

9.2.109 FIFO_LEVEL0 register (Address 0xFA)

Table 122: FIFO_LEVEL0 register

Addr: 0xFA		FIFO_LEVEL0		
Bit	Bit name	Default	Access	Bit description
6:0	<i>fifo_level</i>	0x00	RO	This is the FIFO fill level register.

9.2.110 FIFO_LEVEL1 register (Address 0xFB)

Table 123: FIFO_LEVEL1 register

Addr: 0xFB		FIFO_LEVEL1		
Bit	Bit name	Default	Access	Bit description
3	<i>fifo_empty</i>	0x01	RO	This is the FIFO empty register which is set to one in case the FIFO is empty. 0: FIFO contains data 1: FIFO empty
2	<i>fifo_full</i>	0x00	RO	This is the FIFO full register which is set to one in case the FIFO is full. 0: FIFO not full 1: FIFO full
1	<i>fifo_overflow</i>	0x00	RO	This is the FIFO overflow register which is set to one in case a FIFO overflow has occurred. 0: No FIFO overflow 1: FIFO overflow

9.2.111 FIFO0 register (Address 0xFC)

A FIFO entry (word, 32 bits) can be read with individual read accesses, means 4 consecutive I²C addresses (*fifo_readmode* = 1) starting with **FIFO0**, then **FIFO1**, **FIFO2**, and **FIFO3** or with a burst read accesses of 4*n bytes for n FIFO entries. If a burst mode read of multiple data words is executed, please mind that for **FIFO0** register the I²C register auto increment function shows a special behavior to support seamless readout of the FIFO data. This means after a burst reading of 4 data words reflecting **FIFO0** – **FIFO3** register the internal I²C address pointer is set back to **FIFO0** register to continue readout of the next data word without the need to set the I²C read address back to **FIFO0**. If you read out beyond the end of FIFO SIZE the last FIFO entry will be repeated. There is no underflow flag available. The FIFO SIZE is 64 entries (words). When reading Address from **FIFO0** register the whole FIFO entry (word) is read and captured from FIFO and the FIFO level decrements by 1.

Table 124: FIFO0 register

Addr: 0xFC		FIFO0		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifo0</i>	0x01	RO	This is the low byte of the FIFO which contains the start Address for FIFO burst read.

9.2.112 FIFO1 register (Address 0xFD)

Table 125: FIFO1 register

Addr: 0xFD		FIFO1		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifo1</i>	0x01	RO	This is the middle low byte of the FIFO memory.

9.2.113 FIFO2 register (Address 0xFE)

Table 126: FIFO2 register

Addr: 0xFE		FIFO2		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifo2</i>	0x01	RO	This is the middle high byte of the FIFO memory.

9.2.114 FIFO3 register (Address 0xFF)

Table 127: FIFO3 register

Addr: 0xFF		FIFO3		
Bit	Bit name	Default	Access	Bit description
7:0	<i>fifo3</i>	0x01	RO	This is the high byte low of the FIFO memory.

10 Application information

This chapter provides application related information like different reference schematics for various application use cases as well as an overview of recommended external components. It is also highly recommended to consult the ams OSRAM application support team for circuit diagram and layout review during the customer product development design process to guarantee highest system performance.

10.1 Schematic

The schematic circuit shown in Figure 55 represents a simplified schematic of a force button integration into an automotive product. The SBC circuit U3 is used for vehicle LIN bus communication and provides the V_{VDD33} supply voltage which is typically 3.3V to AS7100 as well as the host MCU U2. Please refer to chapter 5 Electrical characteristics to get details on the full supply voltage range of AS7100.

The I²C communication interface as well as the INT pin of AS7100 are open drain outputs and do require external pull up resistors R_{I2C_PU} and R_{INT_PU} for proper operation of the device. The SYNC pin can be connected to ground in case the external synchronization function of the device is not used.

The EN pin which is used to power up AS7100 is an active high pin and it is recommended to have a weak external pull-down resistor R_{EN_PD} to avoid startup of the device during power up phase of the electrical circuit. Alternatively, it is also possible to select a GPIO pad of the host MCU which has in reset state of the MCU an internal pull-down resistor R_{GPIO_PD} enabled to pull the EN pin low during device startup. Once the MCU is powered up the internal pull down can be disabled and the pin is driven high with a push pull output to enable AS7100. Disabling the internal pull-down resistor helps to reduce unwanted pull-down leakage currents while AS7100 is enabled but is certainly not mandatory.

The application circuit shown in Figure 56 shows the integration of two AS7100 which are synchronized via SYNC pin to its host MCU. The synchronization allows to trigger the measurement start of both devices at the very same time. The I²C interface voltage in this example was selected with 1.8V while AS7100 is supplied via 3.3V with a linear regulator.



CAUTION:

Communication interface voltage depends on device ordering code. Please make sure you use the correct device ordering code to support 3.3V or 1.8V compliant I²C interface voltage. Correct ordering codes can be found in chapter 2 Ordering information.

Figure 55: Application circuit automotive LIN bus force button integration with $V_{IOVDD} = 3.3V$

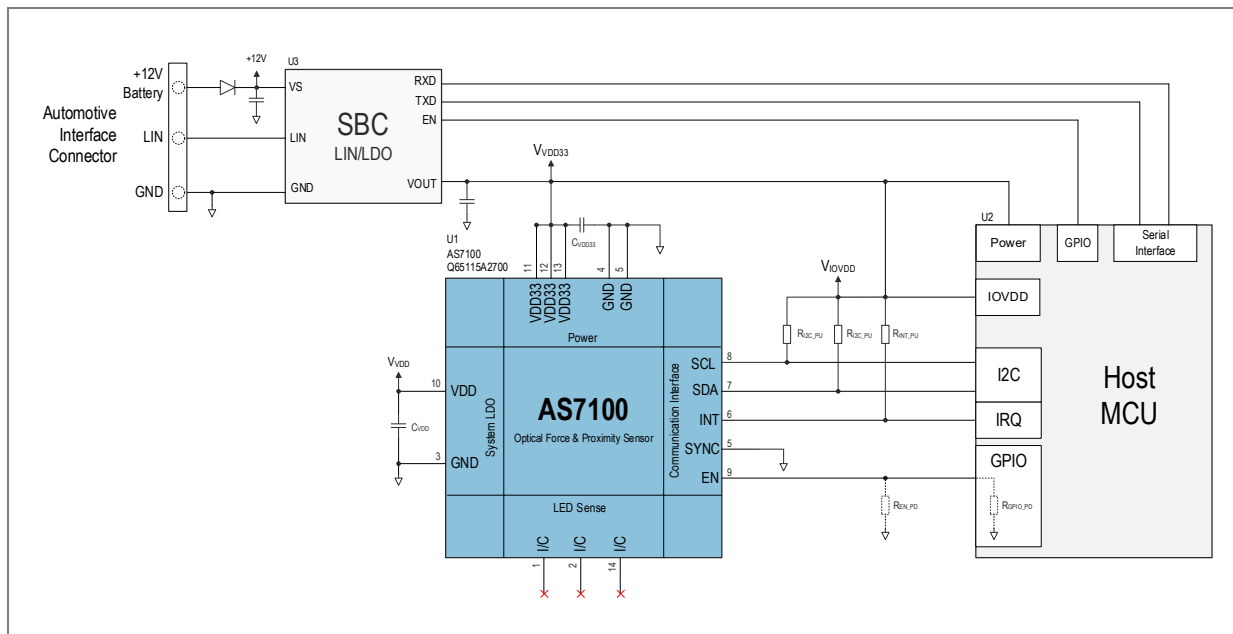
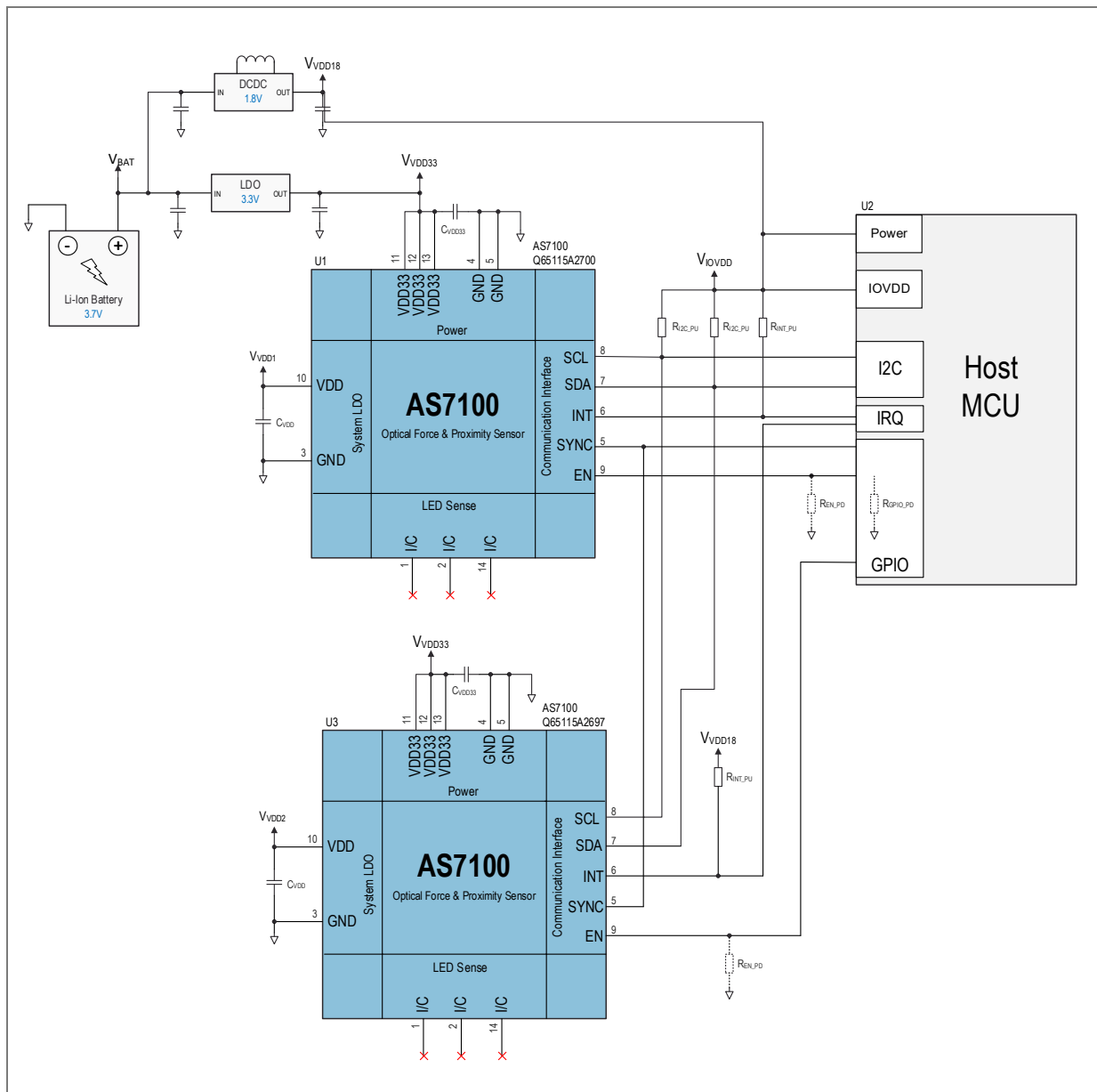


Figure 56: Application circuit with two AS7100 and external MCU synchronization



10.2 External components

This chapter provides recommended external components, for the example schematics shown in chapter 10.1.

Table 128: External components - capacitors

Symbol	Parameter	Operating temperature	Min. rated voltage	Max. tolerance	Recommended typ. value
C _{VDD33}	Input capacitor for VDD33 ⁽¹⁾ pin	-55°C to 150°C	4 V	±10%	1 µF
C _{VDD}	LDO output capacitor for VDD ⁽²⁾ pin	-55°C to 150°C	4 V	±10%	100 nF

(1) Place C_{VDD33} as close as possible to the VDD33 pin.

(2) Place C_{VDD} as close as possible to the VDD pin.

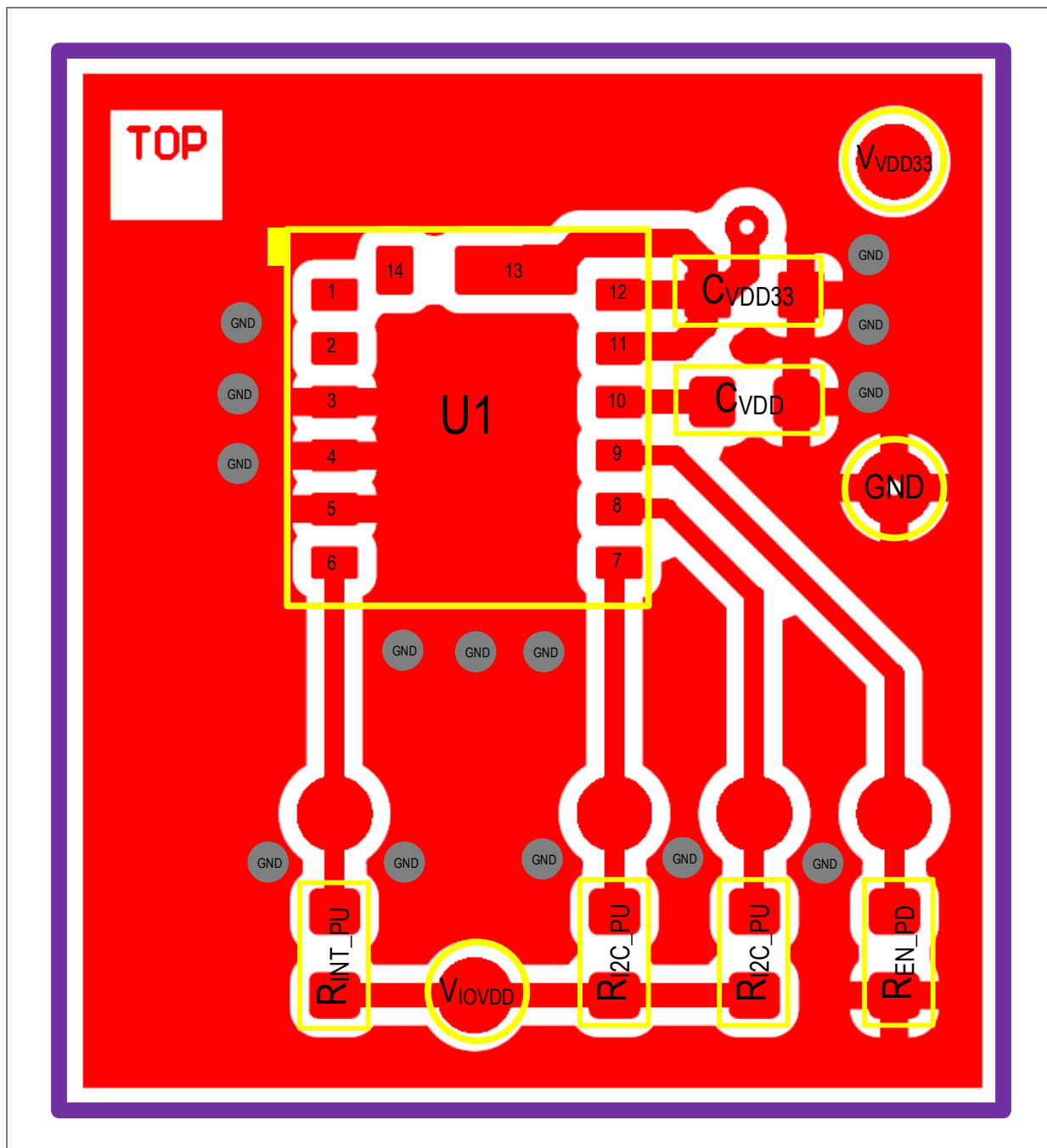
Table 129: External components - resistors

Symbol	Parameter	Min. power dissipation	Max. tolerance	Min. / Max. nominal resistance	Recommended typ. value
R _{I2C_PU}	I ² C bus pull up resistors	0.03 W	±10%	1 kΩ / 47 kΩ	10 kΩ ⁽¹⁾
R _{INT_PU}	INT pin pull up resistor	0.03 W	±10%	1 kΩ / 100 kΩ	47 kΩ
R _{EN_PD}	EN pin pull down resistor	0.03 W	±10%	100 kΩ / 1 MΩ	570 kΩ

(1) The value of the I²C pull up resistors (R_{I2C_PU}) should be based on the bus voltage, system bus speed and trace capacitance.

10.3 PCB layout

Figure 57: AS7100 recommended PCB layout

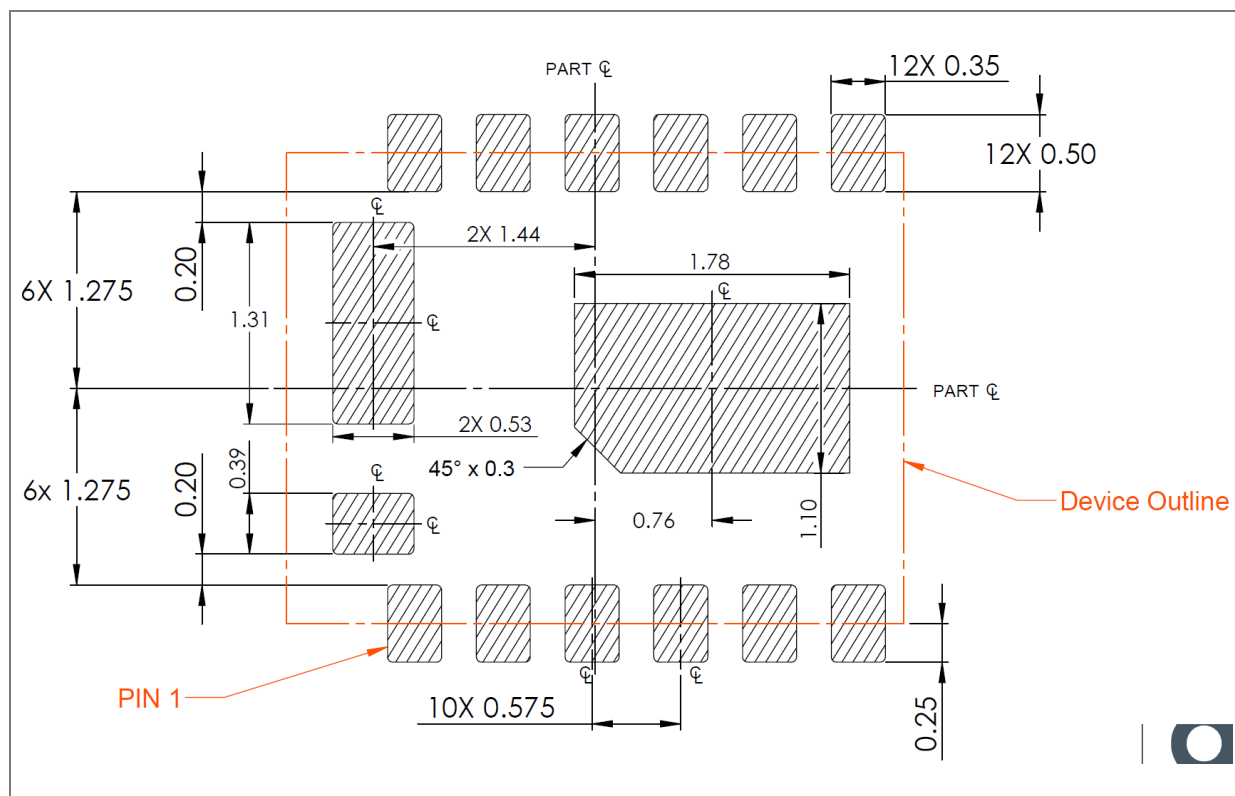


- (1) The placement of the decoupling capacitors is critical. Place the components on the same side of PCB as device as shown in Figure 57 above. Make connections as close as possible to minimize series inductance and resistance.
- (2) All ground vias must be connected to a solid ground plane.

10.4 PCB pad layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

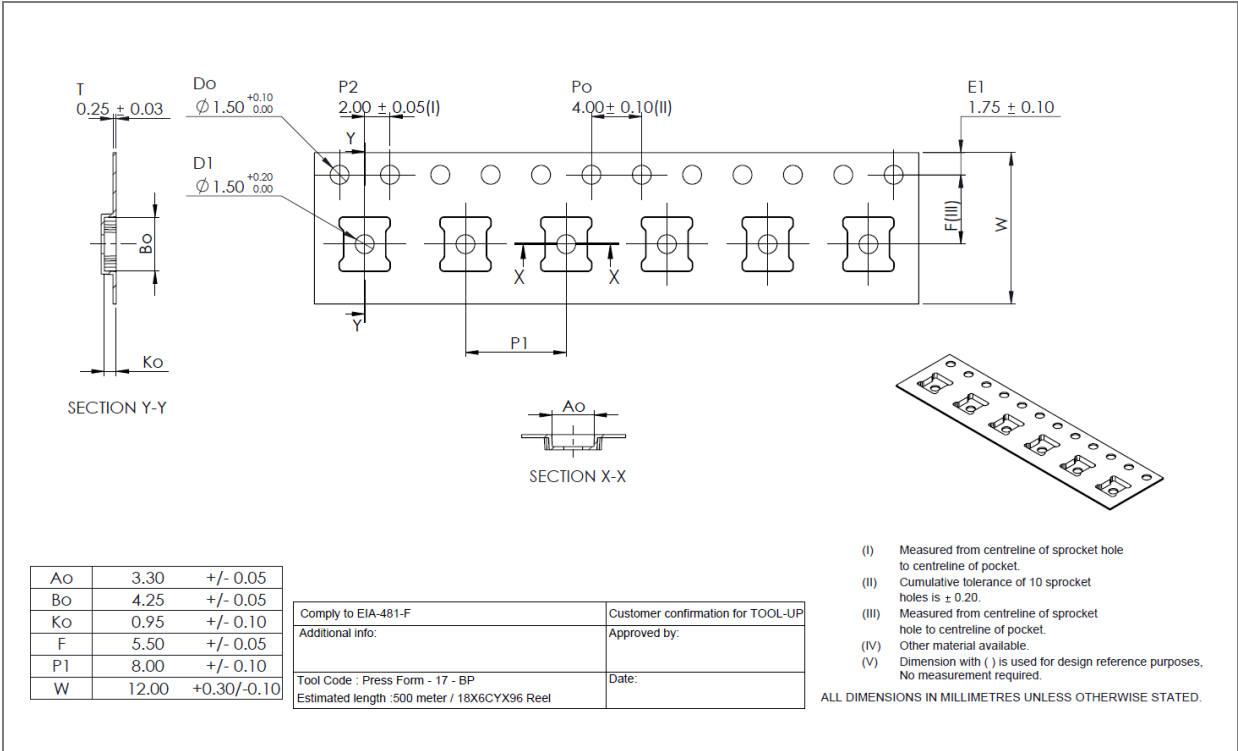
Figure 58: Recommended PCB pad layout



- (1) All dimensions are in millimeters.
- (2) Dimensioning and tolerancing are $\pm 0.05\text{mm}$ unless otherwise noted.
- (3) This drawing is subject to change without notice.

12 Tape & reel information

Figure 60: Tape and reel mechanical drawing



- (1) All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
- (2) The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
- (3) Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001
- (4) ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
- (5) In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
- (6) This drawing is subject to change without notice.

13 Storage information

13.1 Moisture sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

13.2 Shelf life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf life: 24 months
- Ambient temperature: <40°C
- Relative humidity: <90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

13.3 Floor life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor life: 168 hours
- Ambient temperature: <30°C
- Relative humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

13.4 Rebaking instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

14 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade

Other definitions

Draft / Preliminary:
The draft / preliminary status of a document indicates that the content is still under internal review and subject to change without notice. ams-OSRAM AG does not give any warranties as to the accuracy or completeness of information included in a draft / preliminary version of a document and shall have no liability for the consequences of use of such information.

Short datasheet:
A short datasheet is intended for quick reference only, it is an extract from a full datasheet with the same product number(s) and title. For detailed and full information always see the relevant full datasheet. In case of any inconsistency or conflict with the short datasheet, the full datasheet shall prevail.

Changes from previous released version to current revision v3-00	Page
Document security class is updated "PUBLIC" in the footer	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal information

Copyright & disclaimer

Copyright ams-OSRAM AG, Tobelbader Strasse 30, 8141 Premstaetten, Austria-Europe. Trademarks Registered. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

Devices sold by ams-OSRAM AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams-OSRAM AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams-OSRAM AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams-OSRAM AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams-OSRAM AG for each application. This product is provided by ams-OSRAM AG "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams-OSRAM AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams-OSRAM AG rendering of technical or other services.

Product and functional safety devices/applications or medical devices/applications:

ams-OSRAM AG components are not developed, constructed or tested for the application as safety relevant component or for the application in medical devices. ams-OSRAM AG products are not qualified at module and system level for such application.

In case buyer – or customer supplied by buyer – considers using ams-OSRAM AG components in product safety devices/applications or medical devices/applications, buyer and/or customer has to inform the local sales partner of ams-OSRAM AG immediately and ams-OSRAM AG and buyer and/or customer will analyze and coordinate the customer-specific request between ams-OSRAM AG and buyer and/or customer.

ams OSRAM RoHS and REACH compliance statements for semiconductor products

RoHS compliant: The term "RoHS compliant" means that semiconductor products from ams OSRAM fully comply with current RoHS directives, and China RoHS. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment [EU2015/863](#)) above the defined threshold limit in the Annex II.

REACH compliant: Semiconductor products from ams OSRAM are free of Substances of Very High Concern (SVHC) according Article 33 of the [REACH Regulation 2006/1907/EC](#); please refer to the Candidate List of Substances of ECHA [here](#).

Important information: The information provided in this statement represents ams OSRAM knowledge and belief as of the date that it is provided. ams OSRAM bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. We are undertaking efforts to better integrate information from third parties. ams OSRAM has taken and will continue to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams OSRAM and its suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Headquarters

ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

Please visit our website at ams-osram.com

For information about our products go to [Products](#)

For technical support use our [Technical Support Form](#)

For feedback about this document use [Document Feedback](#)

For sales offices and branches go to [Sales Offices / Branches](#)

For distributors and sales representatives go to [Channel Partners](#)