AS8580

Datasheet

Published by ams-OSRAM AG
Tobelbader Strasse 30, 8141 Premstaetten, Austria
Phone +43 3136 500-0
ams-osram.com

Table of contents

1 General description 5
1.1 Key benefits & features 6
1.2 Application example 6
1.3 Block diagram 7

2 Ordering information 8

3 Package 8
3.1 Pin description 9

4 Absolute maximum ratings (non-operating) 10

5 Electrical characteristics 11
5.1 Operating conditions 11
5.2 DC/AC characteristics for inputs and outputs 12
5.3 Internal ESD protection concept 14

6 Functional description 16
6.1 Operation modes overview 17
6.2 Generate trigger mode 19
6.3 Wait mode 19
6.4 Initialization mode 19
6.5 Single measurement mode 20
6.6 Continuous measurement mode 22
6.7 Polling measurement mode 24
6.8 Low power mode 27
6.9 Diagnostic modes 27
6.10 Diagnostic features 29
6.11 Measurement sequence with configuration tables 30
6.12 Chip ID 31
6.13 SPI interface 31
6.14 SPI timing characteristics 34

7 Detailed system and block specification 35
7.1 System timing 35

7.2 System parameters 36
7.3 PLL 37
7.4 TX sine DAC / filter 38
7.5 TX driver and current sensing 38
7.6 TX multiplexer 38
7.7 Trans impedance amplifier 38
7.8 Band pass filter / pre-amplifier 39
7.9 Demodulation 39
7.10 Low pass filter 39
7.11 Offset comp: Programmable gain amplifier 39
7.12 ADC 39
7.13 Voltage regulators 40
7.14 Supply monitor 40

8 SW interface 41
8.1 MEMT_DATA_1-16 (Address 0x00-0x0F, all banks) 42
8.2 BANK_SEL (Address 0x10, all banks) 43
8.3 MEMT_SEQ (Address 0x11, bank 0) 44
8.4 MEMT_CNTL_1 (Address 0x12, bank 0) 45
8.5 MEMT_CNTL_2 (Address 0x13, bank 0) 47
8.6 MEMT_CNTL_3 (Address 0x14, bank 0) 48
8.7 POLL_CYC_CNT (Address 0x15, bank 0) 49
8.8 POLL_CYC_CNT_STS (Address 0x16, bank 0) 49
8.9 RAM_CFG_TBL_CRC (Address 0x17, bank 0) 50
8.10 TBL_CRC_CHK_TSLD (Address 0x18, bank 0) 50
8.11 DIAG_REG_1 (Address 0x19, bank 0) 51
8.12 DIAG_REG_2 (Address 0x1A, bank 0) 52
8.13 DIAG_REG_3 (Address 0x1B, bank 0) 53
8.14 MEMT_CFG1_TBLX (Address 0x11, bank 1-16) 54
8.15 MEMT_CFG2_TBLX (Address 0x12, bank 1-16) 55
8.16 MEMT_CFG3_TBLX (Address 0x13, bank 1-16) 57
8.17 MEMT_CFG4_TBLX (Address 0x14, bank 1-16) 58
8.18 MEMT_CFG5_TBLX (Address 0x15, bank 1-16) 58
8.19 MEMT_CFG6_TBLX (Address 0x16, bank 1-16) 59
8.20 MEMT_CFG7_TBLX (Address 0x17, bank 1-16) 60
8.21 OTP (Address 0x17-0x1F, bank 17) 60

9 Application information 61

10 Package drawings & markings 62

11 Revision information 64

12 Legal information 65

AS8580 Capacitive sensor

1 General description

AS8580 is a capacitive sensor detecting the change of capacitance in different applications. The capacitive sensor measures the relative change of capacitance. This can be used for capacitive touch applications, proximity or human presence detection, fluid level and quality measurements as well as many other applications.

AS8580 captures the sinusoidal current response caused by a forced sinusoidal voltage. Based on that, the change of capacitance in various applications can be detected. Besides capacitive changes, the resistive component in various applications can be detected as well.

This can be useful e.g. to determine/compensate (environmental) disturbances such as moisture, which changes a parallel resistive component along with a change in capacitance.

This high precision performance sensor also supports a multitude of diagnostic features that meet standard ASIL B functional safety requirements.

The capacitive sensing IC is specifically designed to work under high electromagnetic disturbances (EMC) due to adjustable frequencies.

AS8580 has a SPI Interface for reading measurement values and configuration.

It is available in TSSOP-14 package and operates with 5V.

1.1 Key benefits & features

The benefits and features of AS8580, Capacitive sensor are listed below:

Table 1: Added value of using AS8580

Benefits	Features
Very accurate capacitive measurement with excellent sensitivity	Separation of resistive and capacitive components of measured impedance
Touchless and wear free technology	Four independent measurement lines.
Outstanding quality and high durability at lower system costs	Long term delivery and quality due to ams OSRAM own production site in central Europe
Enabler for safety critical applications	Functional safety ASIL B according ISO26262
Suitable for automotive environment	AEC-Q100 Grade 1 qualified

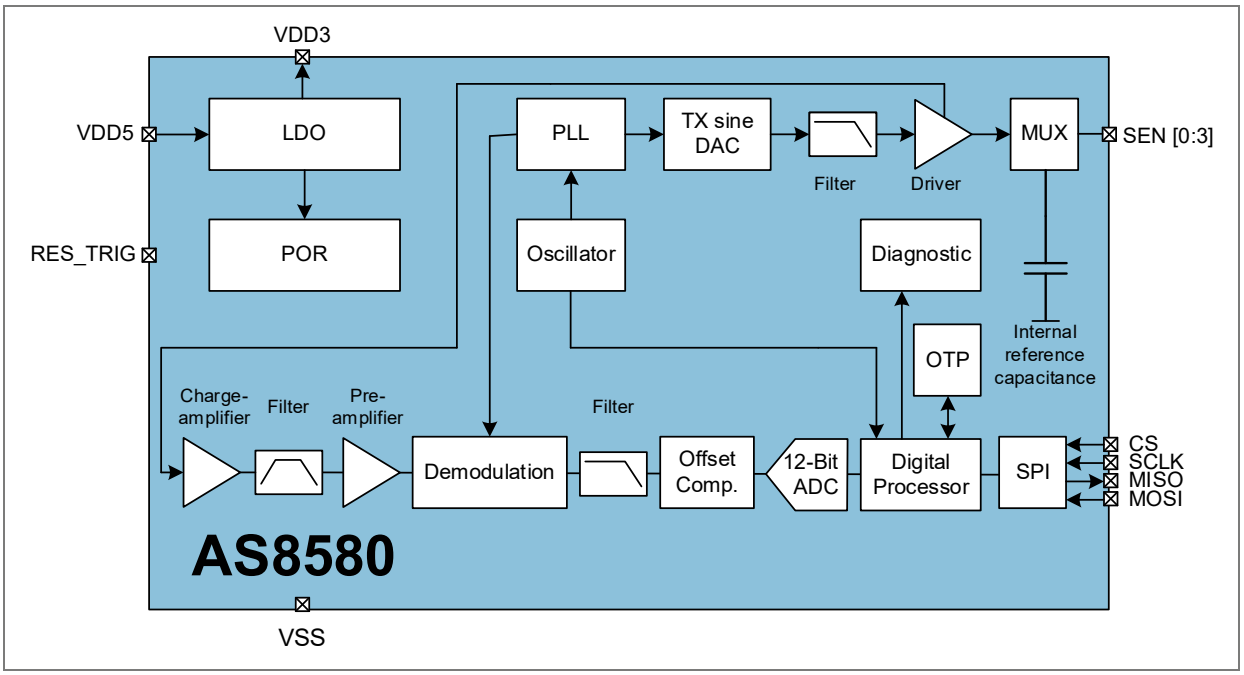
1.2 Application example

- Autonomous driving applications, e.g.: Hands on steering wheel detection
- Automotive door handle / trunk opening applications
- Human presence detection for automotive and non-automotive applications
- Sensing of fluid level and quality in vehicles as well as industrial applications

1.3 Block diagram

The functional blocks of this device are shown below in Figure 1:

Figure 1: Functional blocks of AS8580

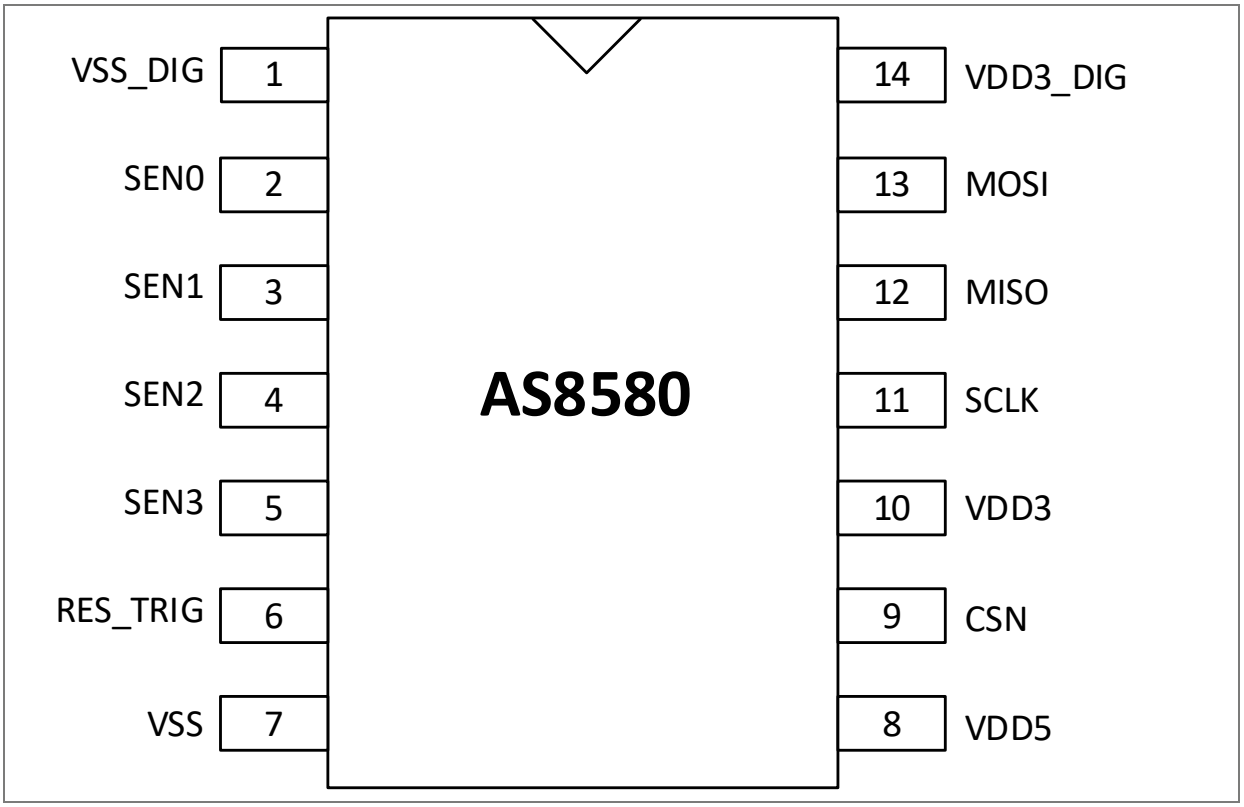


2 Ordering information

Product type	Ordering code	Package	Marking	Delivery form	Delivery quantity
AS8580-ATST	Q65113A8911	TSSOP14	AS8580	Tape & reel	4,500 pcs/reel
AS8580-ATSM	Q65115A1258	TSSOP14	AS8580	Tape & reel	500 pcs/reel

3 Package

Figure 2: Plastic package TSSOP14



3.1 Pin description

Table 2: Pin description of AS8580

Pin number	Pin name	Pin description	Pin type(1)	Notes
1	VSS_DIG	Digital ground	S	
2	SEN0	Driver output	AIO	
3	SEN1	Driver output	AIO	
4	SEN2	Driver output	AIO	
5	SEN3	Driver output	AIO	
6	RES_TRIG	Reset/trigger & Trigger mode indicator	DIO_PUOD	
7	VSS	Analog ground	S	
8	VDD5	5V power supply	S	
9	CSN	SPI chip select	DI_SPU	Selectable pull-up
10	VDD3	3.3V regulated output	S	
11	SCLK	SPI clock	DI_S	
12	MISO	SPI data out	DO_T	
13	MOSI	SPI data in	DI_S	
14	VDD3_DIG	3.3V regulated output, for digital blocks	S	

(1)
S	Supply
AIO	Analog I/O
DI_S	Digital input with Schmitt-trigger
DI_SPU	Digital input with Schmitt-trigger and pull-up
DO_T	Digital output / tri-state
DIO_PUOD	Digital input-output with pull-up / open drain

4 Absolute maximum ratings (non-operating)

Stresses beyond those listed under “Absolute maximum ratings (non-operating)” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Electrical Characteristics.

“Operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS8580

Parameter	Symbol	Min	Max	Unit	Note
DC supply voltage	VDD5	-0.3	7	V	Referenced to VSS
Internal DC supply voltage	VDD3 VDD3_DIG	-0.3	5	V	Referenced to VSS Referenced to VSS_DIG
Difference between VSS-pins	ΔVSS	-0.3	0.3	V	VSS-VSS_DIG
Analog IO-pin voltage	VAIO	-0.3	VDD5+0.3	V	Referenced to VSS
Digital IO-pin voltage	VDIO	-0.3	VDD5+0.3	V	Referenced to VSS_DIG
Input current (latch-up immunity)	I_SCR	-100	100	mA	AEC-Q100-004
Electrostatic discharge human body model	ESD_H1	±4		kV	AEC-Q100-002 SENX pins
Electrostatic discharge human body model	ESD_H2	±2		kV	AEC-Q100-002 All other pins
Storage temperature	TEMP_STRG	-55	150	°C	
Package body temperature	TEMP_BODY		260	°C	IPC/JEDEC J-STD-020(1)(2)
Moisture sensitivity level	MSL	3			ICP/JEDEC J-STD-033

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020C “Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices”.
(2) The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn).

5 Electrical characteristics

5.1 Operating conditions

Operating range defines the limits for functional operation and parametric characteristics of the device. The functionality of the sensor outside the operating range described in this section is not guaranteed. If not differently reported all values in the table below refer to the complete temperature range.

Table 4: Operating conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
DC supply voltage	VDD5	4.5	5	5.5	V	Ramp-up time from 0 to 2.5V must be less than 20msec Referenced to VSS
Digital DC supply voltage	VDD3_DIG	3	3.3	3.6	V	Referenced to VSS_DIG, internally generated
Analog DC supply voltage	VDD3	3	3.3	3.6	V	Referenced to VSS, internally generated
Negative supply voltage, analog, digital	VSS VSS_DIG		0		V	VSS-VSS_DIG is the reference for all other nodes
Difference between VSS-pins	ΔVSS		0		V	VSS and VSS_DIG must be connected together on PCB in all applications
Supply current during measurement	IDD_MEAS		16		mA	With external electrode enabled.
Average supply current in polling mode (see conditions)	IDD_POLL		105		µA	60µs settling, 36ms period, 2 electrodes enabled, accumulation 2 values, room temperature, 5V supply.
Power save supply current	IDD_PS			20	µA	In polling mode, after measurement completion. Room temperature
				50	µA	Full temperature range
Supply current in wait mode	IDD_WAIT		1		mA	
Ambient temperature	TEMP_AMB	-40		125	°C	

5.2 DC/AC characteristics for inputs and outputs

5.2.1 Analog in- and outputs

Table 5: CMOS in-/output, pin type: AIO (pins: SEN0-SEN3)

Parameter	Symbol	Min	Max	Unit	Note
Input leakage current	I_LEAK		10	µA	
Input capacitance	C_IN		10	pF	Info parameter(1)

(1) Info Parameters are not pass/fail parameters in production where limits are calculated from simulation and characterization.

5.2.2 Digital inputs

Table 6: CMOS digital input with Schmitt-trigger, pin type: DI_S (pins: MOSI, SCLK, CSN)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_IH	0.7 * VDD5		V	
Low level input voltage	V_IL		0.3 * VDD5	V	
Negative-going threshold	VT_N	1.9	2.4	V	VDD5 = 5.5V
Positive-going threshold	VT_P	3	3.5	V	VDD5 = 5.5V
Input leakage current	I_LEAK	-1	1	µA	V_IH = 5.5V
Pull-up current (pins: CSN)	I_PU	-250	-50	µA	V_IL = 0.0V

5.2.3 Digital outputs

Table 7: CMOS digital output tri-state, pin type: DO_T (pins: MISO)

Parameter	Symbol	Min	Max	Unit	Note
High level output voltage	V_OH	VDD5 - 0.5		V	
Low level output voltage	V_OL		VSS + 0.4	V	
Output drive strength	I_OH		1	mA	VDD5 = 4.5V
Output drive strength	I_OL		1	mA	VDD5 = 4.5V
Tri-state leakage current	I_OZ	-10	10	µA	To VSS

Table 8: CMOS digital input-output open drain with pull-up, pin type: DIO_PUOD (pins: RES_TRIG)

Parameter	Symbol	Min	Max	Unit	Note
High level input voltage	V_IH	0.7 * VDD5		V	
Low level input voltage	V_IL		0.3 * VDD5	V	
Low level output voltage	V_OL		VSS + 0.4	V	
Output drive strength	I_OL		4	mA	VDD5 = 4.5V
Tri-state leakage current	I_OZ	-10	10	µA	To VSS
Pull-up resistance	R_PU	6	15	kΩ	

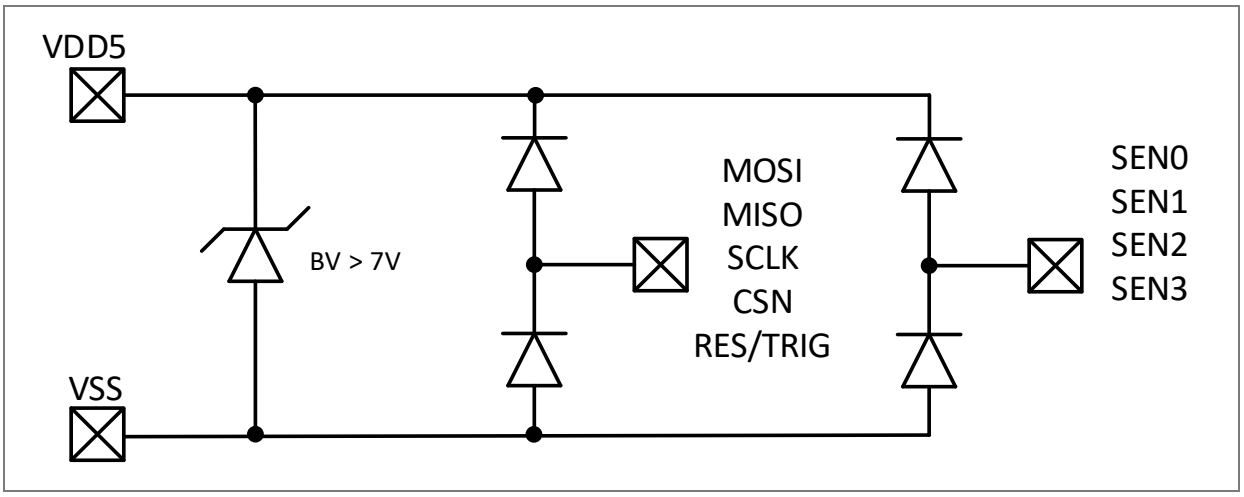
5.3 Internal ESD protection concept

VSS supply domain

VSS and VSS_DIG must be connected together in all applications.

VDD5 supply domain

Figure 3: ESD protection circuit on VDD5 domain



3.3V supply domains

Figure 4: ESD protection circuit on VDD3 domain

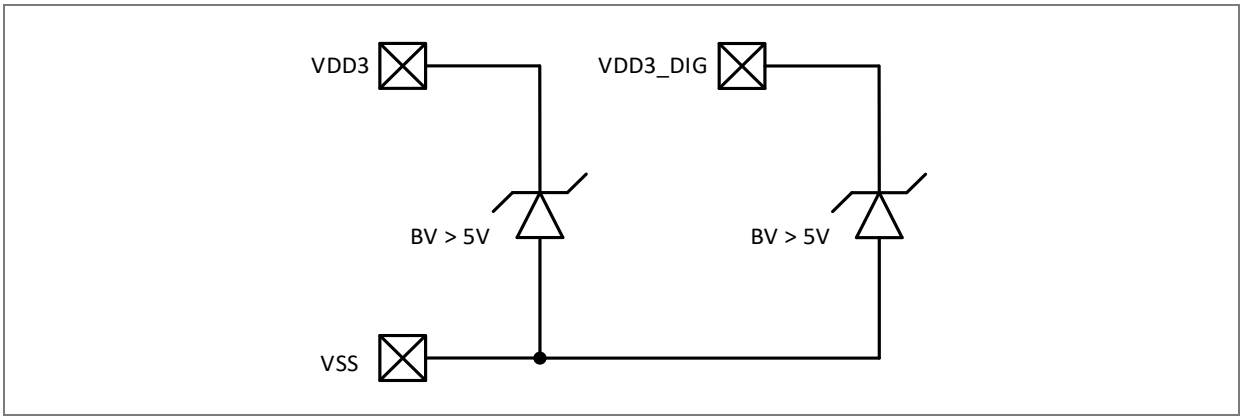


Table 9: ESD protection on VDD5 domain

Parameter	Min	Max	Unit	Note
Positive ESD clamp voltage	7		V	Info parameter(1)
Positive ESD protection leakage current		1	µA	0<V<7 T=25°C Info parameter(1)

(1) Info Parameters are not pass/fail parameters in production where limits are calculated from simulation and characterization

Table 10: ESD protection on VDD3 and VDD3_DIG domains

Parameter	Min	Max	Unit	Note
Positive ESD clamp voltage	5		V	Info parameter(1)
Positive ESD protection leakage current		1	µA	0<V<5 T=25°C Info parameter(1)

(1) Info Parameters are not pass/fail parameters in production where limits are calculated from simulation and characterization

6 Functional description

The purpose of this sensor is to measure a sensor capacitance at four pins, SEN0 to SEN3.

The measurement is realized with a transceiver architecture operating between 5MHz and 20MHz. In short, the transmitter forces a sine wave voltage across the load to measure; and the receiver detects the current response of the load. The current response is converted to a voltage and then demodulated; this is then filtered and converted in 12-bit digital words; it is possible to accumulate the digital words for noise reduction. The architecture allows the detection of not only capacitive changes, but also of changes due to environmental factors such as moisture, which adds a parallel resistive component along with a change in capacitance.

The response can be measured on any of the 4 SEN pins connected to the sensor driver through an analog multiplexer. The carrier frequency of 5-20MHz is generated by a PLL frequency synthesizer; an optional spread spectrum function varies the frequency of the carrier signal in order to reduce the emission level by spreading the RF energy over a broader band.

6.1 Operation modes overview

The device can operate in different modes: Initialization, single measurement, continuous measurement, polling measurement, diagnostic, and low power modes.

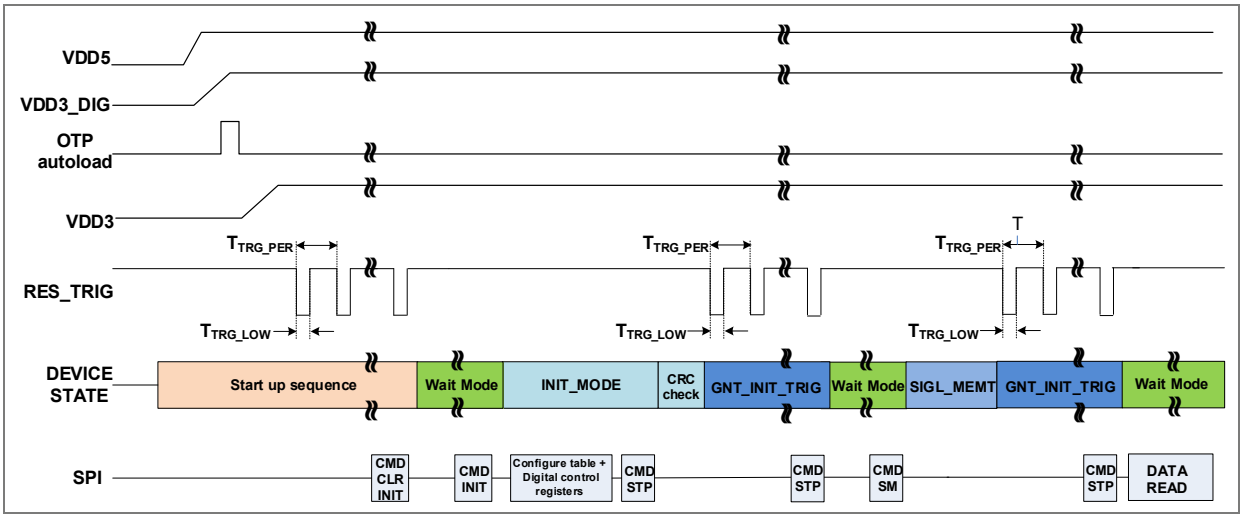
Once the voltage at VDD3_DIG crosses the POR release threshold the digital control logic starts functioning; the NOT_INIT bit in the diagnostic register is set; the OTP contents are loaded and the VDD3 LDO is turned on. Once the voltage at VDD3 crosses the POR release threshold the device completes the startup sequence and starts generating a trigger pulse on RES_TRIG.

The device remains in this state until it receives a CLEAR_NOT_INIT command; no other command will be accepted in this phase.

At any time, a low pulse on RES_TRIG of at least TRST_LOW will reset the device.

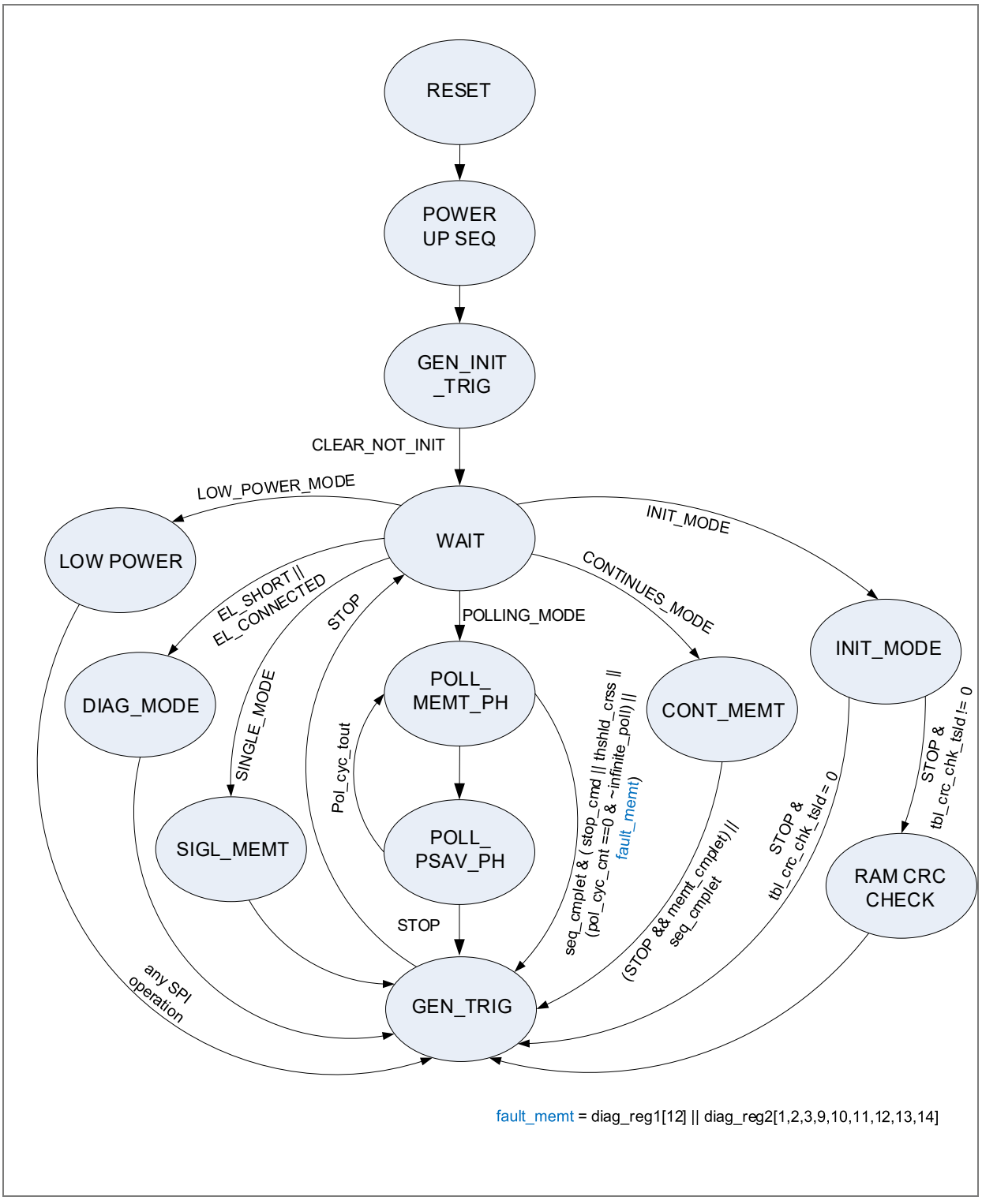
The power-up sequence waveform is given below.

Figure 5: Power-up sequence



The state diagram of the device is given below:

Figure 6: State diagram



6.2 Generate trigger mode

The device generates a trigger pulse on RES_TRIG to notify that it is ready to accept new commands.

It can enter wait mode after receiving a STOP command.

6.3 Wait mode

The device enters wait mode at startup after receiving a CLEAR_NOT_INIT command.

It can also enter this mode from all other modes after receiving a STOP command.

From this mode the device can enter into any mode through SPI command.

6.4 Initialization mode

This mode can be entered only from wait mode following an INIT_MODE command.

The device can be configured via SPI; writing to configuration tables in any other mode is not possible; any attempt to do so will result in the INVALID_SPI_WRITE flag being set.

Once the MCU completes configuring tables and control registers, exit from this mode is possible by sending a STOP command. On STOP command if TBL_CRC_CHK_TSLD is non-zero then the configuration table CRC check will be executed. On completion of CRC check the device enters into generate trigger mode and then enters wait mode by STOP command.

‘0’ in TBL_CRC_CHK_TSLD will result into device entering generate trigger mode without configuration table CRC check.

6.5 Single measurement mode

This mode can be entered only from wait mode following a SINGLE_MODE command.

The device should be properly configured before entering this mode.

Once into this mode, old measurement data is cleared from memory; a new measurement is executed with the configuration table settings pointed by MEMT_STRT_PTR; MEMT_SEQ content is ignored.

Each conversion will take between 45 and 300 µs, depending on the LPF settling time defined in SETTLING_DCLPF.

Measurement data will be stored at a location corresponding to the active configuration table.

Once the measurement is complete the device enters the generate trigger mode; it will go back to wait mode after receiving a STOP command.

The single measurement operation waveform and flowchart are given below.

Figure 7: Single measurement operation waveform

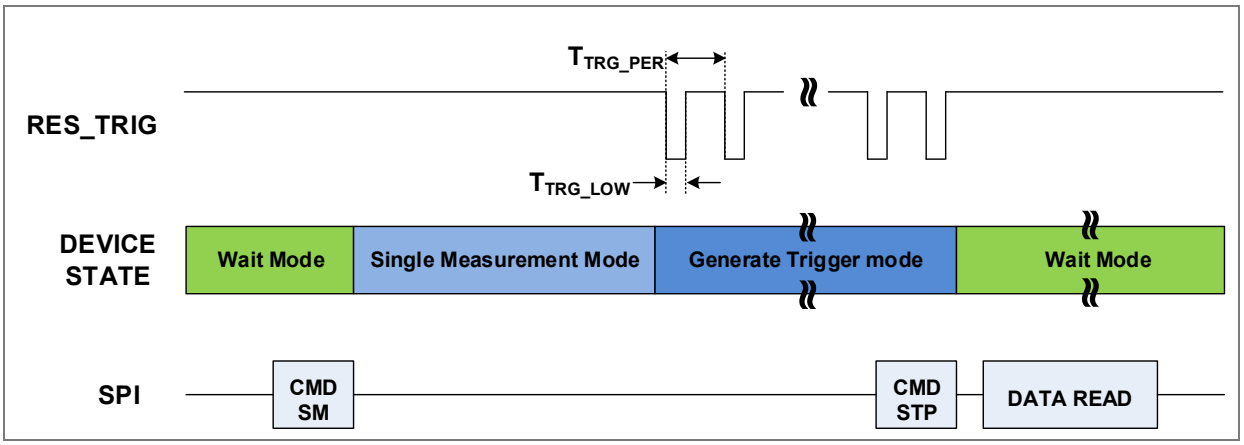
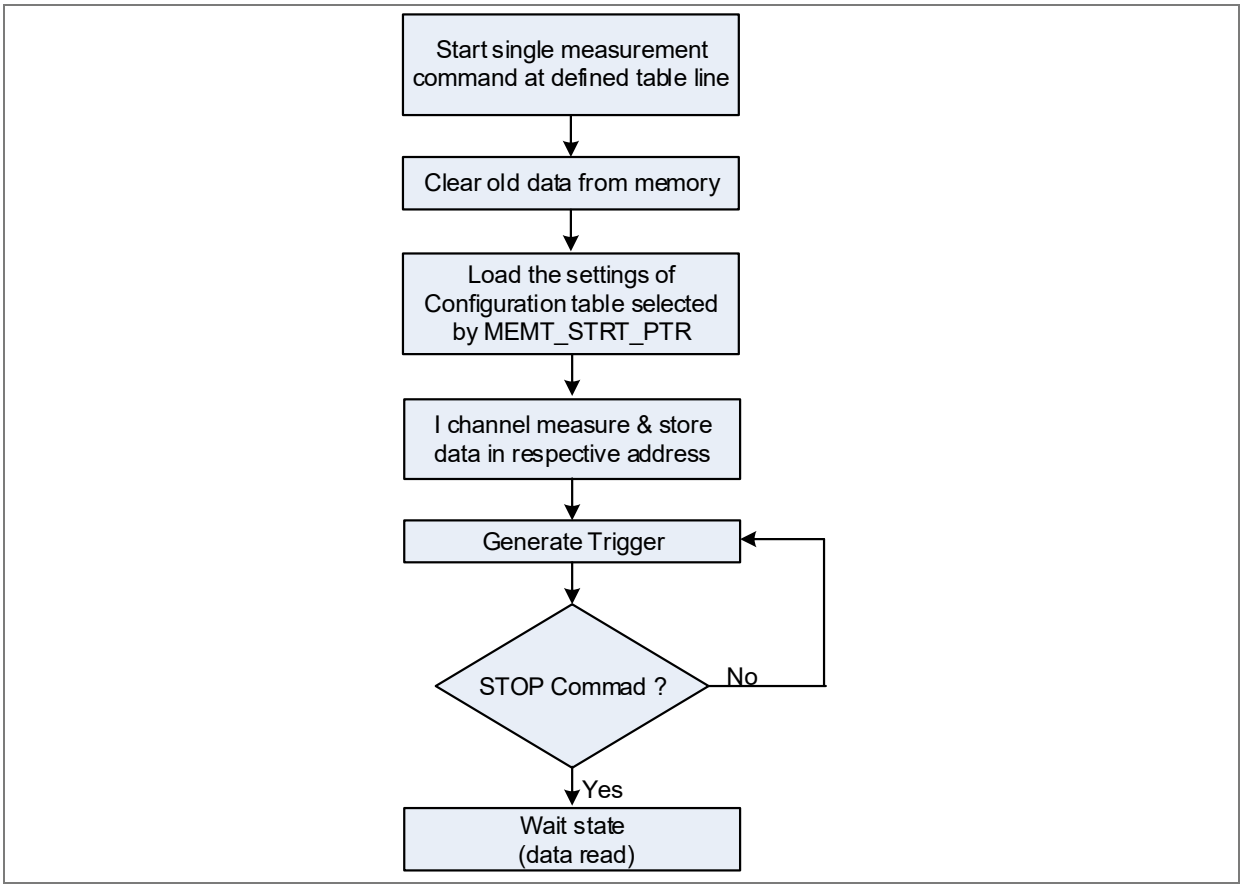


Figure 8: Single measurement operation flowchart



6.6 Continuous measurement mode

This mode can be entered only from wait mode following a CONTINUOUS_MODE command.

The device should be properly configured before entering this mode.

Once into this mode, old measurement data is cleared from memory; a sequence of measurements is executed using settings written in the configuration tables enabled in MEMT_SEQ , and starting with the table pointed by MEMT_STRT_PTR; more information can be found in chapter 6.11.

Measurement data will be stored at a location corresponding to the active configuration table.

Once the measurement is complete the device enters into the generate trigger mode; it will go back to wait mode after receiving a STOP command.

The continuous measurement operation waveform and flowchart are given below.

Figure 9: Continuous measurement operation waveform

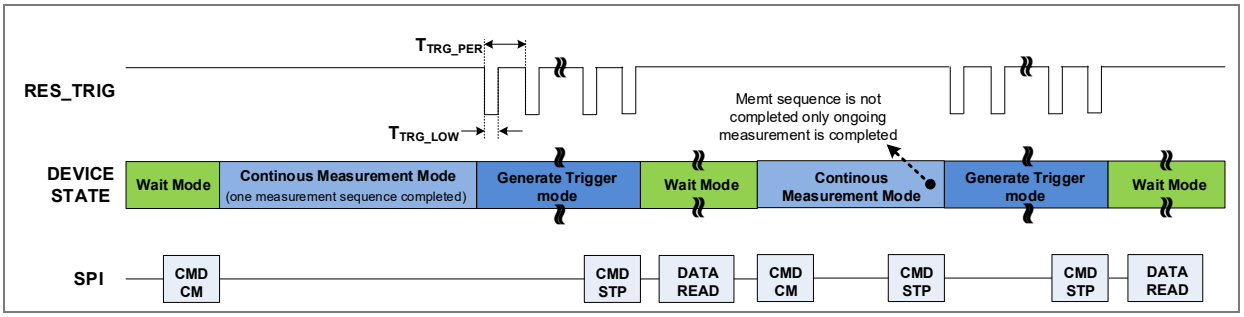
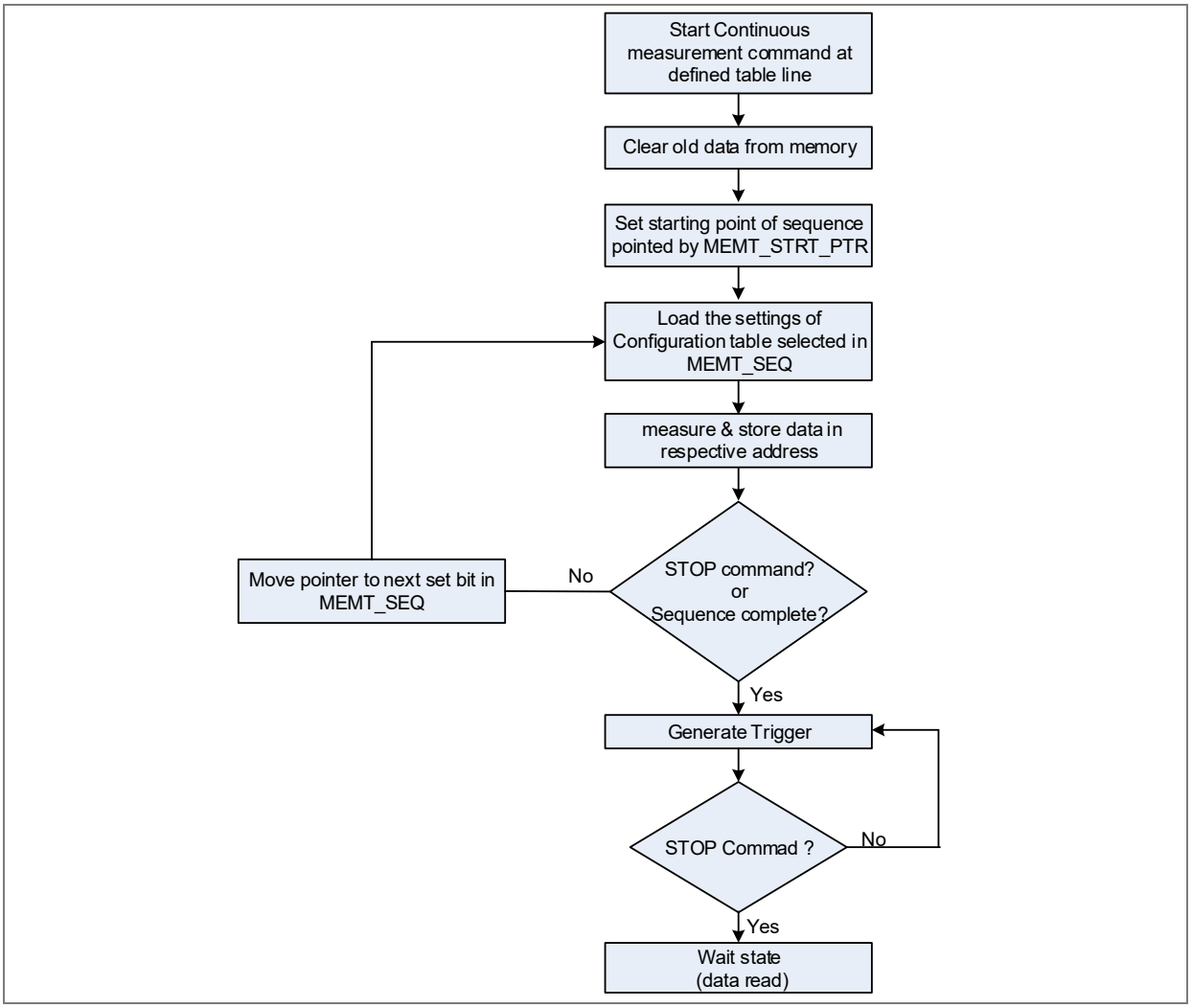


Figure 10: Continuous measurement operation flowchart



6.7 Polling measurement mode

This mode can be entered only from wait mode following a POLLING_MODE command.

The device should be properly configured before entering this mode.

Once into this mode, old measurement data is cleared from memory if the clear memory bit is high.

Measurements are executed in sequence as in continuous mode, as described in chapter 6.11.

The device repeats the measurement sequence for a number of times specified in POLL_CYC_CNT; the limit can be disabled by setting INFINITE_POLLING.

The interval between the starting point of two measurement sequences can be selected from 12 to 128 ms acting on POLL_TIME.

Measurement data is stored according to a FIFO buffer concept: The latest value is always saved at address 0x00, the second-last at address 0x01, etc.

After every measurement the data is compared with THRESHOLD_LOW and THRESHOLD_HIGH of the corresponding configuration table. If the measured data crosses any of these lower or higher thresholds then the respective flag will be set in DIAG_REG_1.

Between the completion of a measurement sequence and the start of the next one the device enters a power save state; all AFE blocks and the oscillator block are turned off; the VDD3 regulator is off; a low frequency oscillator and the polling cycle timer will be working in this phase.

Any SPI transaction during the power save state will enable the oscillator, which will keep working until the next measurement phase; in this case there will be an additional power consumption due to the oscillator running.

An SPI transaction is recognized after 5 pulses of SCLK past the falling edge of CSN.

After the total number of polling cycles are completed or if any threshold cross flags are set or any diagnostic events are detected, then the device enters into generate trigger mode; it will go back to wait mode after receiving a STOP command. It is also possible to terminate the polling mode by sending a STOP command; the device will complete the current measurement sequence then enter into generate trigger mode. Any other command will be ignored.

If TBL_CRC_CHK_TSLD is non-zero then the configuration table CRC check will be executed every TBL_CRC_CHK_TSLD measurement sequences; a CRC check lasts for 116 clock cycles (29µs typ.).

Following are some operation waveforms and a flowchart of polling mode:

Figure 11: Polling cycle waveform

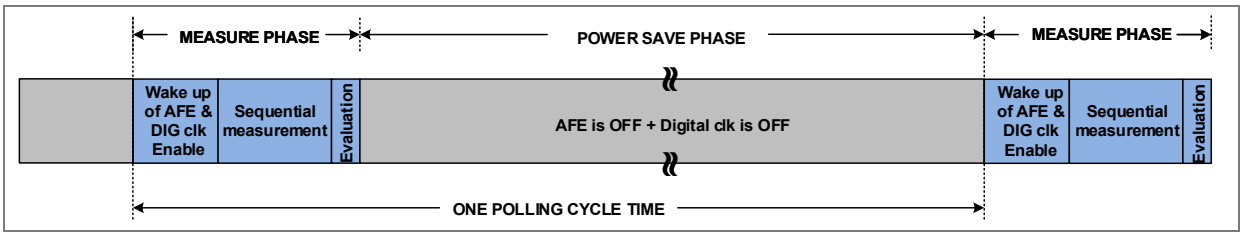


Figure 12: Polling mode operation

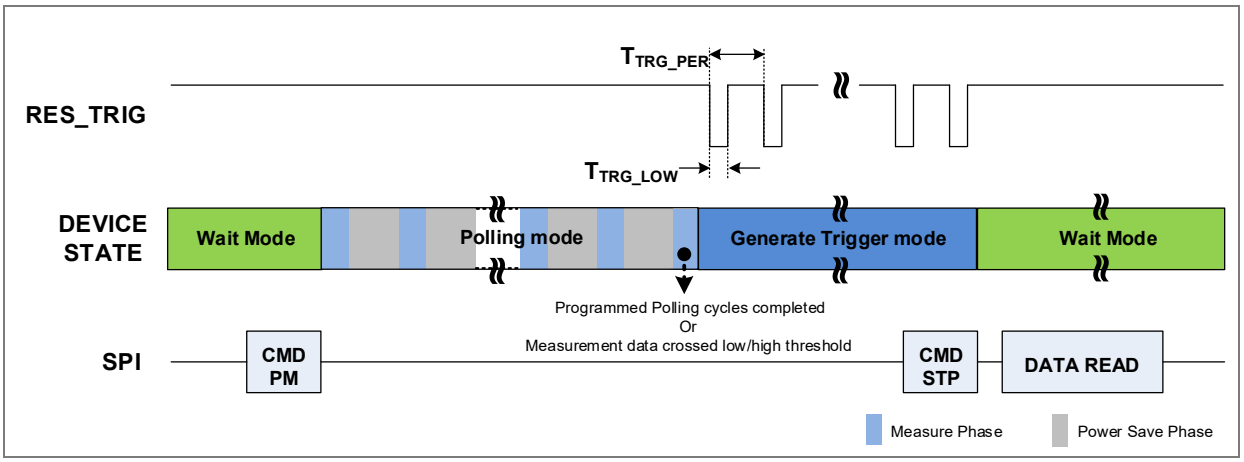


Figure 13: Polling mode operation with asynchronous STOP command

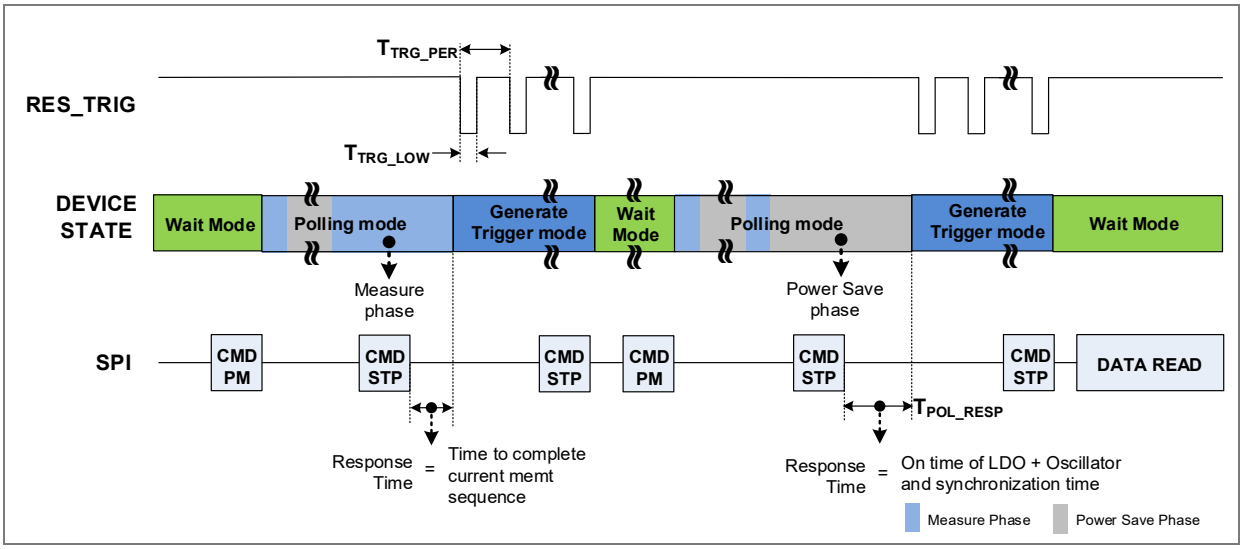
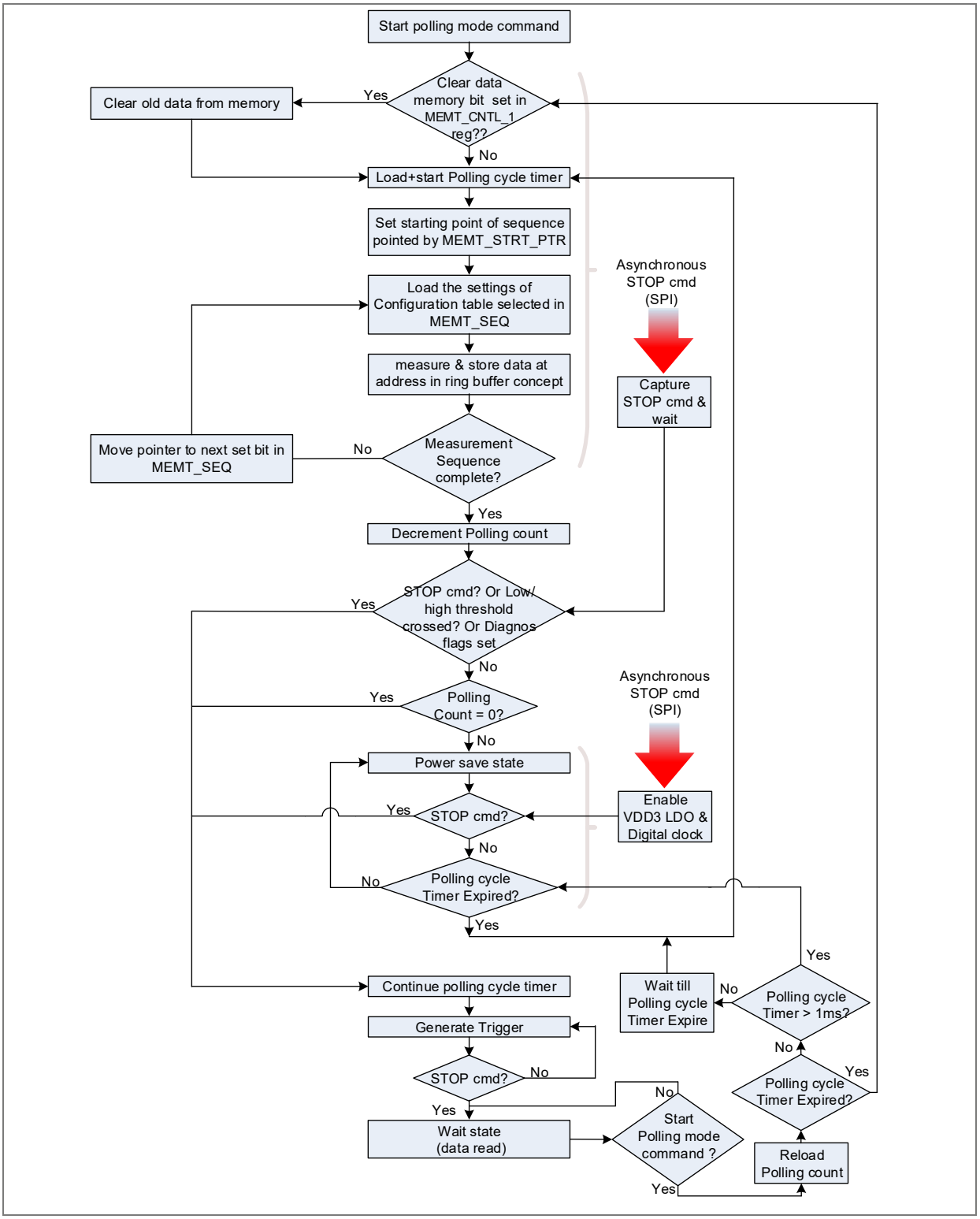


Figure 14: Polling mode operation flowchart



6.8 Low power mode

This mode can be entered only from wait mode following a LOW_PWR_MODE command.

Any SPI operation will cause the device to enter into generate trigger mode.

6.9 Diagnostic modes

Diagnostics is implemented to ensure all blocks are operating within their operating range (not only functional) to allow robust determination when the system may not be able to properly detect the capacitance change. This applies not only to the functionality of the sensor but also to the interface.

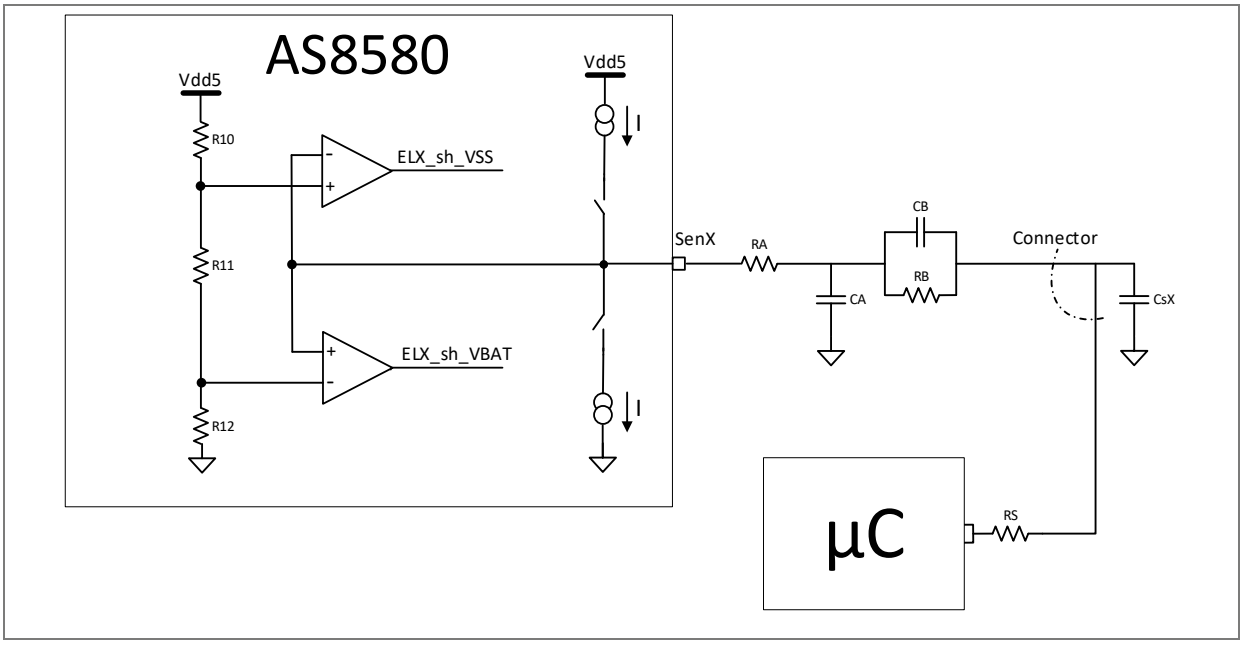
When the µC is not performing the EL_CONNECTED diagnostic the connection between the electrode and the µC itself has to be tri-stated.

Information:

CUSTOMER shall take care that any non-ideal effect (PSRR, Impedance, etc.) due to the connection of the µC to the electrodes will not affect the measurement.

The simplified schematic diagram in diagnostic mode is given below.

Figure 15: Diagnostic concept



Two dedicated diagnostic modes are in place to verify that the electrodes are not shorted to VSS nor to VBAT and that the electrodes are connected to the device.

In EL_SHORT mode the device is able to detect a short to VBAT or GND.

On every selected sensor pin two current mirrors force sequentially a positive and negative current and a couple of comparators check that the voltage stays close to VDD5 and VSS, respectively.

The relevant bits of DIAG_REG_1 are then updated; the completion of this procedure is communicated to the host through pulses on RES_TRIG until a STOP command is received.

In EL_CONNECTED mode the device is able to detect an open connection.

To perform this diagnostic function the µC has to first force the electrodes to VSS.

After a settling time from the mode change command the sensor forces a positive current on each selected electrode and a comparator checks that the voltage stays close to VSS.

The relevant bits of DIAG_REG1 are then updated; the completion of this procedure is communicated to the host through pulses on the RES_TRIG pin until a STOP command is received from SPI.

Sensor pins can be individually enabled by writing on ELEC_DIAG_SEL.

Table 11: Diagnostic function

Parameter	Symbol	Min	Typ	Max	Unit	Note
Short to VSS threshold	TH_DIAG_VSS		0.9*VDD5		V	Info parameter(1)
Short to VBAT threshold	TH_DIAG_VBAT		0.15*VDD5		V	Info parameter(1)
Short to VBAT bias current	I_DIAG_SH_VBAT	250	360	500	µA	Info parameter(1)
Short to VSS bias current	I_DIAG_SH_VSS	80	120	160	µA	Info parameter(1)
Bias current EL_CONNECTED	I_DIAG_CONN	14	20	30	µA	Info parameter(1)
Evaluation time EL_SHORT	T_DIAG_SH		120		µs	One electrode
Evaluation time EL_CONNECTED	T_DIAG_CONN		60		µs	One electrode

(1) Info Parameters are not pass/fail parameters in production where limits are calculated from simulation and characterization.

6.10 Diagnostic features

The device performs a number of diagnostic checks at various phases; the results are available as diagnostic flags. Some checks also cause the device to exit polling mode after the measurement sequence is completed and to enter the generate trigger mode. A list is given below.

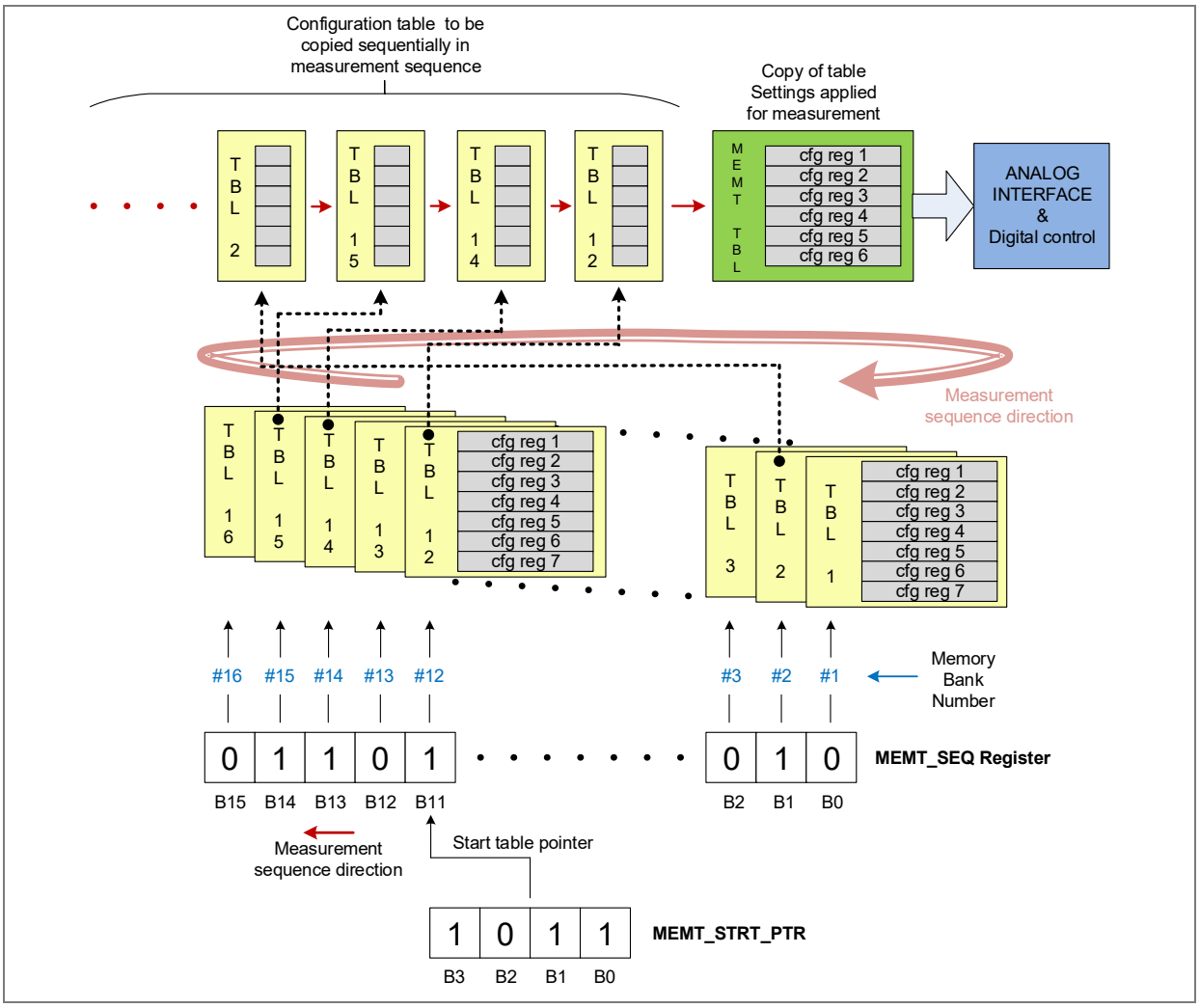
Table 12: List of diagnostic checks

Diagnostic feature	Enabled	Effect	Note
EL_SHORT	By command	Diag. flag	
EL_CONNECTED	By command	Diag. flag	
Undervoltage VDD5	During measurement	Diag. flag + Stop polling	
Undervoltage VDD3	During measurement	Diag. flag + Stop polling	
Overvoltage VDD3	During measurement	Diag. flag + Stop polling	
Overvoltage VDD3 DIG	During measurement	Diag. flag + Stop polling	
Overcurrent VDD3	During measurement	Diag. flag + Stop polling	
Overcurrent VDD3 DIG	During measurement	Diag. flag + Stop polling	
Thermal protection	During measurement	Diag. flag + Stop polling	
PLL lock fail	During measurement	Diag. flag + Stop polling	
Electrode driver overcurrent	During measurement	Diag. flag + Stop polling	
Measurement data crossed upper or lower threshold	During measurement	Diag. flag + Stop polling	
CRC on RAM fail	During measurement and after CRC write	Diag. flag + Stop polling	
NOT_INIT	During power-up	Diag. flag	
RAM BIST TEST fail	During power-up	Diag. flag	
OTP_FAIL	During power-up	Diag. flag	
SPI_PARITY	After SPI frame	Diag. flag	
SHORT/LONG SPI	After SPI frame	Diag. flag	
NO BANK ACCESS	After SPI frame	Diag. flag	
INVALID_SPI_WRITE	After SPI frame	Diag. flag	

6.11 Measurement sequence with configuration tables

The concept of measurement sequence with different configuration settings applied is shown in the following diagram:

Figure 16: Measurement sequence with configuration tables



A measurement sequence begins with the configuration table pointed by MEMT_STRT_PTR, then the table pointer is increased. If a bit in the MEMT_SEQ is 1 then the corresponding configuration table will be part of the sequential measurement; if it is 0 the table will not be used. The settings in the selected tables will be used when their turn arrives. A sequence is completed once all 16 tables are checked and processed accordingly.

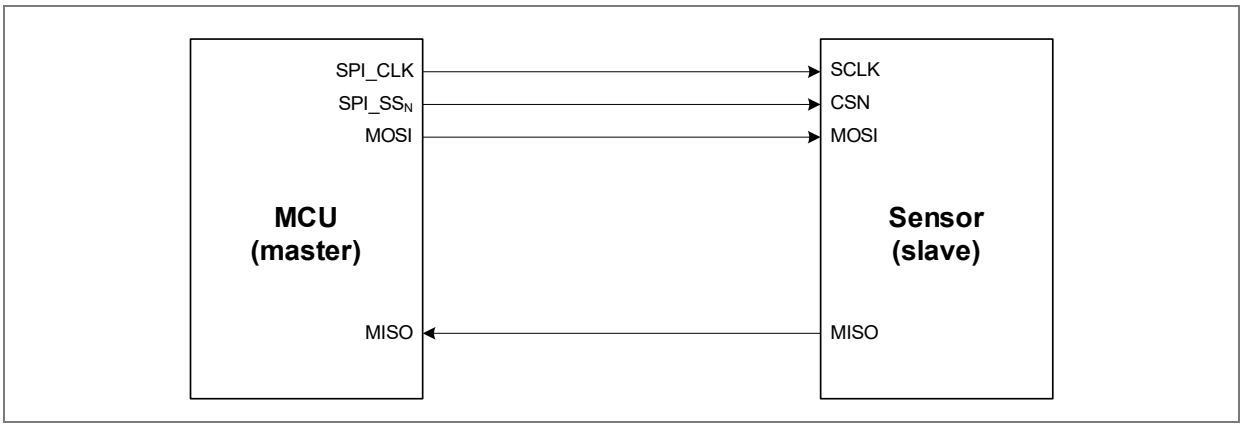
6.12 Chip ID

All devices are provided with a unique ID code stored at addresses 0x1C:0x1E in the OTP memory.

6.13 SPI interface

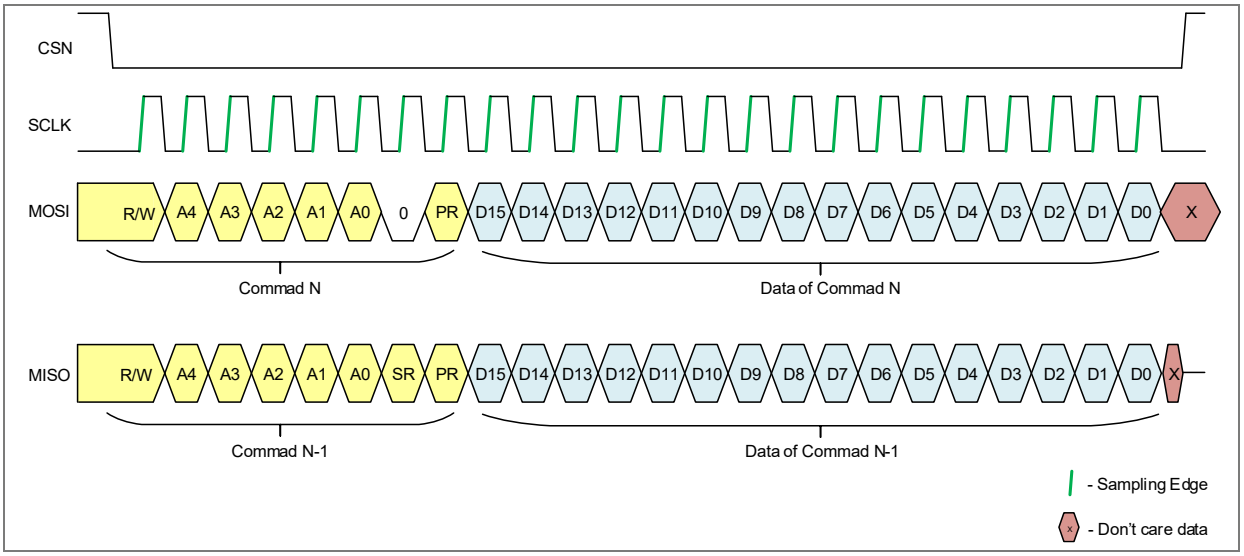
The sensor communicates through a serial peripheral interface (SPI), consisting of Serial Clock (SCLK), Data Out (MISO), Data In (MOSI), and Chip Select (CSN) pins. The sensor acts as SPI slave.

Figure 17: SPI bus topology



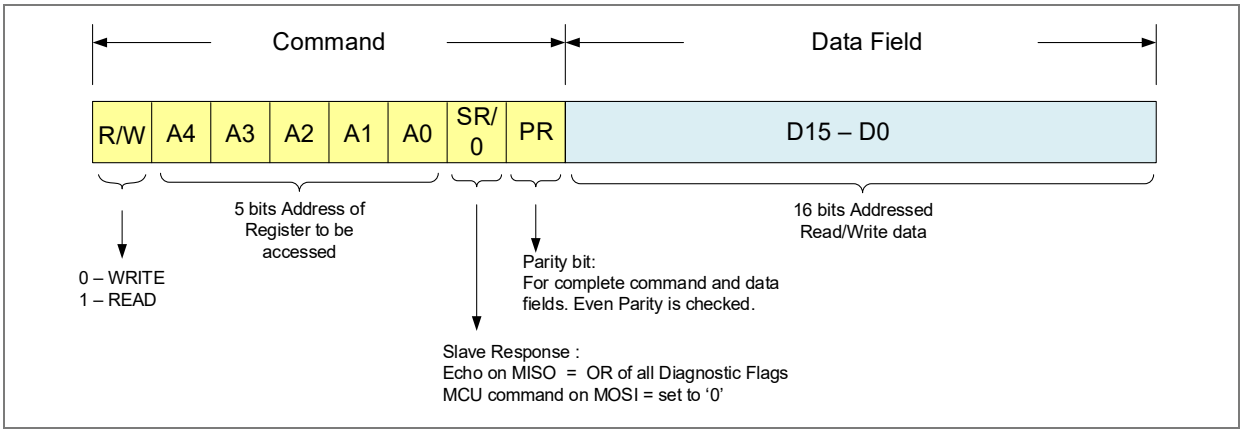
The SPI transaction begins when CSN is asserted (driven low). On every positive edge of SCLK, master and slave sample data on MISO and MOSI, respectively. On every negative edge of SCLK, master and slave send data on MOSI and MISO, respectively. The SPI transaction ends when CSN goes high. A complete SPI transaction contains 24 SCLK cycles. Shorter or longer transactions will result in errors being reported in the diagnostic register. A time diagram of an SPI transaction is shown below.

Figure 18: SPI transaction detailed diagram



An SPI frame is composed by an 8-bit command, followed by a 16-bit data field. The SPI frame format is shown in following diagram.

Figure 19: SPI frame format



Two types of SPI transfers are possible, write and read. The device always transmits data relative to the previous transaction; it echoes the previous command in the command field and sends data of the previously addressed register in the data field. Below are examples of write and read transactions.

Figure 20: SPI write transaction

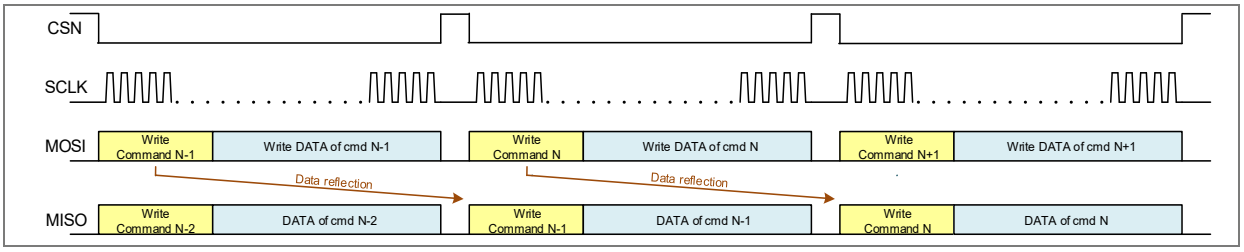
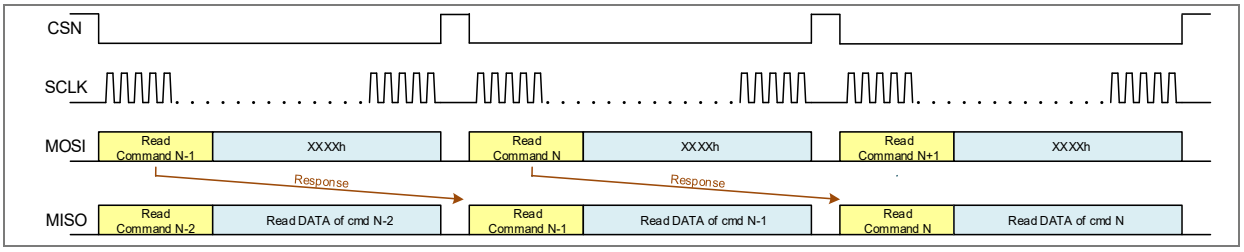
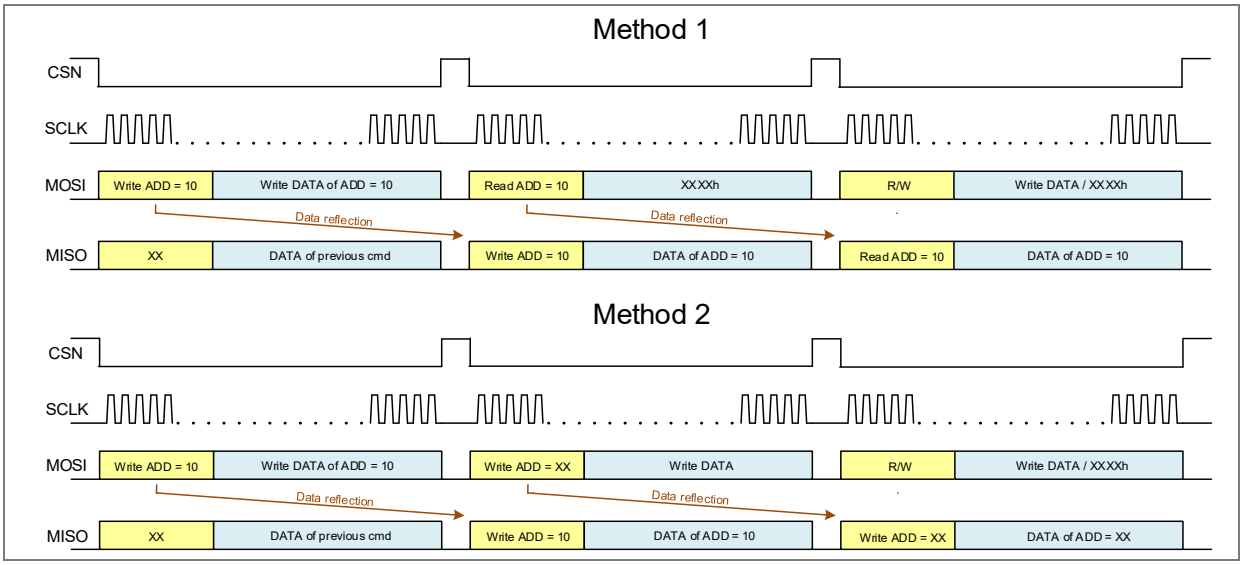


Figure 21: SPI read transaction



In the system it is required to validate data written through SPI. This can be done by a dedicated read transaction or by reading the register just written during the next write transaction. Both methods are illustrated in the following diagram.

Figure 22: SPI write operation data check methods



6.14 SPI timing characteristics

Figure 23: SPI timing diagram

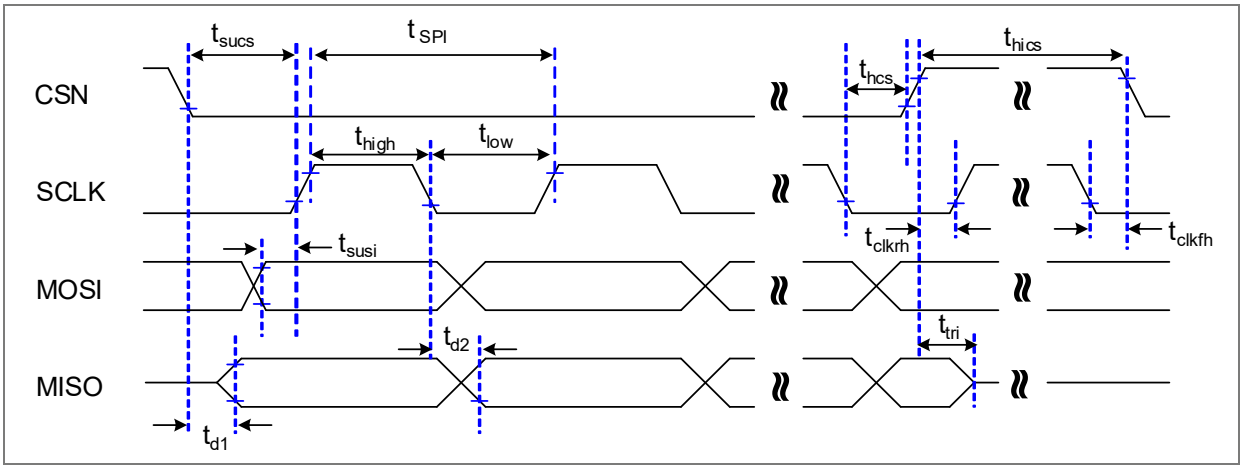


Table 13: SPI timing characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
SCLK period	t_{SPI}	125			ns	Max frequency is 8 MHz
SCLK high time	t_{high}	57.5	62.5	-	ns	
SCLK low time	t_{low}	57.5	62.5	-	ns	
CSN setup time	t_{sucs}	57.5	62.5	-	ns	
Delay time 1	t_{d1}	-	-	40	ns	
MOSI setup time	t_{susi}	15	-	-	ns	
Delay time 2	t_{d2}	-	-	40	ns	
CSN hold time	t_{hcs}	57.5	$T_{SPI}/2$	-	ns	
Tri-state delay time	t_{tri}	-	-	30	ns	
CSN high time	t_{hics}	1250	-	-	ns	
SCLK hold time after CSN rising	t_{clkrh}	10	-	-	ns	
SCLK hold time before CSN falling	t_{clkfh}	10	-	-	ns	

7 Detailed system and block specification

7.1 System timing

Figure 24: System timing

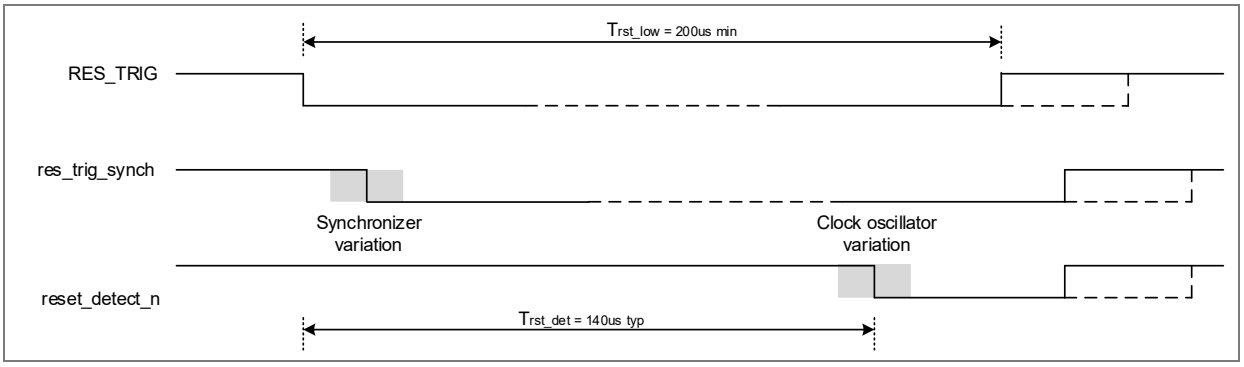


Table 14: System timing

Parameter	Symbol	Min	Typ	Max	Unit	Note
Low time of trigger pulse	TTRG_LOW	14	16	18	µs	
Trigger pulse period	TTRG_PER	4	7	10	ms	
Minimum low time on RES_TRIG to reset the device	TRST_LOW	200			µs	
Reset detection time	TRST_DET	105	140	175	µs	
Response time for STOP/SPI command during power save phase in polling mode	TPOL_RESP			100	µs	Wait time before sending the next SPI command.
Polling time accuracy	TPOL_ACC	-15		15	%	Polling time is selected via register

7.2 System parameters

Table 15: System parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transceiver carrier frequency	AFE_FREQ	5		20	MHz	Set via register (1)
System sensitivity	AFE_SENS		1.9		fF/LSB	Part-to-part variation PRE_GAIN 4; PGA_GAIN -33.3; room temperature; typical supply; TX and RX filters at 3 x AFE_FREQ; at the AFE_FREQ factory trimmed frequency *(7.43 MHz)*
Wake up time	AFE_WAKEUP			60	µs	PLL prescaler ratio = 1 Info parameter (2)
Measurement time	AFE_TMEAS		210		µs	Using 2 tables, 60µs LPF settling, PLL prescaler 1; add 15µs for each additional oversampling measurement. Info parameter(2)
System noise	AFE_N		4		LSB RMS(3)	Configuration as in AFE_SENS definition above; 2 accumulations; room temperature; typical process.
System tolerance to temperature drift	AFE_TOL		5	40	LSB/ºC	

(1) Frequency over 15MHz is not pass/fail parameters in production where limits are calculated from simulation and characterization.
(2) Info Parameters are not pass/fail parameters in production where limits are calculated from simulation and characterization.
(3) Noise is calculated as the standard deviation of 100 measurements.

7.3 PLL

The PLL synthesizer generates a clock signal with frequency between 5 MHz and 20 MHz. The reference frequency is generated by a 4MHz oscillator conveniently divided by a prescaler to ensure an optimum PLL locking time. The oscillator frequency can be changed by ±160 kHz acting on RCO.

Table 16: PLL parameters

Parameter	Symbol	Min	Typ	Max	Unit	Note
Main clock frequency	MCLK	3.8	4	4.2	MHz	Without spread spectrum. Factory trimmed
Frequency step	OSC_STEP		80		KHz	Info parameter(1)
Oscillator switch-off time	OSC_OFF		2		µs	Info parameter(1)
Start-up time	OSC_ON		2		µs	Info parameter(1)
PLL input frequency	PLL_FIN	0.1		4.2	MHz	Reference frequency
PLL output frequency	PLL_FOUT	5		20	MHz	
VCO phase resolution	PLL_PHRES		11.25		deg	Info parameter(1)
Settling time 00b	PLL_TS0		5		µs	Prescaler ratio = 1
Settling time 01b	PLL_TS1		20		µs	Prescaler ratio = 7
PLL bandwidth	PLL_BW		100		KHz	Info parameter(1)
Spread spectrum deviation	PLL_SS_DEV	0		10	%	Selectable via register Info parameter(1)

(1) Info Parameters are not pass/fail parameters in production where limits are calculated from simulation and characterization.

7.4 TX sine DAC / filter

The SINEDAC block generates a discrete sine wave with 16 samples per period; it uses 16 clock phases from the PLL VCO with 1/16 TCLK phase resolution. The SINEDAC is based on a resistive divider with variable R/R ratio.

These can be defined by using FREQ, PRESCALER, and TX_LPF fields in the control registers.

The DAC output is filtered with a first order passive low-pass filter for noise reduction.

7.5 TX driver and current sensing

“Driver” module in block diagram. The transmitter topology is designed to optimize performance and power consumption across frequency. The output stage can drive a continuously changing capacitive load at 5 to 20 MHz providing a low impedance output. Over-current events are signaled through the OC_DRIVER flag.

7.6 TX multiplexer

“MUX” module in block diagram. A multiplexer is implemented to connect the buffered sinewave signal to each sensor (SEN0 through SEN3) and/or an internal reference capacitance. The 30pF internal reference capacitance is sub ranged in 2pF steps with REFERENCE field in MEMT_CNTL_1 register.

SEN controls which sensors are connected during every measurement; it is possible to have more than one sensor connected at the same time.

Unused sensors can be shorted to ground by setting SEN_TO_GND.

7.7 Trans impedance amplifier

“Charge amplifier” in block diagram. The current-to-voltage conversion is performed by a trans-impedance amplifier. The feedback impedance is predominantly capacitive in the operating frequency range; considering the sensor this creates a constant closed loop gain factor (C/C) over frequency.

The op-amp topology is designed to optimize performance in the entire frequency range.

7.8 Band pass filter / pre-amplifier

“Filter / Preamplifier” in Block Diagram. An AC coupled low-pass filter is implemented to ensure better EMC performance and minimize the effect of harmonics. The gain can be changed in order to optimize the signal to noise ratio. PRE_GAIN bits can be used to control the gain, and RX_LPF to define the cut-off frequency.

7.9 Demodulation

The demodulation module multiplies the signal by ±1 using a passive switch. The absolute phase shift between the carrier signal (SINDAC block) and the clock can be programmed in steps of 11.25º.

7.10 Low pass filter

A third-order low-pass filter is needed to reject the $2F_c$ and higher demodulator terms. A cutoff frequency of 40 KHz was chosen as a tradeoff between stop-band attenuation and settling time. The filter is a cascade of a second-order Sallen-Key stage and a first-order passive stage, providing a response close to a Bessel approximation.

7.11 Offset comp: Programmable gain amplifier

A programmable gain amplifier is used to further increase the level of the demodulated and filtered DC signal. The amplifier has a second input used to add or subtract an offset in order to shift the input range of the signal chain. The offset signal is generated by a 10-bit DAC.

Use register fields PGA_GAIN_ISET and PGA_OV_ISET to control this.

7.12 ADC

A 12-bit SAR ADC is used to convert the analog signal into digital words.

The wait time from low-pass filter (see 7.10) power-up to A/D conversion can be adjusted from 20µs to 272µs by acting on SETTLING_DCLPF.

Each conversion requires 14 clock cycles of 1µs (typical value).

7.13 Voltage regulators

Two independent voltage regulators are used to supply the digital and analog blocks with 3.3V; the voltage is factory trimmed. An external capacitor is required to ensure stability of each regulator.

7.14 Supply monitor

VDD5, VDD3, and VDD3DIG are constantly monitored in order to ensure that all internal blocks operate correctly.

Under-voltage of VDD3DIG generates a reset of the digital machine.

Other events are signaled through flags in the diagnostic register.

8 SW interface

Table 17: Register overview

Addr.	Control & status	Table1	Table2	...	Table16
	Bank #00	Bank #01	Bank #02	...	Bank #16
(5b)	(16b)	(16b)	(16b)	...	(16b)
0x00	MEMT_DATA_1				
0x01	MEMT_DATA_2				
•	•				
•	•				
0x0E	MEMT_DATA_15				
0x0F	MEMT_DATA_16				
0x10	BANK_SEL				
0x11	MEMT_SEQ	MEMT_CFG1_TBL1	MEMT_CFG1_TBL2	...	MEMT_CFG1_TBL16
0x12	MEMT_CTL_1	MEMT_CFG2_TBL1	MEMT_CFG2_TBL2	...	MEMT_CFG2_TBL16
0x13	MEMT_CTL_2	MEMT_CFG3_TBL1	MEMT_CFG3_TBL2	...	MEMT_CFG3_TBL16
0x14	MEMT_CTL_3	MEMT_CFG4_TBL1	MEMT_CFG4_TBL2	...	MEMT_CFG4_TBL16
0x15	POLL_CYC_CNT	MEMT_CFG5_TBL1	MEMT_CFG5_TBL2	...	MEMT_CFG5_TBL16
0x16	POLL_CYC_CNT_	MEMT_CFG6_TBL1	MEMT_CFG6_TBL2	...	MEMT_CFG6_TBL16
0x17	RAM_CFG_TBL_C	MEMT_CFG7_TBL1	MEMT_CFG7_TBL2	...	MEMT_CFG7_TBL16
0x18	TBL_CRC_CHK_T	Reserved	Reserved	...	Reserved
0x19	DIAG_REG_1	Reserved	Reserved	...	Reserved
0x1A	DIAG_REG_2	Reserved	Reserved	...	Reserved
0x1B	DIAG_REG_3	Reserved	Reserved	...	Reserved
0x1C	Reserved	Reserved	Reserved	...	Reserved
0x1D	Reserved	Reserved	Reserved	...	Reserved
0x1E	Reserved	Reserved	Reserved	...	Reserved
0x1F	Reserved	Reserved	Reserved	...	Reserved

Bank independent registers

Registers under bank select. Bank selection is password protected.

8.1 MEMT_DATA_1-16 (Address 0x00-0x0F, all banks)

Table 18: Measurement data register

R-0(1)	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MEASUREMENT[15:0]															
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description	
MEASUREMENT[15:0]	The number of bits of measured value depends on the accumulation setting programmed in the corresponding configuration table:	
	ACCU[1:0]	**MEASUREMENT[15:0]**
	00	MEAS[15:4],0000
	01	MEAS[15:3],000
	10	MEAS[15:2],00
	11	MEAS[15:1],0
	Polling mode: FIFO buffer used; newest value is stored at address 0; second-last at address 1, etc. **Single mode:** Value is stored at the address corresponding to the measurement table (e.g. measurement table 5 at address 4). **Continuous mode:** Value is stored at the address corresponding to the measurement table	

(1) [Bit type]-[power-on value] →R = Read only, RW = Read/write
E.g. R-1 means read-only bit with power-on at 1

8.2 BANK_SEL (Address 0x10, all banks)

Table 19: Bank select register

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
ACCESS WORD[7:0]								BANK[7:0]							
BIT 15							BIT 8	BIT 7							BIT 0

Field	Description
ACCESS WORD[7:0]	Password to protect from accidental change of content. Data is written into the bank selection bits only when this field is 0x5A. A wrong password will deselect the bank.
BANK[7:0]	Selected bank number (0 to 0x11), e.g. 0 selects bank 0. 0x11 selects bank 17.

At power up no bank is selected and only this register is accessible. If no bank is selected and an SPI is initiated to access other registers, then the NO_BANK_ACCESS flag will turn on in DIAG_REG_2.

8.3 MEMT_SEQ (Address 0x11, bank 0)

Table 20: Measurement sequence register

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
MEMT_SEQ_EN[15:0]															
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description
MEMT_SEQ_EN[15:0]	Each bit enables a table in a measurement sequence; bit 0 corresponds to Table 1, bit 15 to Table 16. Configuration registers for Table X are available at bank X. The measurement sequence moves from LSB to MSB, starting from the bit position specified in MEMT_STRT_PTR bits in MEMT_CNTL_2 register. In single measurement mode the content of this register is ignored.

8.4 MEMT_CNTL_1 (Address 0x12, bank 0)

Table 21: Measurement control register 1

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
0	0	RCO[1:0]		CONTROL[4:0]					POLL_TIME[2:0]			REFERENCE[3:0]			
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description		
RCO[1:0]	Oscillator frequency tuning. This setting is only applicable when RCO_EN is set		
	RCO[1:0]		**Frequency**
	00		4MHz + 80KHz
	01		4MHz + 160KHz
	10		4MHz - 80KHz
	11		4MHz - 160KHz
CONTROL[4:0]	Chip control settings		
	Bit	**Name**	**Description**
	4	INFINITE_POLLING	0 – Polling cycle counter is active. After each polling sequence the counter is decremented. Polling cycle will run until the counter becomes ‘0’. The counter status can be checked in the POLL_CYC_CNT_STS register. 1 – Polling cycle will run indefinitely. The polling cycle counter is not decremented.
	3	CLEAR_MEMORY	Clear measurement memory in polling mode. 0 – Previous measurement data is retained in memory. Once measurement starts the corresponding locations will be overwritten. 1 – Clears measurement data from memory before starting polling. (Default)
	2	DC_LPF_RESET	Reset the DC/LPF between measurements 0 – Disabled. 1 – Enabled. (Default)
	1	CSN_PU	Enable internal CSN pull up resister 0 – Pull up connected (Default) 1 – No pull up.
	0	RCO_EN	Enables oscillator control by RCO
POLL_TIME[2:0]	Polling time selection (typical value)		
	POLL_TIME[2:0]		**Time (ms)**
	000		12
	001		16
	010		20

Field	Description	
	011	28
	100	36
	101	48
	110	64
	111	128
REFERENCE[3:0]	Internal reference capacitance selection (typical value)	
	REFERENCE[3:0]	**Ref cap (pf)**
	0000	-
	0001	2
	0010	4
	0011	6
	0100	8
	0101	10
	0110	12
	0111	14
	1000	16
	1001	18
	1010	20
	1011	22
	1100	24
	1101	26
	1110	28
	1111	30

8.5 MEMT_CNTL_2 (Address 0x13, bank 0)

Table 22: Measurement control register 2

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	R-0	R-0	R-0	R-0
0	0	0	0	COMMAND[3:0]				MEMT_STRT_PTR[3:0]				MEMT_CUR_PTR[3:0]			
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description		
COMMAND[3:0]	Measurement or diagnostic mode.		
	COMMAND[3:0]	**Name**	**Description**
	0000	NOP	No operation will be performed.
	0001	STOP	Stop current measurement or trigger generation **Single mode:** Measurement is stopped after current measurement is finished. **Polling mode:** Measurement is stopped after completing all measurements defined in MEMT_SEQ register. **Continuous mode:** Measurement is stopped after current measurement.
	0010	CLEAR_NOT_INIT	Clear the NOT_INIT flag in the diagnostic register.
	0011	INIT_MODE	Configuration and control registers can be written exclusively in this mode.
	0100	POLLING_MODE	The device performs the measurements in sequence, starting from the table pointed by MEMT_STRT_PTR and for tables enabled in MEMT_SEQ_EN; then it goes into power saving mode according to POLL_TIME setting; then the cycle repeats
	0101	SINGLE_MODE	The device performs one measurement, corresponding to the table pointed by MEMT_STRT_PTR
	0110	CONTINUOUS_MODE	The device performs one measurement sequence, starting from the table pointed by MEMT_STRT_PTR and for tables enabled in MEMT_SEQ_EN
	0111	EL_CONNECTED	Command to start diagnosis procedure to check electrode connection to SENx pins.
	1000	EL_SHORT	Command to start diagnosis procedure to check electrode short to GND or VBAT.
	1001	LOW_PWR_MODE	Enters into lower power mode. Only possible from wait mode.
MEMT_STRT_PTR[3:0]	Measurement start pointer. It points to the start table in a measurement sequence. In single mode only one table is considered.		
MEMT_CUR_PTR[3:0]	Measurement current pointer. It points to the last table that has completed the measurement.		

8.6 MEMT_CNTL_3 (Address 0x14, bank 0)

Table 23: Measurement control register 3

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
0	0	0	ELEC_DIAG_SEL[3:0]				spread_sp[2:0]			SETTLING_DCLPF[5:0]					
BIT 15				BIT 8				BIT 7						BIT 0	

Field	Description		
ELEC_DIAG_SEL[3:0]	Selects the electrodes for connectivity and short circuit diagnostic test.		
	ELEC_DIAG_SEL[3:0] BITS	**Description**	
	[0] = 1	E0 electrode selected	
	[1] = 1	E1 electrode selected	
	[2] = 1	E2 electrode selected	
	[3] = 1	E3 electrode selected	
SPREAD_SP[2:0]	Spread spectrum clock variation settings		
	SPREAD_SP[2:0]	**Frequency variation (%)**	**Number of steps**
	000	No Modulation	-
	100	1.25	32
	101	2.5	64
	110	5	128
	111	10	256
	others	No Modulation	-
SETTLING_DCLPF[5:0]	Low pass filter settling time (typical value)		
	SETTLING_DCLPF[5:0]	**Settling time (µs)**	
	0x00	20	
	0x01	24	
	0x02	28	
	:	:	
	:	:	
	0x3D	264	
	0x3E	268	
	0x3F	272	

8.7 POLL_CYC_CNT (Address 0x15, bank 0)

Table 24: Required polling cycles

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
POLL_CYC_CNT[15:0]															
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description
POLL_CYC_CNT [15:0]	Number of polling cycles to be executed in polling mode. This is programmed before initiating a polling mode measurement. The value is loaded into an internal counter before start. After completion of a measurement cycle the internal counter value is decremented by one. Once these polling cycles are completed a trigger pulse is generated on TRIG pin

8.8 POLL_CYC_CNT_STS (Address 0x16, bank 0)

Table 25: Polling cycle counter

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
POLL_CYC_CNT[15:0]															
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description
POLL_CYC_CNT_STS [15:0]	Remaining polling cycles to be executed in polling mode.

8.9 RAM_CFG_TBL_CRC (Address 0x17, bank 0)

Table 26: Configuration tables CRC

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
RAM_CFG_TBL_CRC[15:0]															
BIT 15								BIT 8							
BIT 7								BIT 0							

Field	Description
RAM_CFG_TBL_CRC[15:0]	Contains the 16 bits combined crc of the all configuration tables (1-16) calculated and written by the mcu. The sensor calculates the crc of all configuration tables programmed in ram with polynomial x16 + x12 + x5 + 1, with initial value of 0x1d0f, and compares it with ram_cfg_tbl_crc. A mismatch is signaled in diag_reg1.

8.10 TBL_CRC_CHK_TSLD (Address 0x18, bank 0)

Table 27: CRC check threshold

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
TBL_CRC_CHK_TSLD[15:0]															
BIT 15								BIT 8							
BIT 7								BIT 0							

Field	Description
TBL_CRC_CHK_TSLD[15:0]	Number of measurement sequences to perform before initiating a CRC check in polling mode; the CRC check will be repeated every TBL_CRC_CHK_TSLD measurement sequences. 0 means no CRC check.

8.11 DIAG_REG_1 (Address 0x19, bank 0)

Table 28: Diagnostic register 1

R-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
DIAG1[15:0]															
BIT 15								BIT 8							BIT 7	BIT 0

Field	Description	
DIAG1[15:0]	Contains the diagnostic flags corresponding to different diagnostic features. Individual bits, once set, will stay high until cleared by a write (writing '1' in any position is not accepted).	
	Bit	**Description**
	15	Bitwise OR of DIAG_REG_2[15:0] and DIAG_REG_3[0]. If this bit is 1 then the MCU needs to read DIAG_REG_2 and DIAG_3
	14	Measurement data crossed upper threshold
	13	Measurement data crossed lower threshold
	12	RAM table CRC check fail
	11	SEN3 pin electrode connection status. 0 – Electrode is connected to pin. 1 – Electrode is not connected to pin.
	10	SEN2 pin electrode connection status. 0 – Electrode is connected to pin. 1 – Electrode is not connected to pin.
	9	SEN1 pin electrode connection status. 0 – Electrode is connected to pin. 1 – Electrode is not connected to pin.
	8	SEN0 pin electrode connection status. 0 – Electrode is connected to pin. 1 – Electrode is not connected to pin.
	7	SEN3 pin electrode is shorted to VBAT.
	6	SEN2 pin electrode is shorted to VBAT.
	5	SEN1 pin electrode is shorted to VBAT.
	4	SEN0 pin electrode is shorted to VBAT.
	3	SEN3 pin electrode is shorted to GND.
	2	SEN2 pin electrode is shorted to GND.
	1	SEN1 pin electrode is shorted to GND.
	0	SEN0 pin electrode is shorted to GND.

8.12 DIAG_REG_2 (Address 0x1A, bank 0)

Table 29: Diagnostic register 2

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-1
DIAG2[15:0]															
BIT 15								BIT 8							BIT 0

Field	Description	
DIAG2[15:0]	Contains the diagnostic flags corresponding to different diagnostic features. Individual bits, once set, will stay high until cleared by a write (writing '1' in any position is not accepted).	
	Bit	**Description**
	15	OTP_FAIL: CRC OTP fail.
	14	OC_DRIVER: Overcurrent in the electrode driver
	13	PLL_FAIL: PLL fail during measurement
	12	TH_PROT: Thermal protection
	11	OC_DVDD3: Overcurrent VDD3 DIG
	10	OV_DVDD3: Overvoltage VDD3 DIG
	9	OC_VDD3: Overcurrent VDD3
	8	RAM BIST test fail
	7	NO_BANK_ACCESS: No bank is selected for SPI operation.
	6	LONG_SPI: Received a too long SPI frame
	5	SHORT_SPI: Received a too short SPI frame
	4	SPI_PARITY: Indicates the parity error in the SPI operation.
	3	VDD3V_UV: The bit is set when voltage at VDD3 falls below the UV threshold.
	2	VDD3V_OV: The bit is set when voltage at VDD3 is exceeds the OV threshold.
	1	VDD5V_UV: The bit is set when voltage at VDD5 falls below the UV threshold.
	0	NOT_INIT: This flag is set at power-on.

8.13 DIAG_REG_3 (Address 0x1B, bank 0)

Table 30: Diagnostic register 3

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
DIAG3[15:0]															
BIT 15								BIT 8							BIT 0

Field	Description	
DIAG3[15:0]	Contains the diagnostic flags corresponding to different diagnostic features. Individual bits, once set, will stay high until cleared by a write (writing ‘1’ in any position is not accepted).	
	Bit	**Description**
	15-2	Reserved, set to ‘0’
	0	OTP ECC DONE: Information flag, set when otp error correction detected and corrected a bit flip.
	1	INVALID_SPI_WRITE: Write to a table configuration register was attempted while not in INIT mode.

8.14 MEMT_CFG1_TBLX (Address 0x11, bank 1-16)

Measurement configuration register 1, there are 16 independent registers corresponding to 16 measurement tables.

Table 31: Measurement configuration register 1

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
PRESCALER [1:0]		FREQ[7:0]								SEN[5:0]					
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description		
PRESCALER[1:0]	PLL prescaler ratio.		
	PRESCALER[1:0]	**Ratio**	
	00	1	
	01	7	
	10	Not supported	
	11	Not Supported	
FREQ[7:0]	PLL feedback divider. Must be between 2 and 200. The output frequency is: FPLL = Fosc / (Prescaler ratio) x FREQ		
SEN[5:0]	Electrode selection MUX control		
	Bit	**Symbol**	**Description**
	5	SEN_TO_GND	Internally ground sensors not connected or when not measuring 0 – No grounding 1 – Grounded
	4	REF_SEL	Connect the reference electrode 0 – Not connected 1 – Connected
	3	E3_SEL	Connect the E3 electrode 0 – Not connected 1 – Connected
	2	E2_SEL	Connect the E2 electrode 0 – Not connected 1 – Connected
	1	E1_SEL	Connect the E1 electrode 0 – Not connected 1 – Connected
	0	E0_SEL	Connect the E0 electrode 0 – Not connected 1 – Connected

8.15 MEMT_CFG2_TBLX (Address 0x12, bank 1-16)

Measurement configuration register 2, there are 16 independent registers corresponding to 16 measurement tables.

Table 32: Measurement configuration register 2

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
0	0	PHASE[4:0]					TX_LPF[2:0]			TIA_FB_R[2:0]			RX_LPF[2:0]		
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description	
PHASE[4:0]	Demodulator phase shift. The SINDAC Phase is shifted by this amount with respect to the demodulator signal; LSB is 11.25º.	
TX_LPF[2:0]	Transmitter filter cutoff frequency (typical value)	
	TX_LPF[2:0]	**-3dB frequency (MHz)**
	000	-
	001	12.5
	010	17.5
	011	25
	100	35
	101	50
	110	70
	111	100
TIA_FB_R[2:0]	Trans Impedance Amplifier Feedback Resistance (typical value)	
	TIA_FB_R[2:0]	**RF(KΩ)**
	X00	0.75
	X01	1.5
	X10	3
	X11	6
RX_LPF[2:0]	Receiver filter cutoff frequency (typical value)	
	RX_LPF[2:0]	**-3dB frequency (MHz)**
	000	26
	001	36
	010	40
	011	50
	100	60

Field	Description	
	101	70
	110	80
	111	100

TIA_FB_R values X00 and X11 are not pass/fail parameters in production where limits are calculated from simulation and characterization.

8.16 MEMT_CFG3_TBLX (Address 0x13, bank 1-16)

Measurement configuration register 3; there are 16 independent registers corresponding to 16 measurement tables.

Table 33: Measurement configuration register 3

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
PGA_OV_ISET[9:0]										PGA_GAIN_ISET[3:0]				ACCU[1:0]	
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description		
PGA_OV_ISET[9:0]	PGA voltage offset correction for I channel. Voffset= PGA_OV_ISET / 1024 x 2.7V		
PGA_GAIN_ISET[3:0]	PGA gain selection for I channel (typical value)		
	PGA_GAIN_ISET[3:0]	**Symbol**	**Gain**
	0000	PGA_G0	-1
	0001	PGA_G1	-2
	0010	PGA_G2	-3.34
	0011	PGA_G3	-4.67
	0100	PGA_G4	-6.67
	0101	PGA_G5	-10.67
	0110	PGA_G6	-16
	0111	PGA_G7	-24
	1000	PGA_G8	-26.67
	1001	PGA_G9	-33.34
	1010	PGA_G10	-40
	1011	PGA_G11	-53.3
	Others	PGA_G12	-53.3
ACCU[1:0]	Measurement accumulation.		
	ACCU[1:0]	**Accumulation**	
	00	No	
	01	2 values	
	10	4 values	
	11	8 values	

PGA_GAIN_ISET values PGA_G1, PGA_G2, and PGA_G3 are not pass/fail parameters in production where limits are calculated from simulation and characterization.

8.17 MEMT_CFG4_TBLX (Address 0x14, bank 1-16)

Measurement configuration register 4 is unused and reserved for future extensions.

8.18 MEMT_CFG5_TBLX (Address 0x15, bank 1-16)

Measurement configuration register 5. There are 16 independent registers corresponding to 16 measurement tables.

Table 34: Measurement configuration register 5

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
THRESHOLD_LOW[15:0]															
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description		
THRESHOLD_LOW[15:0]	Lower threshold. If the measured value is lower than the threshold the device will exit Polling mode and go into Generate Trigger mode, and the corresponding flag in DIAG_REG_1 will be set. Depending on the ACCU setting the MCU has to program the threshold with the appropriate number of bits.		
	ACCU	**Lower threshold**	**Set to '0'**
	00	[15:4]	[3:0]
	01	[15:3]	[2:0]
	10	[15:2]	[1:0]
	11	[15:1]	[0]

8.19 MEMT_CFG6_TBLX (Address 0x16, bank 1-16)

Measurement configuration register 6. There are 16 independent registers corresponding to 16 measurement tables.

Table 35: Measurement configuration register 6

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
THRESHOLD_HIGH[15:0]															
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description		
THRESHOLD_HIGH[15:0]	Higher threshold. If the measured value is higher than the threshold the device will exit Polling mode and go into Generate Trigger mode, and the corresponding flag in DIAG_REG_1 will be set. Depending on the ACCU setting the MCU has to program the threshold with the appropriate number of bits.		
	ACCU	**Lower threshold**	**Set to '0'**
	00	[15:4]	[3:0]
	01	[15:3]	[2:0]
	10	[15:2]	[1:0]
	11	[15:1]	[0]

8.20 MEMT_CFG7_TBLX (Address 0x17, bank 1-16)

Measurement configuration register 7. There are 16 independent registers corresponding to 16 measurement tables.

Table 36: Measurement configuration register 7

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
0	0	0	0	0	0	0	0	0	0	0	0	0	PRE_GAIN[2:0]		
BIT 15				BIT 8				BIT 7				BIT 0			

Field	Description	
PRE_GAIN[2:0]	Pre-demodulator gain (typical value)	
	PRE_GAIN[2:0]	**Gain (V/V)**
	X00	1
	X01	2
	X10	4
	X11	8

PRE_GAIN values X01 and X11 are not pass/fail parameters in production where limits are calculated from simulation and characterization.

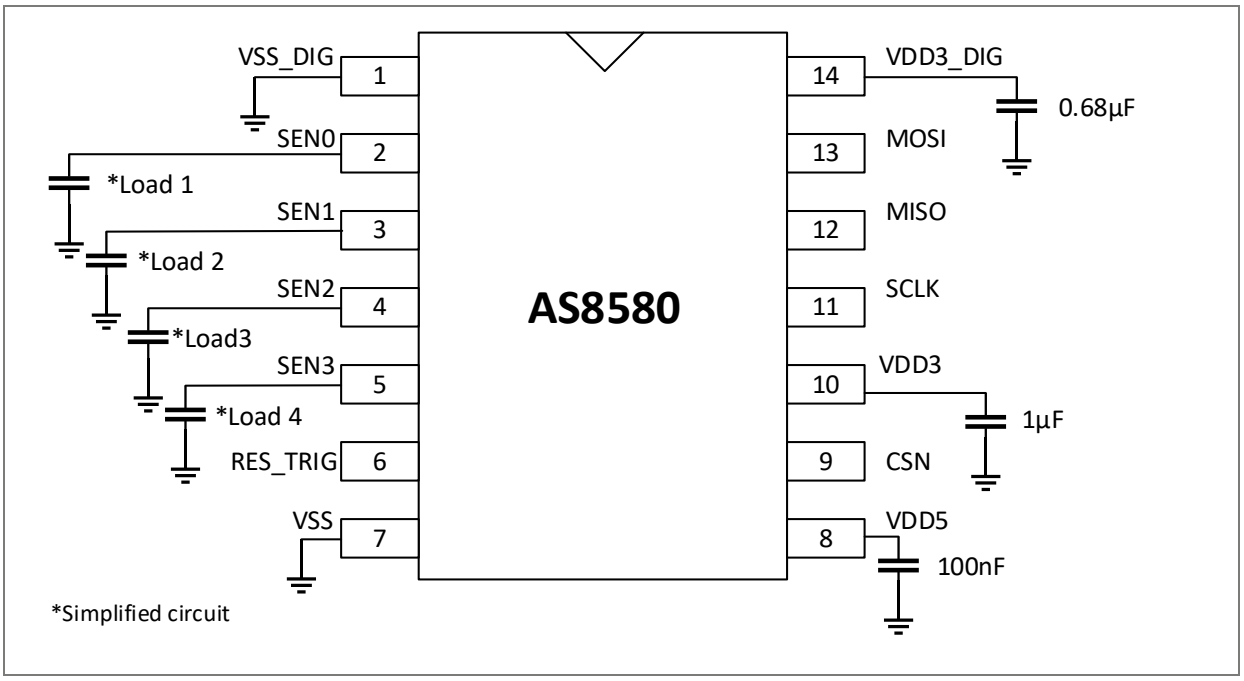
8.21 OTP (Address 0x17-0x1F, bank 17)

This register space is used to store one time programmable data.

Chip ID is stored at 0x1C:0x1E.

9 Application information

Figure 25: Application diagram

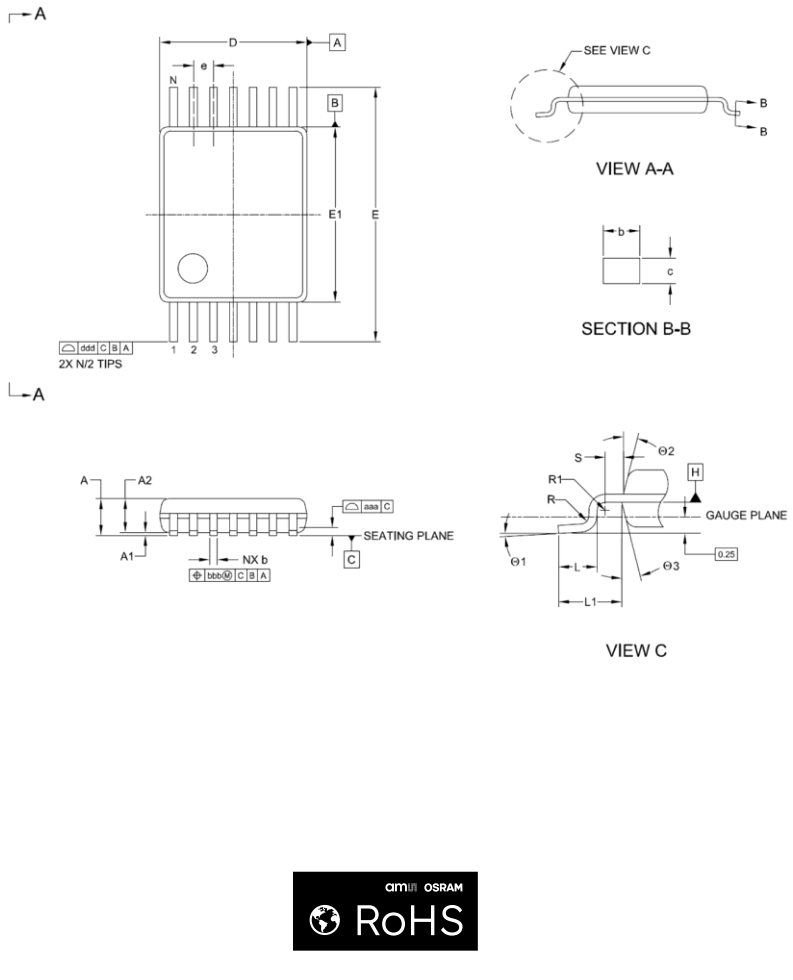


It is recommended to comply with the following rules in order to have the best performance.

- Supply filtering: The main supply capacitor has to be of low ESR-ESL type. The supply cap has to be placed as close as possible to the related sensor pin.
- Grounding: The ground plane has to be distributed following a star routing concept to provide better separation between analog and digital supply.
- Vias: Place via arrays instead of a single via.
- Digital signals: The digital bus has to be placed as far as possible from the analog signals in order to avoid signal coupling. Where not possible a ground shielding plane should be placed between the two.
- Analog signals: Sensitive analog paths have to be shielded with ground tracks to avoid coupling.

10 Package drawings & markings

Figure 26: Mechanical dimensions of TSSOP14



Ref	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E		6.40 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00REF	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	-	12REF	-
Θ3	-	12REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N		14	

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.

Figure 27: Marking of plastic production parts (top view)

YY	Last two digits of the current year
WW	Manufacturing week
M	Plant identification letter
ZZ	Letters for free traceability (defined by ams OSRAM)
@	Sublot identifier

11 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade

Other definitions

Draft / Preliminary:
The draft / preliminary status of a document indicates that the content is still under internal review and subject to change without notice. ams-OSRAM AG does not give any warranties as to the accuracy or completeness of information included in a draft / preliminary version of a document and shall have no liability for the consequences of use of such information.

Short datasheet:
A short datasheet is intended for quick reference only, it is an extract from a full datasheet with the same product number(s) and title. For detailed and full information always see the relevant full datasheet. In case of any inconsistency or conflict with the short datasheet, the full datasheet shall prevail.

Changes from previous released version to current revision v1-00	Page
Initial production version	
“Info Parameter” definition clarified on several tables	All
Minor modifications to “General Description”	5

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

12 Legal information

Copyright & disclaimer

Devices sold by ams-OSRAM AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams-OSRAM AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams-OSRAM AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams-OSRAM AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams-OSRAM AG for each application. This product is provided by ams-OSRAM AG “AS IS” and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams-OSRAM AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams-OSRAM AG rendering of technical or other services.

Product and functional safety devices/applications:
The hardware was developed in the domain of SEooC (Safety Element out of Context) using ams-OSRAM AG best system know how. The final system or target application is not known to ams-OSRAM AG. This implies, that ams-OSRAM AG does not guarantee for a system functional safety concept. The final responsibility for achieving a certain ASIL (Automotive Safety Integrity Level) in the target application is the responsibility of the system integrator.

ams OSRAM RoHS and REACH compliance statements for semiconductor products

RoHS compliant: The term “RoHS compliant” means that semiconductor products from ams OSRAM fully comply with current RoHS directives, and China RoHS. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment EU2015/863) above the defined threshold limit in the Annex II.

REACH compliant: Semiconductor products from ams OSRAM are free of Substances of Very High Concern (SVHC) according Article 33 of the REACH Regulation 2006/1907/EC; please refer to the Candidate List of Substances of ECHA here.

Important information: The information provided in this statement represents ams OSRAM knowledge and belief as of the date that it is provided. ams OSRAM bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. We are undertaking efforts to better integrate information from third parties. ams OSRAM has taken and will continue to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams OSRAM and its suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Headquarters
ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

Please visit our website at ams-osram.com
For information about our products go to Products
For technical support use our Technical Support Form
For feedback about this document use Document Feedback
For sales offices and branches go to Sales Offices / Branches
For distributors and sales representatives go to Channel Partners