Mira016

Datasheet

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Mira016 0.16 MP NIR-enhanced global shutter image sensor

1 General description

1.1 Key specifications & features

The benefits and features of Mira016, 0.16 MP NIR-enhanced global shutter image sensor are listed below:

Table 1: Key specifications

Parameter	Value	Remark
Active pixels	400 (H) x 400 (V)	
Pixel	2.79 µm × 2.79 µm	BSI stacked technology with high NIR sensitivity and QE coupled with low noise and low cross talk
Optical format	1/11.6”	
Package size (CSP)	1.79mm x 1.79mm	Active area 62% of die size
Maximum frame rate	360 fps in 10-bit mode 200 fps in 12-bit mode	At full resolution Higher fps settings upon request
	730 fps in 8-bit mode 640 fps in 10-bit mode	Special high-speed mode. Limited to 400x300 resolution
Shutter type	Voltage domain pipelined global shutter	Supports pipelined exposure and image readout
Spectrum	Mono | NIR	
Supported lens chief ray angle (CRA)	0° to 27°	
ADC resolution	8-bit | 10-bit | 12-bit	
Programmable gain	**Analog**: 1x | 2x in 12-bit mode 1x | 2x | 4x in 10-bit mode 1x | 2x | 4x | 8x | 16x in 8-bit mode **Digital**: In 1/16th increments	Higher analog gains and finer gain tuning are available upon request
Data interface	MIPI CSI-2 v1.3 DPHY v1.2 1 Data lane | 1 Clock lane	1.5Gbps with data scrambling support

Table 2: Added value of using Mira016

Features	Benefits
High sensitivity and NIR enhanced pixel	High sensitivity and compact pixel size achieved via state-of-the-art BSI technology with NIR enhancement allowing to use lower power illuminators
Context switching	Two register contexts for on-the-fly configuration changes to exposure and readout settings without interrupting the video stream
On-chip processing	• Defect pixel detection and correction on-chip • Image statistics histogram can be output • Event detection • In-pixel background light cancellation • Digital pixel binning • Black sun protection • Flexible ROI selection (incl. mirroring, flipping, cropping & subsampling) • Automatic black level calibration
On-chip advanced power management	Smart powering of on chip blocks with respect to frame rate and exposure time resulting in extended battery life
On-chip temperature sensor	Accurate temperature reading on junction temperature
Illumination synchronization trigger	Accurate timing between illumination and actual exposure
Fast ADC with analog and digital CDS	Low column FPN, low 1/f noise and high fps

Table 3: Key electro optical parameters (Typical)

Parameter	Value	Remark
Full well charge (FWC)	10300e-	
Dark temporal noise (DTN)	6.1e-	10-bit, 2x analog gain
Shutter efficiency (dB)	-93dB -123dB	@940nm @550nm
Dark current (DC)	66e-/s	60°C
Quantum efficiency (QE)	95% 56% 36%	@550nm @850nm @940nm
Active power consumption	33.3mW @ 120fps, 10-bit 7.4mW @ 15fps,10-bit	Advanced on-chip power management adjusts power to various parts of the chip based on frame rate. Lower power modes available upon request
Standby power consumption	<300µW	

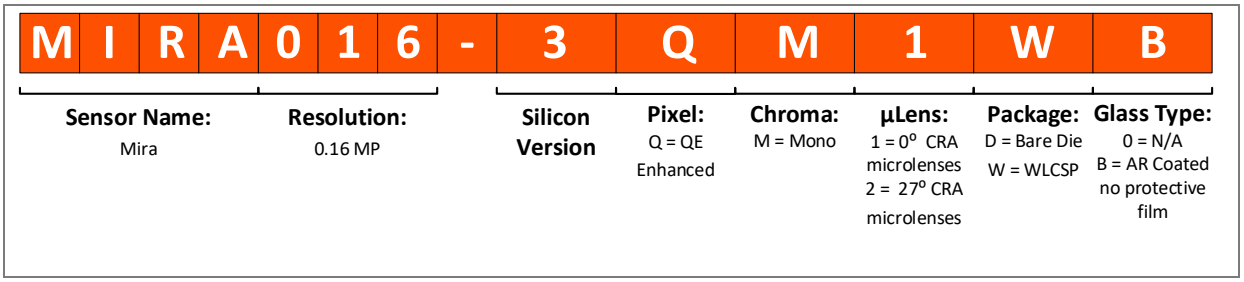
1.2 Applications

- Active stereo vision
- Structured light vision
- Eye tracking
- Head tracking

2 Ordering information

Product type	Ordering code	Package	Delivery form	Color filter	Delivery quantity
Mira016-3QM1WB	Q65113A7951	CSP	Reel	Mono	2000 pcs/reel
Mira016-3QM2WB	Q65113A7962	CSP	Reel	Mono	2000 pcs/reel
Mira016-3QM1D0	Q65113A8228	Bare die	RW		

Figure 1: Product code description



3 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at absolute maximum rating conditions is not implied, nor at any other conditions beyond those indicated under “Operating Conditions”.

Table 4: Absolute maximum ratings of Mira016

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Electrical parameters						
VDD28	Analog and pixel supply voltage			3.3	V	
VDD11	Core supply			1.26	V	
I_{SCR}	Input current (latch-up immunity)		± 100		mA	JESD78E 90°C
VI	Digital input voltage level	-0.3		4.125	V	
Electrostatic discharge						
ESD_{HBM}	Electrostatic discharge HBM			± 2	kV	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM			± 500	V	JS-002-2018
Temperature ranges and storage conditions						
R_{THJP}	Junction to package thermal resistance		3.3		°C/W	
T_J	Operating junction temperature	-30		90	°C	
T_{BODY}	Package body temperature			260	°C	IPC/JEDEC J-STD-020 (1)
	Number of reflow cycles			3		Due to the small pad pitch, standard reflow process may need to be adjusted to achieve reliable solder result.
T_{DRY}	Recommended dry bake temperature	105		125	°C	
t_{DRY}	Recommended dry bake time	8		24	h	125 °C
MSL	Moisture sensitivity level		3			Represents a floor lifetime of 168 h
RH_{NC_CSP}	Relative humidity (non-condensing) for CSP	5		85	%	
RH_{NC_RW}	Relative Humidity (non-condensing) for RW			30	%	
T_{STRG_CSP}	Storage temperature for CSP	-40		85	°C	
T_{STRG_RW}	Storage temperature for RW	17		28	°C	
t_{STRG_CSP}	Storage time for CSP			1	year	According to MSL3
t_{STRG_RW}	Storage time for RW			3	months	Refers to indicated date of packaging

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn)

4 Electrical characteristics

Table 5: Electrical characteristics of Mira016

Symbol	Parameter	Min	Typ.	Max	Unit
Continuous power dissipation					
P_T	CPD@360 fps,10-bit, 0.16 MP		55		mW
P_T	CPD@15 fps, 10-bit, 0.16 MP		7		mW
Power supplies					
VDD28	Analog supply voltage	2.7	2.8	2.9	V
VDD11	Core supply voltage	0.99	1.1	1.21	V
IDD28	Analog supply current			60	mA
IDD11	Core supply current			60	mA
Digital I/O					
VIH	High level input voltage	0.8× VDD11 *(0.88)*	VDD11	1.85(1)	V
VIL	Low level input voltage			0.2× VDD11 *(0.22)*	V
VOH	High level output voltage	0.7× VDD11		VDD11	V
VOL	Low level output voltage	VSS11		0.3× VDD11	V
treq_exp	REQ_EXP pulse width	2xCLK_IN periods			
treq_frame	REQ_FRAME Pulse Width	2xCLK_IN periods			
Reference clock					
fCLK_IN(2)	CLK_IN frequency	12	24	64	MHz
DCCLK_IN	CLK_IN duty cycle	45	50	55	%
C-Cjitter,CLK_IN	CLK_IN cycle-to-cycle jitter			100	ps
trise/fall,CLK_IN	Rise and fall transition time			5	ns

(1) In case of input signal level >1.5 V, a 22 kOhm resistor and below 1 MOhm is necessary in series between RST_N pin and external RST_N signal.

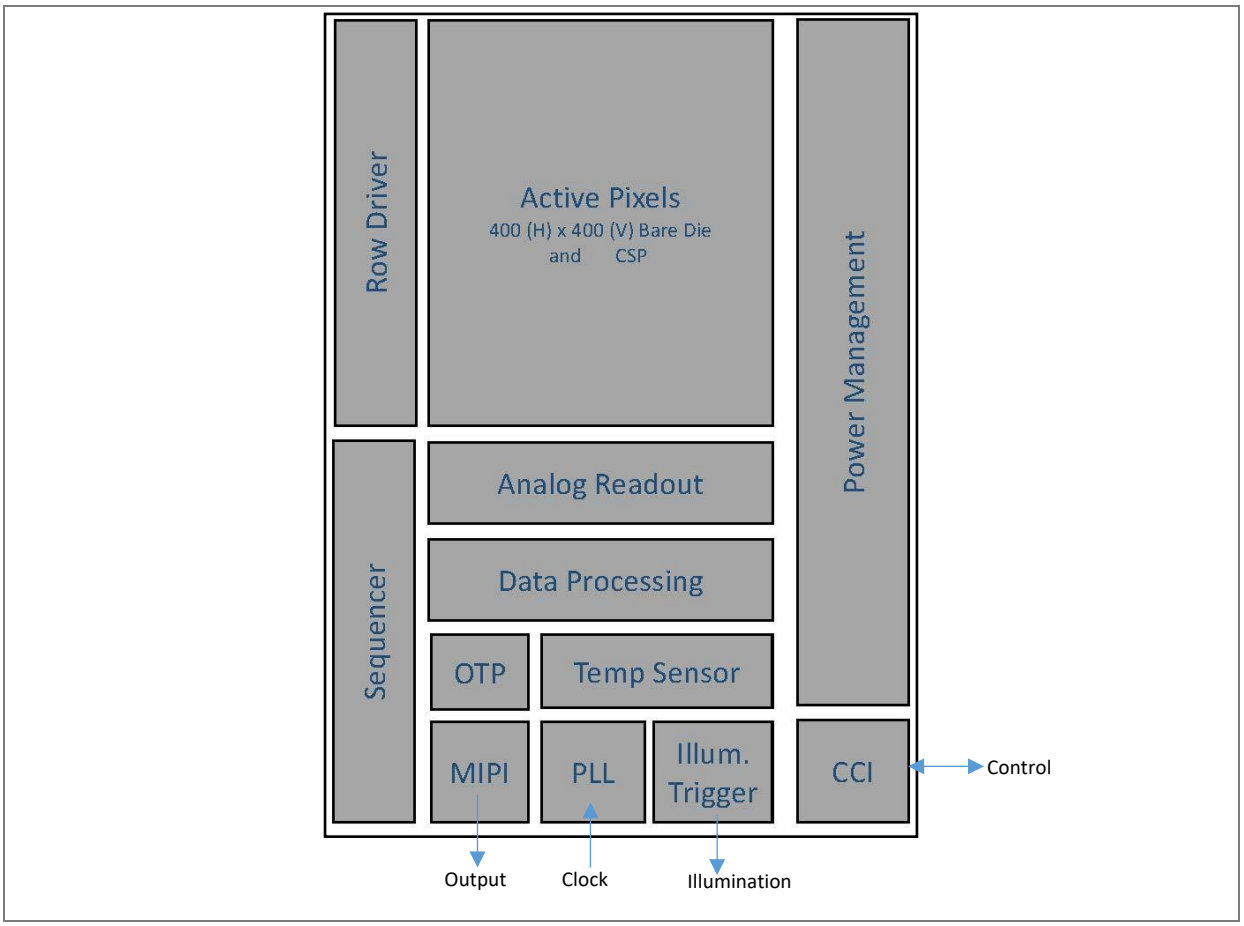
(2) The MIPI block requires an escape clock frequency between 12 MHz and 20 MHz (excluding the boundary conditions of 12 MHz and 20 MHz). Given the PLL architecture the input clock ranges between 20 MHz < fCLK_IN < 24 MHz should not be used (both boundaries 20 MHz and 24 MHz can still be used).

5 Functional description

This section provides a brief overview of the functionality of the different blocks in the sensor's architecture as depicted in Figure 2 and introduces some special operating modes. For more details, please refer to the product description PD001058.

5.1 Sensor architecture

Figure 2: A high-level representation of the Mira016



The sensor is compliant to the MIPI CSI-2 v1.3 protocol interface and the D-PHY v1.2 physical layer specifications to transmit the image data to the host processor. It uses one data lane and one clock lane operating up to 1.5 Gbps.

To configure the operation of the sensor, registers need to be programmed through the CCI (Camera Control Interface) interface. This interface is fully compliant with the CCI standard which is a subset of the I²C standard and compatible with an I²C bus.

An on-chip sequencer generates all internal timing required by the row driver and pixel array to acquire images and output the data through the analog readout, the digital data processing and finally off-chip through the MIPI interface. The sequencer itself is programmed through the CCI interface. Streaming of images or video can be triggered either through an IO pin or through the CCI interface.

The power management module minimizes the power consumption of the sensor whenever possible.

The on-chip PLL transforms a low-frequency CMOS input clock into all high-frequency clocks needed to operate the sensor.

The sensor supports controlling other components in the system. It has dedicated outgoing signals for system synchronization between the image sensor itself and an external illumination component (i.e. a NIR illuminator).

The integrated temperature sensor allows for device temperature measurements by the user.

A non-volatile, 8 kbit One Time Programmable memory is included on-chip. Part of this memory is used by ams OSRAM to store a unique device ID and sensor calibration data; the other part is available to the customer.

5.2 Special operating modes

5.2.1 On-chip background light cancellation

When it needs to operate under extremely bright background conditions, the sensor can be put in background light cancellation mode. In this mode, two exposures are performed consecutively. A first exposure is performed without activating any external illumination and captures the information of the background scene. A second exposure follows with the external illumination active. This exposure contains information about the background light and that of the external illumination. The signal of the second exposure is stored and subtracted from the first exposure to cancel out the background light. The operation is done on-chip, so a single readout provides the background-light-free image to the external processor, halving power consumption or doubling the frame rate compared to off-chip background light cancellation methods. For details, please refer to 6.7.1 and 6.8.4 with more information in the user guide.

5.2.2 On-chip event detection

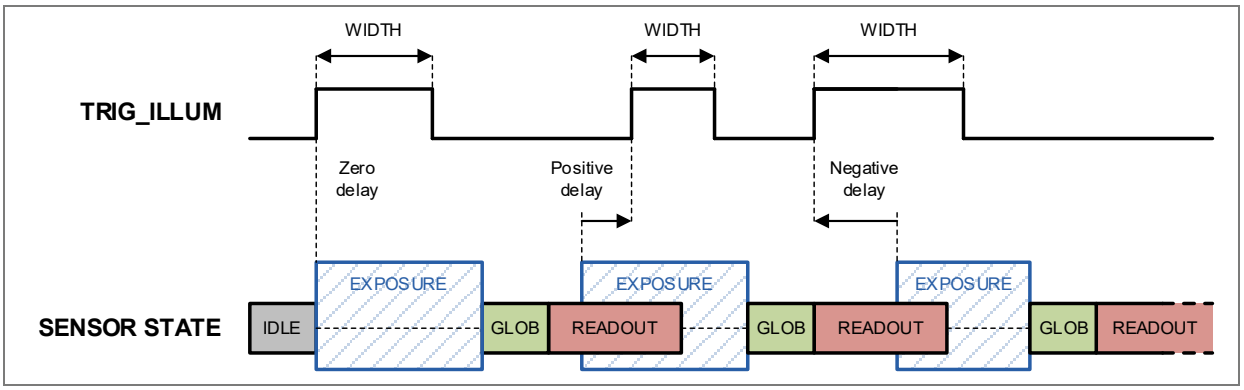
The on-chip event detection can be used for numerous applications but is mainly intended for supporting a *Sensing Mode* (or auto wake-up mode). In this mode, the sensor runs at a low frame rate with low power consumption. When an event is detected, the sensor autonomously switches the active context to enable high frame rate readout (full performance). For details, please refer to the user guide.

5.2.3 Illumination trigger

The illumination trigger (TRIG_ILLUM) output pin can be used to control an off-chip driver for a flash or illumination device. The trigger is synchronized to the exposure of the pixel array. The delay between the trigger and the exposure phase can be programmed, as well as the width of the trigger signal.

Figure 3 shows how the TRIG_ILLUM signal can be positioned with respect to the sensor's exposure phase. The delay is the time between the TRIG_ILLUM rising edge and the start of exposure on the pixel array. The width is the high time of the TRIG_ILLUM signal.

Figure 3: Illumination trigger



The illumination trigger is synchronized to the actual exposure on the pixels. Any latency between external requests and start of exposure on the pixels is automatically taken into account.

5.2.4 Low power mode (Power Management Unit - PMU)

The sensor automatically uses a smart low power mode of functionality which considerably reduces the overall power consumption of the sensor. This functionality is most efficient when high data rate mode is used (e.g. 1.5 Gbps). In such mode, the sensor quickly sends the frame data off-chip then enters low power mode until a next frame is needed, reducing the power consumption almost linearly with the fps decrease.

5.3 Readout delay

For easy integration with complex systems, where two image sensors are connected to a single MIPI receiver, the sensor has an on-chip delay mechanism that allows the delay of the readout of one of sensors, until the readout of the other is finished.

6 Operating the sensor

This chapter shows the basics of how to operate the sensor and introduces the user to the sensor's interfaces. For more details, please refer to the user guide.

6.1 Power supplies

6.1.1 External power supplies

To power the sensor two externally generated supplies are required as listed in Table 5. Avoid using switching power supplies, especially for the analog supplies. Please ensure that enough current is supplied to the sensor during startup as shown in Table 5.

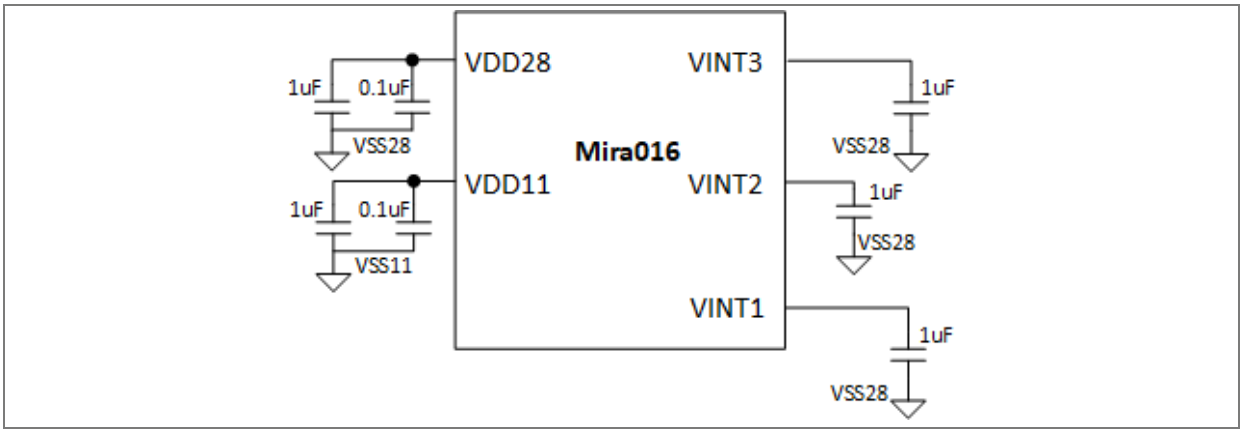
For optimal noise performance, it is advised to keep the analog and digital ground nets separated and connect them together as close as possible to the external supply regulators.

The local decoupling needs to be repeated for each pin per supply on bare die.

6.1.2 Biasing (on-chip regulators)

Operating the pixel and readout layer requires multiple supply levels. These levels can be generated using on-chip regulators. The regulator output voltages are controlled using the CCI interface. Each supply regulator requires decoupling by using at least 1 µF capacitor. Figure 4 shows the voltage regulator pins that need to be decoupled using capacitors.

Figure 4: Regulator decoupling and biasing



6.2 Power-up/down sequence

Attention:

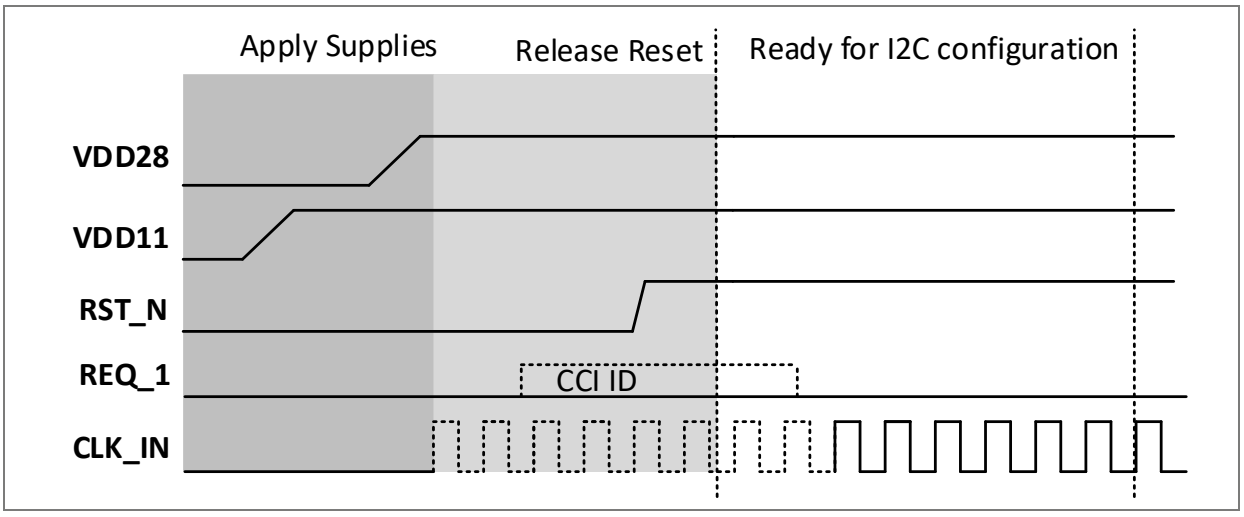
A specific order and timing must be applied to the sensor supplies to guarantee a proper power-up/power-down sequence and to avoid peak currents.

Please ensure that enough current is supplied during startup as shown in Table 5.

6.2.1 Power-up sequence

1. Apply VDD11 supply and allow the supply to finish ramping.
2. Apply VDD28 and allow the supply to finish ramping.
3. Drive REQ_1 pin to 0 or 1 depending on desired CCI_ID to change the device address.
4. Release the hard reset signal on the RST_N pin.
5. Apply the external clock on the CLK_IN input (note steps 4 and 5 are interchangeable).
6. Drive REQ_1 pin back to 0
7. I²C communication is now available to configure the sensor and start image acquisition.

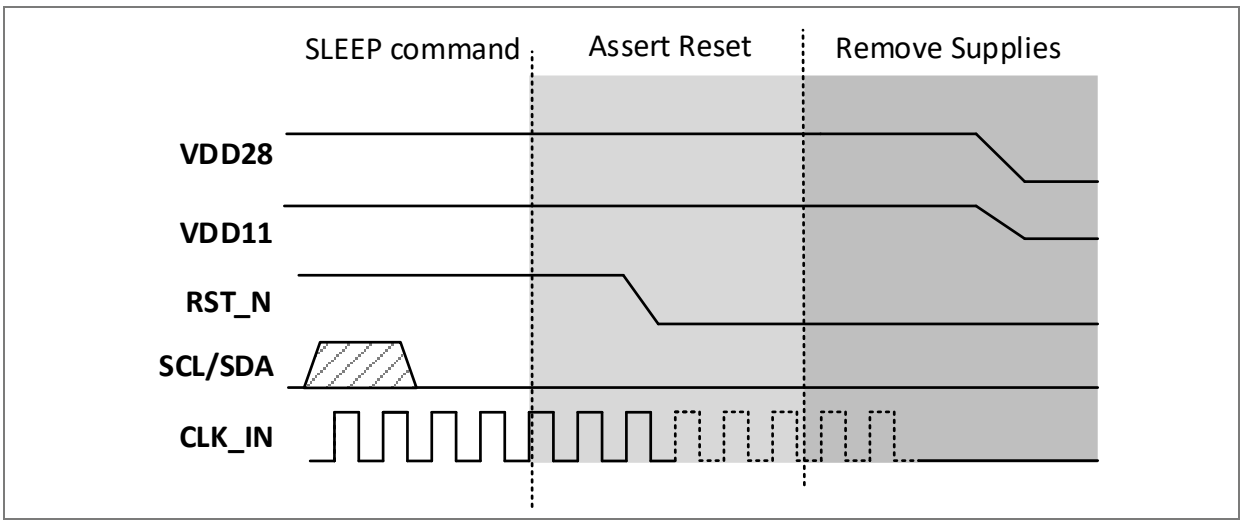
Figure 5: Power-up sequence



6.2.2 Power-down sequence

1. Use CCI to send a sleep command
2. De-assert the RST_N input pin
3. The external clock on CLK_IN pin can now be disabled
4. Disable VDD28 and VDD11

Figure 6: Power-down sequence



6.3 Clocking

The sensor has two CMOS clock inputs: CCI_SCL and CLK_IN. CCI_SCL is part of the CCI used to configure the sensor. All other internal sensor clocks are derived from the PLL, taking CLK_IN as input clock. Refer to Section 3 for the electrical specifications of the input clocks.

6.4 Camera control interface (CCI)

The serial Camera Control Interface (CCI) interface (defined in the MIPI CSI2 specification CSI-2-v1.3) provides read and write access to control and status registers within the sensor.

Mira016 image sensor always operates as a CCI slave on the CCI bus.

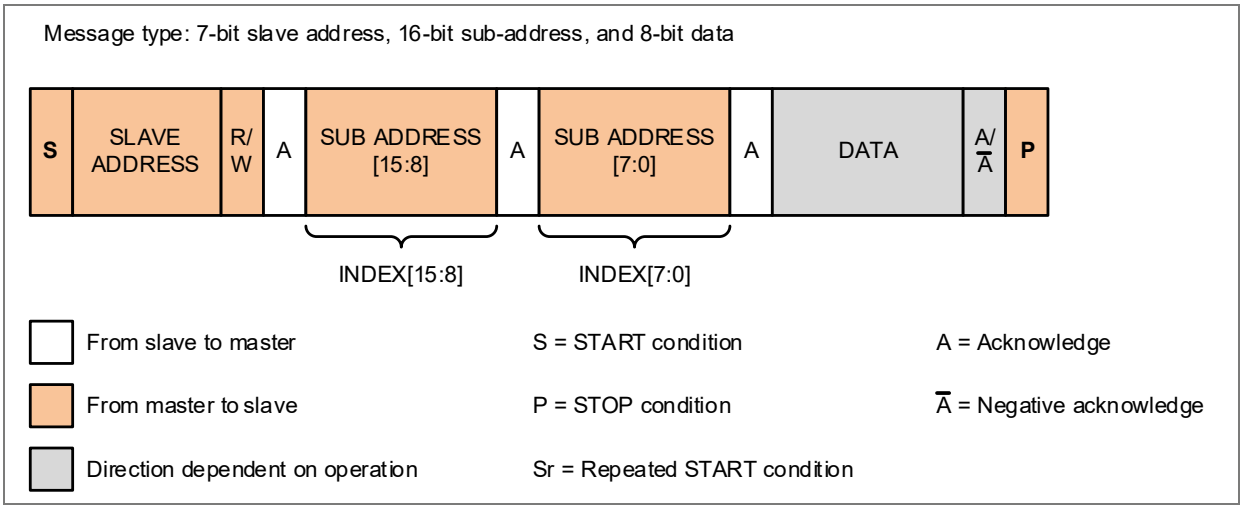
The 7-bit slave address of Mira016 is 011011X, where the last bit 'X' is the CCI_ID which can be configured to either 1 or 0 during the startup in order to connect two Mira016 image sensors on a single bus.

CCI is a subset of the I²C protocol, using two wires SCL and SDA to carry the clock and data respectively. Therefore, the Mira016 can also be connected to the system I²C bus. Care must be taken so that I²C masters do not try to utilize I²C features which are not supported by CCI devices. For this reason, there is typically a dedicated CCI interface between the sensor and the host system.

6.4.1 Message format

Figure 7 shows the general CCI message format. The sensor uses 16-bit sub-address (index) with 8-bit data, which means every 8 bits of data is followed by an ACK/NACK. A message may contain multiple 8-bit data fields if a multi-byte register is accessed. Every CCI transaction starts with a ***start condition*** and ends with a ***stop condition***. The ***repeated start*** condition is only used in read operations starting from a random address location.

Figure 7: CCI message format



The sensor contains many registers of different sizes. Multi-byte registers have their most significant byte located at the lowest address and their least significant byte located at the highest address (i.e. big-endian byte format). Partial access to multi-byte registers is not allowed. Use sequential read/write operations to access multi-byte registers.

6.4.2 Read and write operations

The Mira016 supports four different read operations and two different write operations from the CCI specification:

1. Single write to random location
2. Single read from random location
3. Single read from current location
4. Sequential write to random location
5. Sequential read from random location
6. Sequential read from current location

Please refer to the user guide for detailed information.

6.4.3 Timing characteristics

The CCI timing diagram is shown in Figure 8. The timing specifications are shown in Table 6.

Figure 8: CCI timing diagram

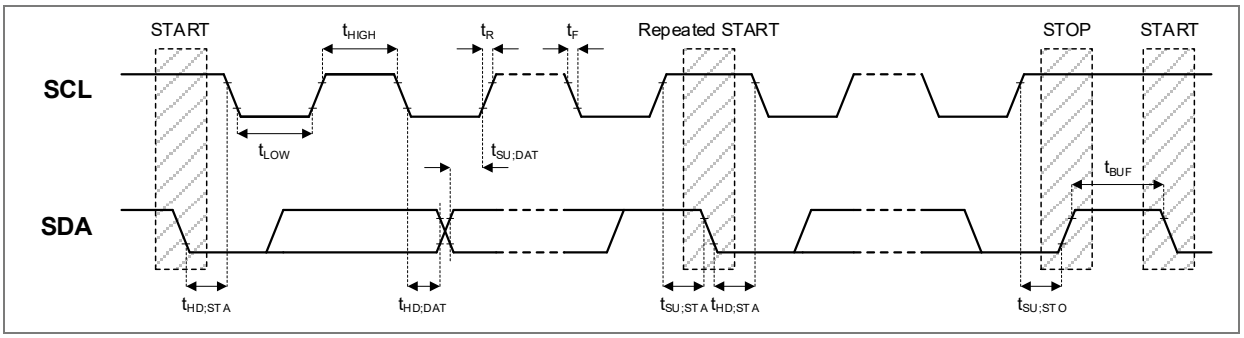


Table 6: CCI timing specification

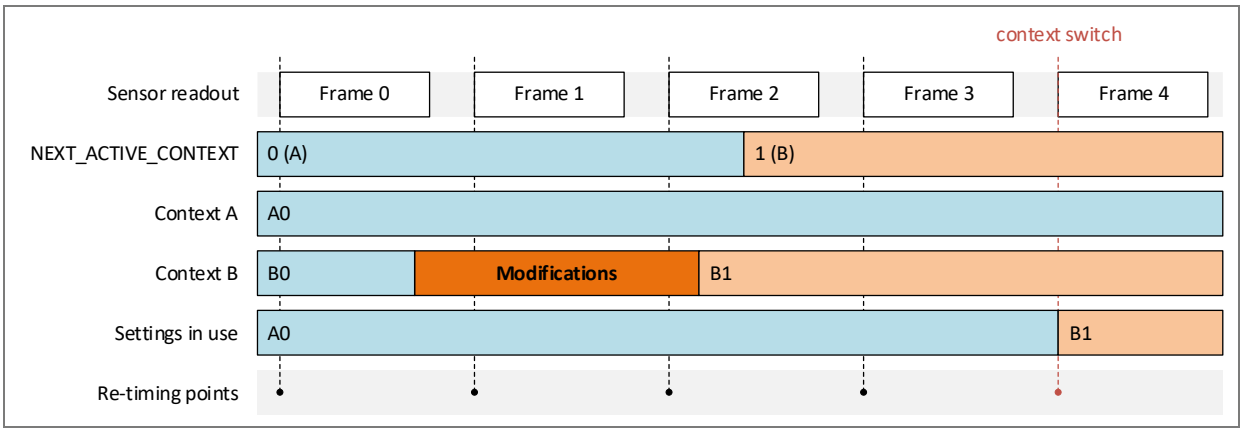
Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	-		400	kHz
t_{LOW}	LOW period of the SCL clock	1.3		-	µs
t_{HIGH}	HIGH period of the SCL clock	0.6		-	µs
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6		-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6		-	µs
$t_{HD;DAT}$	Data hold time	0		-	µs
$t_{SU;DAT}$	Data setup time	0.1		-	µs
$t_{SU;STO}$	Setup time for STOP condition	0.6		-	µs
t_R	Rise time of both SDA and SCL signals	-		0.3	µs
t_F	Fall time of both SDA and SCL signals	-		0.3	µs
t_{BUF}	Bus free time between a STOP and START condition	1.3		-	µs

6.4.4 Context switching

Some register settings are “context switchable”, which means they are derived from one of the sensor’s context banks. Mira016 supports two contexts, named A and B. **Context switching** changes the active context, causing all context switchable registers to take their value from the new context bank. The sensor always applies the new settings on a frame boundary, regardless of when the user initiates the context switch.

Figure 9 shows an example of a context switch. The sensor is streaming images with settings derived from context A. The user prepares a new set of settings by modifying an inactive context (B). These modifications do not influence the current sensor operation. When the new settings are written to the sensor, the user initiates a context switch by changing the NEXT_ACTIVE_CONTEXT register to value 1 (context B). The sensor retimes the context switch to a frame boundary (frame 4 in this example) to make sure all exposure and readout settings are consistent in the output frames.

Figure 9: Context switch



The re-time mechanism can be disabled to switch the active context when the sensor is not streaming.

The following settings are context switchable and can be set independently per context.

- Exposure/frame settings
  - Exposure time
  - Frame time
  - Number of frames in an acquisition sequence
  - Illumination trigger alignment
- Region of interest (ROI)
  - One programmable horizontal window
  - Up to 10 programmable vertical windows-
  - Subsampling in X and Y direction
  - Binning in X and Y direction
  - Mirroring in X and Y direction
- Digital gain
- Enable/disable of different features
  - Illumination trigger
  - Synchronization trigger

  - On-chip event detection
  - On-chip histogram generation
- Data transmission options
  - Pixel data + histogram data (when enabled)
  - Histogram data only

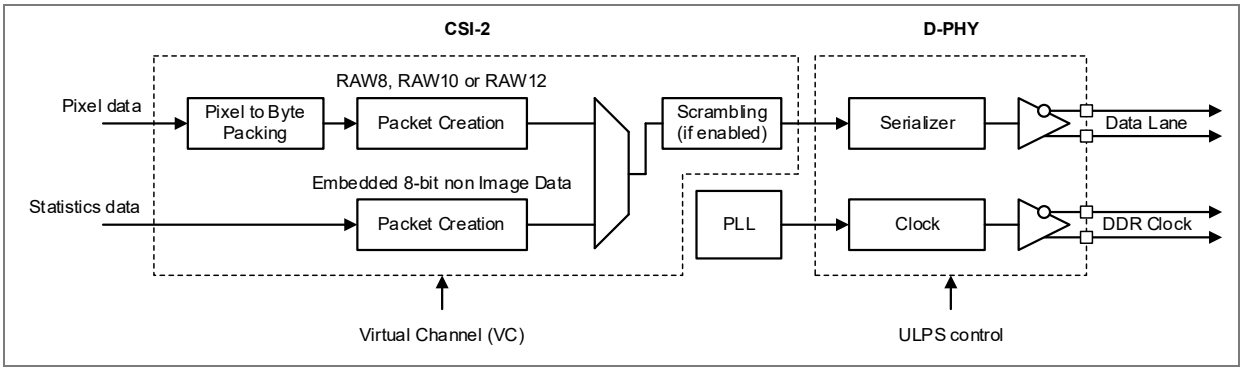
6.5 CSI-2 and D-PHY

The sensor's MIPI interface consists of a CSI-2 protocol layer combined with a D-PHY physical layer. The type of data lane used is a CIL-MFEN. The type of clock lane used is a CIL-MCNN.

Figure 10 shows an overview of the output data interface. The pixel data is transmitted as RAW8, RAW10, or RAW12 CSI-2 packets. The packet type depends on the bit depth. If on-chip statistics gathering is enabled, it is transmitted as "Embedded 8-bit non Image Data" at the end of each frame. The user can set the Virtual Channel to be used for all data packets. The generation of Line Start and Line End packets depends on the selected frame mode.

The sensor supports data scrambling, which requires CSI-2 v2.0 compatibility.

Figure 10: MIPI output interface overview



The D-PHY layer serializes the CSI-2 packets and transports them to the receiving system on a single data lane. The D-PHY clock lane transports a DDR clock that is used by the receiving system to sample the data on the data lane. This clock lane can operate in continuous or non-continuous mode. The clock lane and data lane both support Ultra-Low Power State (ULPS).

All DPHY-v1.2 data rate dependent timing parameters are adjustable through register settings. This ensures that the timing specifications on the interface can be met when operating the sensor in different modes or at different output data rates.

The following sub-sections provide more details on the supported CSI-2 and D-PHY features, with more details in the User Guide.

6.5.1 Frame mode

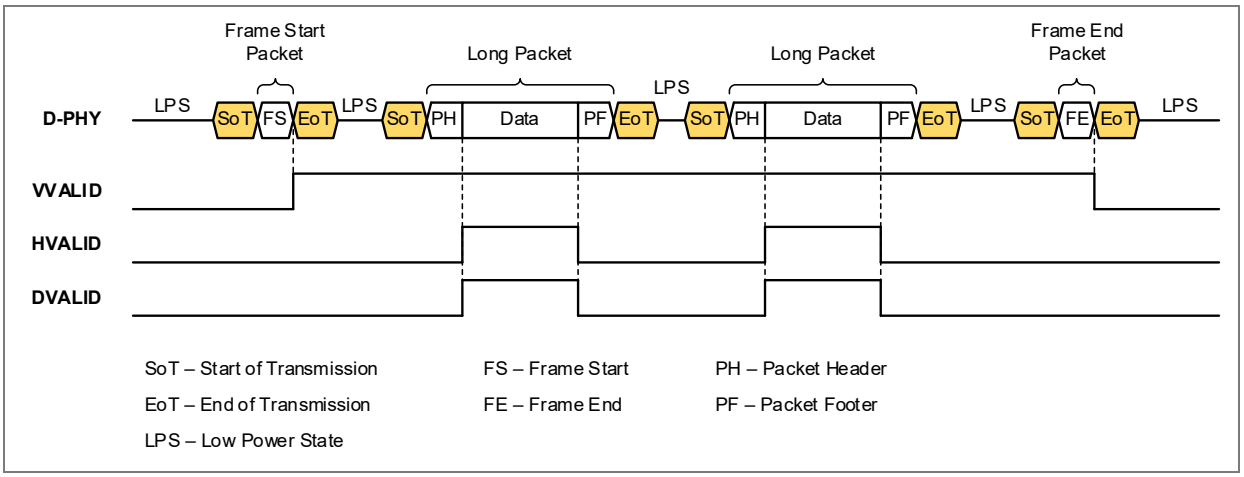
The frame mode determines whether the output interface inserts Line Start and Line End packets in the data stream. Two frame modes are available:

- Global timing mode
- Accurate timing mode

By default, the sensor operates in global timing mode, which means that Line Start and Line End packets are not generated. Figure 11 shows an example of a frame with two rows, transmitted on the output interface in global timing mode.

Note that the VVALID, HVALID and DVALID signals in the figure are only concepts to help illustrate the behavior of the packets on the interface. These signals are not part of the output interface and are not generated by the sensor.

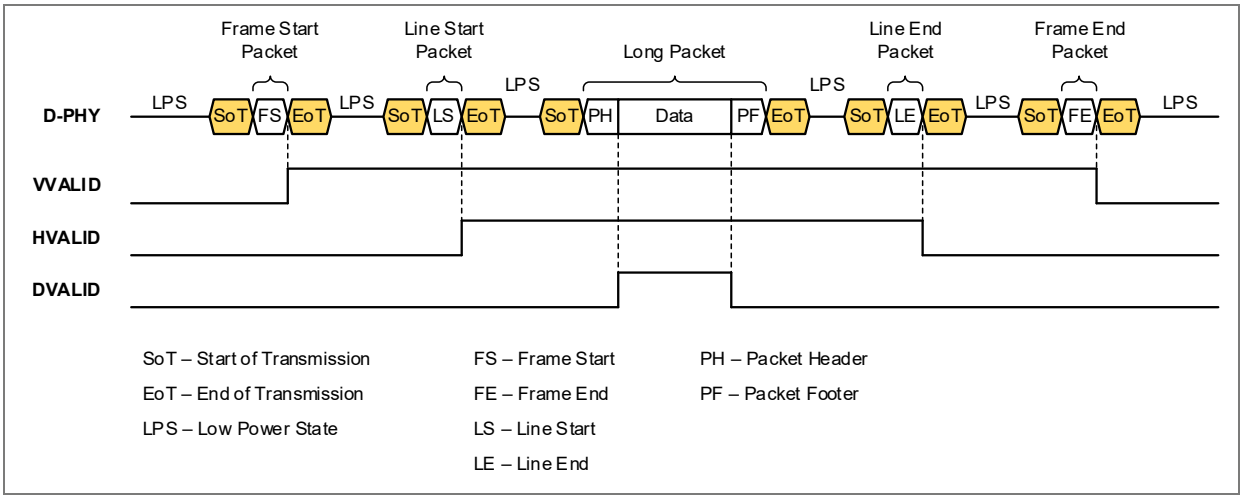
Figure 11: Frame mode – global timing mode



When using *accurate timing mode*, each data packet is surrounded by a Line Start and Line End packet pair. Figure 12 shows an example of a frame with one row, transmitted on the output interface in accurate timing mode.

Accurate timing mode increases the line time and possibly decreases the maximum achievable frame rate. This is due to the additional time it takes to transmit the Line Start and Line End packets. Power consumption will be higher due to increased high-speed activity on the D-PHY lanes.

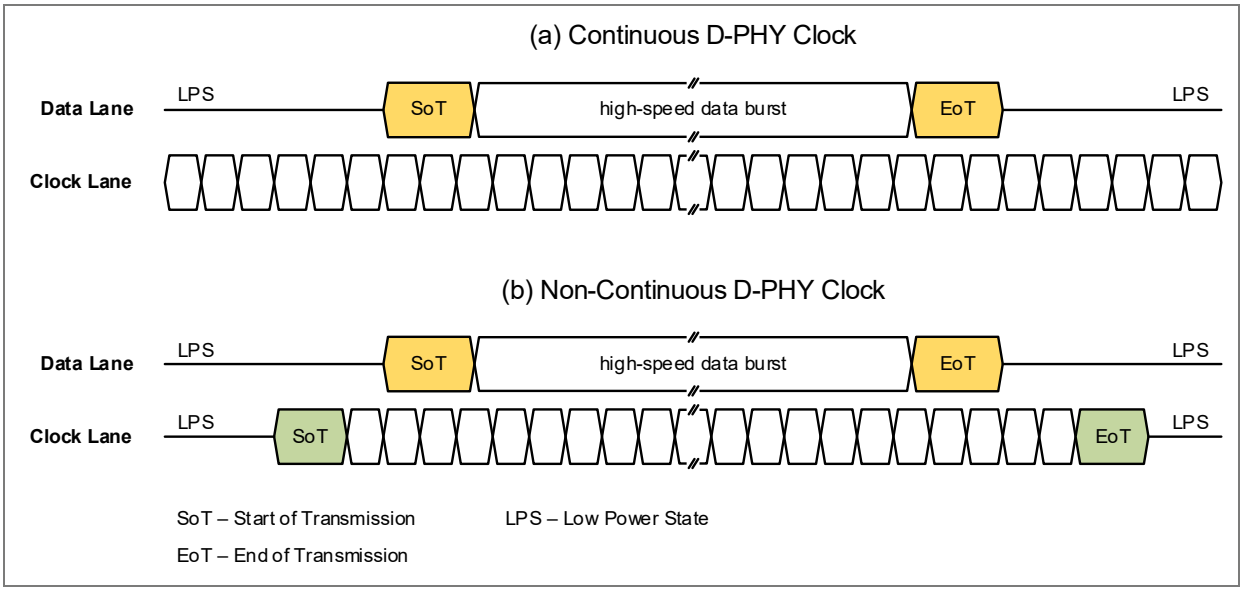
Figure 12: Frame mode – accurate timing mode



6.5.2 Continuous and non-continuous D-PHY clocking

The D-PHY clock lane can operate in continuous or non-continuous mode as shown in Figure 13. In *continuous clock mode*, the clock lane remains in high-speed mode between data bursts. The clock lane starts transporting a DDR clock as soon as the output interface is properly initialized and remains in high-speed mode indefinitely. In *non-continuous clock mode*, the clock lane goes to Low Power State in between data bursts. The clock lane exits Low Power State prior to the transmission of a high-speed data burst on the data lane. It re-enters Low Power State after the high-speed data burst is completed. Note that the Start of Transmission (SoT) and End of Transmission (EoT) sequences are different for the clock and data lane.

Figure 13: Continuous and non-continuous clock mode



The choice between continuous and non-continuous clock mode is a trade-off between power, throughput and receiver complexity. Using continuous D-PHY clocking is straightforward and allows the highest data throughput, but it consumes more power as the clock lane is also running when no data is being transmitted.

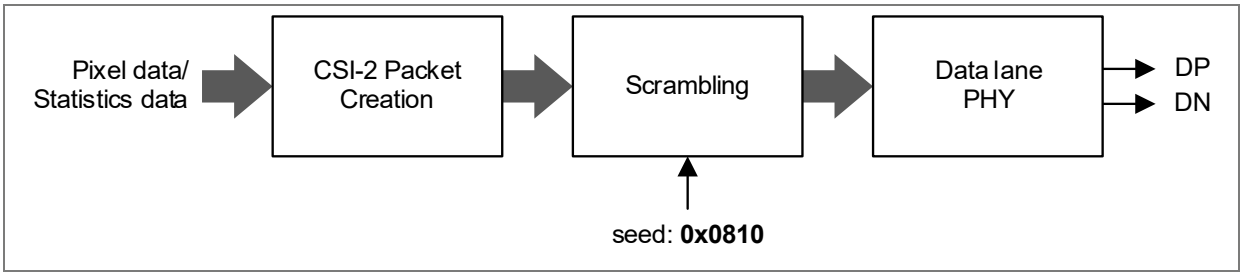
6.5.3 Data scrambling

Data scrambling is a CSI-2 version 2.0 feature.

Data scrambling is a technique used to mitigate the effects of EMI and RF self-interference by randomizing the data in the CSI-2 packets. Figure 14 gives a high-level overview of the data scrambling used in the output interface. When enabled, the long packet header, data payload, long packet footer, and short packets are scrambled before they are transmitted across the D-PHY data lane. Scrambling applies to pixel data and statistics data (if enabled). Data scrambling does not affect the D-PHY clock lane.

The lane seed value used to initialize the scrambler is 0x0810.

Figure 14: Data scrambling



6.6 Reset

The sensor has two reset states, called *hard reset* and *soft reset*. In the hard reset state, the entire sensor is reset. This includes resetting the CCI interface and internal register banks. All registers will be reset back to their default value. In the soft reset state, the entire sensor is reset, except for the CCI interface and internal register banks. All registers will retain their values. All static register configuration is done while the sensor is in soft reset state.

Hard reset state is entered by asserting the asynchronous reset input pin (RST_N) low. Note that CCI communication is not possible until the RST_N pin is de-asserted high.

Soft reset state is entered and exited through CCI write operations.

6.7 Image acquisition

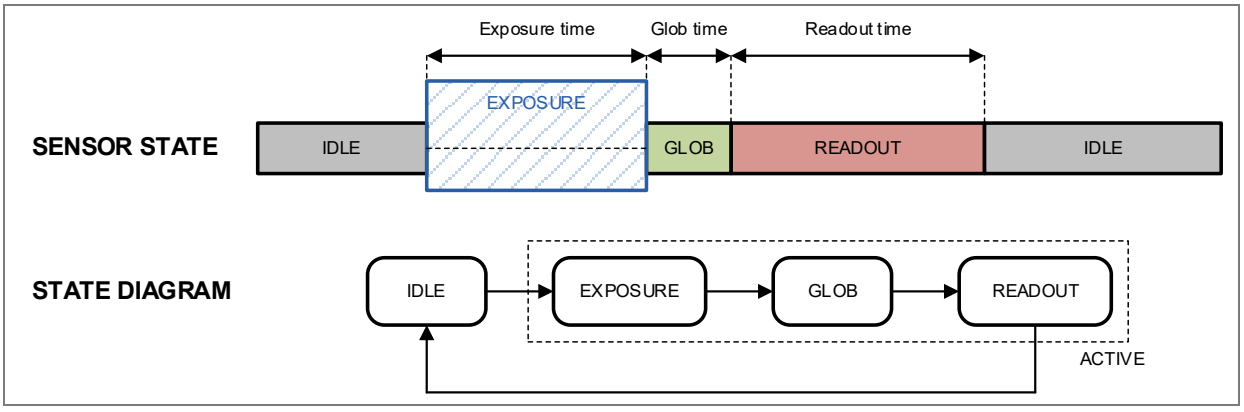
This section gives a general overview of the sensor's image acquisition. It explains important concepts, which the user needs to understand in order to configure the sensor correctly. These concepts also help in understanding the sensor's possibilities and limitations.

The image acquisition consists of several phases that are reflected by the sensor's state. The sensor can be in any of the following states:

- **IDLE**: The sensor awaits external requests.
- **ACTIVE**: The sensor is acquiring a frame. This state has three sub-states, called EXPOSURE, GLOB and READOUT.
  - **EXPOSURE**: The global shutter is opened, and photons are accumulated in the pixels. The length of this state is called the *exposure time*. This total accumulation or integration of incident light over the exposure time is called the *integrated pixel value*.
  - **GLOB**: The global shutter is closed by sampling all integrated pixel values. The length of this state is called the *glob time*. The glob time is a constant for a given use case.
  - **READOUT**: The acquired frame with metadata and mandatory overhead is read out. The length of this state is called the *readout time*.

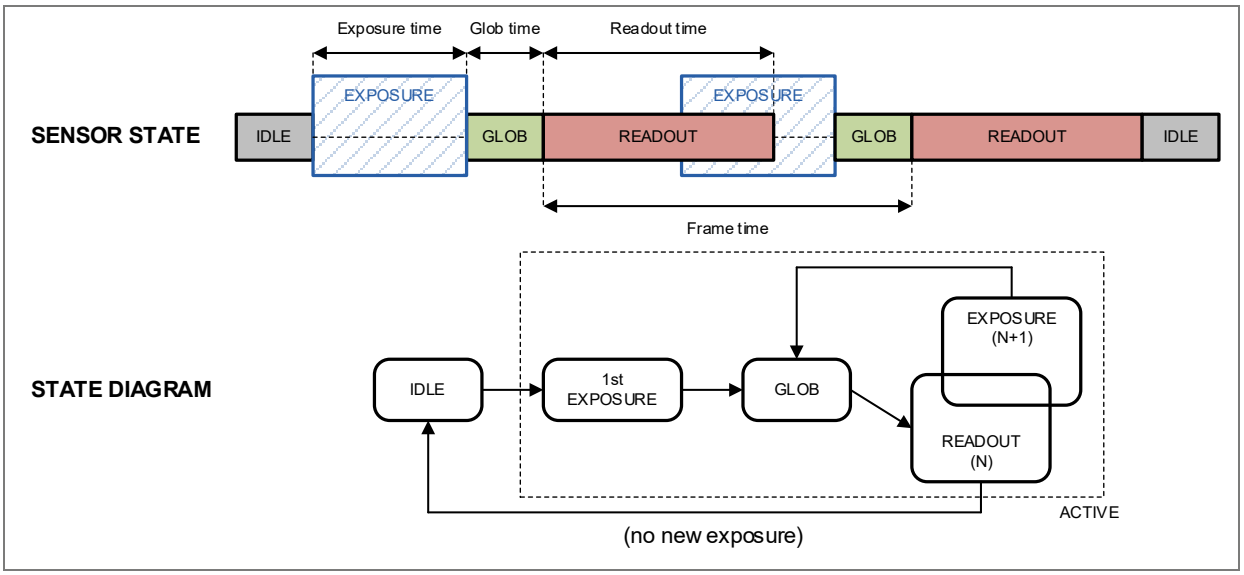
During image acquisition, the sensor moves through several states, as shown in Figure 15. After an external request, the sensor goes through a sequential succession of EXPOSURE – GLOB – READOUT to grab a single image. After this cycle, the sensor moves back to IDLE, waiting for new requests. Since only one frame is captured before returning to IDLE, this mode of operation is referred to as *sequential operation*. This means that the sensor moves through the states in a sequential manner, with only one state activated at any given time.

Figure 15: Sequential image acquisition



When multiple frames are acquired back-to-back without passing through IDLE state, the sensor operates in *pipelined mode*, as shown in Figure 16. In this mode, the sensor can be in the EXPOSURE state and READOUT state at the same time. While the readout of frame N is busy, the exposure of frame N+1 is already started. The EXPOSURE can partially overlap or fully overlap with the READOUT state. The time between two consecutive frames is called the *frame time*.

Figure 16: Pipelined image acquisition



Depending on the selected Sensor Control Mode, the exposure time and frame time are controlled through external timing or through register settings. Refer to section 6.8 for more information on the Sensor Control Modes. The readout time depends on the selected data rate, output interface configuration and region of interest.

6.7.1 Background light cancellation

Background Light Cancellation is a special sensor acquisition mode designed to handle very bright background conditions. As introduced in section 5.2.1, this involves two exposures, with an external illumination source alternatingly turned on or off, followed by a single image readout of the on-chip calculated difference image.

Information:

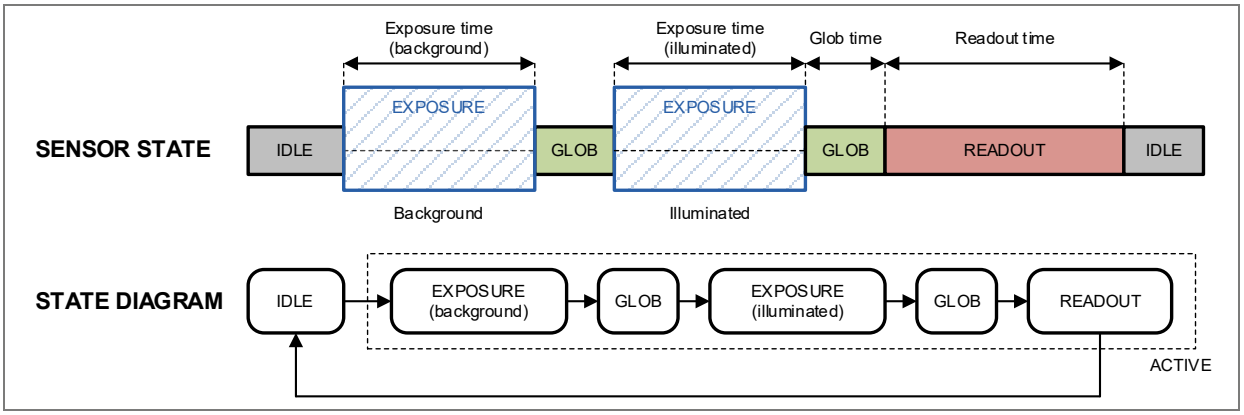
Use the sensor's Illumination Trigger to synchronize the external illumination source to the exposure of the illuminated scene. Section 5.2.3.

Image acquisition in Background Light Cancellation mode is different from the normal operating mode as two exposure phases are needed for each readout. Each exposure is followed by a glob phase to sample the integrated pixel values of that exposure. Figure 17 shows the sequential image acquisition in Background Light Cancellation mode.

After an external request, the sensor goes through a sequential succession of EXPOSURE – GLOB – EXPOSURE – GLOB – READOUT to grab a single image. After this cycle, the sensor moves back to IDLE. The first EXPOSURE captures the background scene, and the second EXPOSURE captures the illuminated scene. When enabled, the sensor's Illumination Trigger is activated during the second exposure. The READOUT phase reads out the difference image.

The exposure time of the background scene and the illuminated scene can be programmed independently.

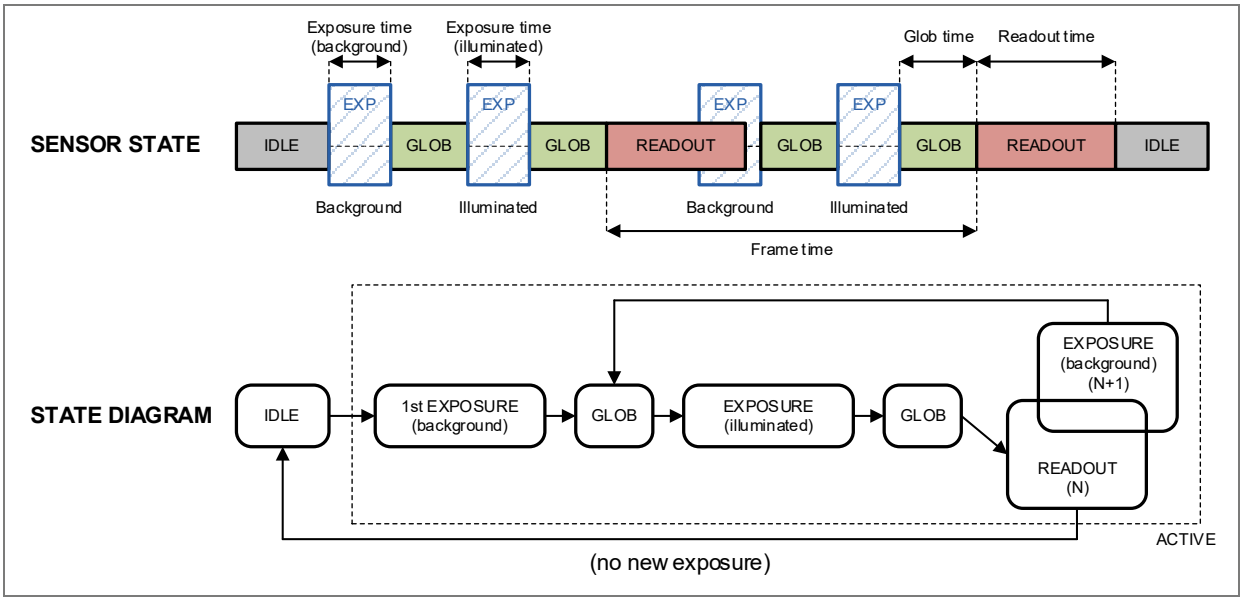
Figure 17: Sequential image acquisition with background light cancellation



Background Light Cancellation also supports pipelined image acquisition, as shown in Figure 18. While the readout of frame N is busy, the **background** exposure of frame N+1 is already started. The **background** EXPOSURE can partially overlap or fully overlap the READOUT state.

Background Light Cancellation uses a dedicated Sensor Control Mode called 'Background Light Cancellation'. Refer to section 6.8.4 for more details.

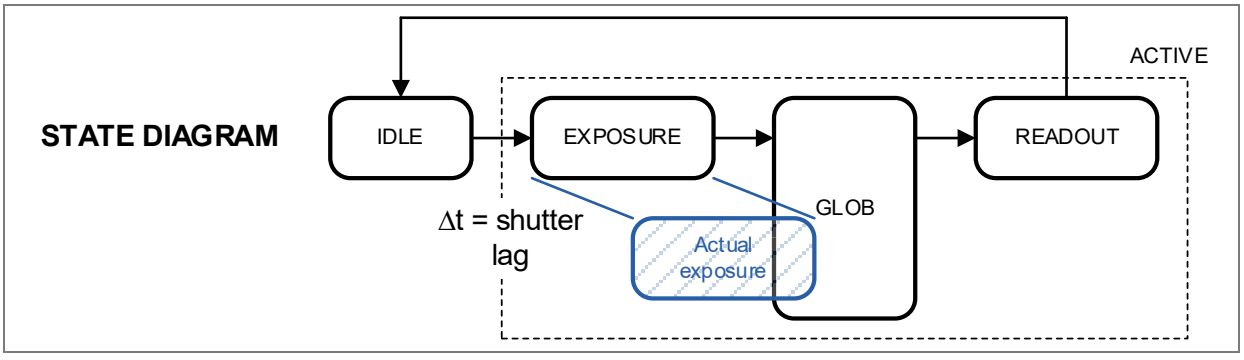
Figure 18: Pipelined image acquisition with background light cancellation



6.7.2 Shutter lag

The *shutter lag* is the time offset between the EXPOSURE state and the actual exposure on the pixel array. Figure 19 shows the state diagram for sequential image acquisition with the shutter lag annotated. Shutter lag is also present for pipelined image acquisition.

Figure 19: Sequential image acquisition with shutter lag



The actual exposure ends in the GLOB state when the integrated pixel values are sampled and the global shutter is closed. This sampling operation takes some time, which means the actual exposure does not end immediately at the start of the GLOB state, but somewhere during the GLOB state. This *time overlap* between the actual exposure and GLOB causes the *shutter lag*.

By default, the sensor also introduces the shutter lag at the start of EXPOSURE to compensate for the time overlap. This is called *shutter lag matching* and acts as a delay between the external exposure request and the actual start of exposure on the pixel array.

Information:

Throughout this document, the terms “exposure” and “exposure time” always refer to the EXPOSURE state. Whenever the “actual exposure” is meant, it is explicitly referenced to as such.

6.8 Sensor control modes

This section details all Sensor Control Modes that are available to the user. Depending on the selected mode, the image acquisition is controlled differently. Choosing a Sensor Control Mode depends on the amount of desired external control and ease of use.

Modes Full External, Triggered Internal, and Streaming are used to control the image acquisition as shown in Figure 15 and Figure 16.

The Background Light Cancellation mode is a dedicated control mode for background light cancellation. It is used to control the image acquisition as shown in Figure 17 and Figure 18.

Table 7 gives a brief overview of the available Sensor Control Modes. Each mode is detailed in one of the following sections.

Table 7: Sensor control modes

Name	External control	Internal control
Full external	• Start of exposure • End of exposure (and start of readout)	Readout details
Triggered internal	A finite sequence of 1 or more consecutive frames	• Length of exposure • Frame rate • Sequence length (number of frames) • Readout details
Background light cancellation	A finite sequence of 1 or more consecutive frames using Background Light Cancellation	• Length of background exposure • Length of illuminated exposure • Frame rate • Sequence length (number of frames) • Readout details • Background Light Cancellation operation
Streaming	An infinite sequence of consecutive frames (until a HALT command is received)	• Length of exposure • Frame rate • Readout details

6.8.1 Request commands

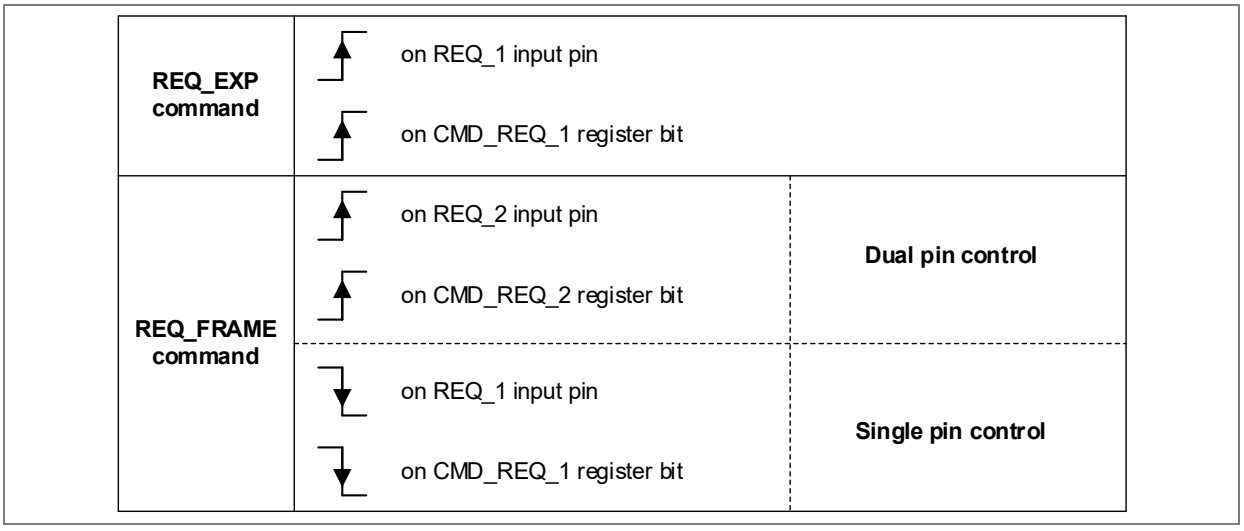
The sensor has two Request Commands to control image acquisition, named REQ_EXP and REQ_FRAME. The exact functionality of each command depends on the selected Sensor Control Mode. The Request Commands can be generated through the sensor's IO pins (this is referred to as *pin-controlled* operation) or through the CCI interface by setting certain register bits (this is referred to as *software-controlled* operation). By default, each Request Command is generated by its own sensor input pin or register bit. This is called *dual pin control*. It is also possible to generate both Request Commands from a single input pin or register bit. This is known as *single pin control*.

Figure 20 gives an overview of how the REQ_EXP and REQ_FRAME commands can be generated. The Request Commands are triggered by a rising or falling edge on the sensor input pin or register bit.

Information:

The REQ_2 sensor input pin is not available on the CSP package option. Use single pin control and/or software-controlled operation to generate the REQ_FRAME command.

Figure 20: Request command generation



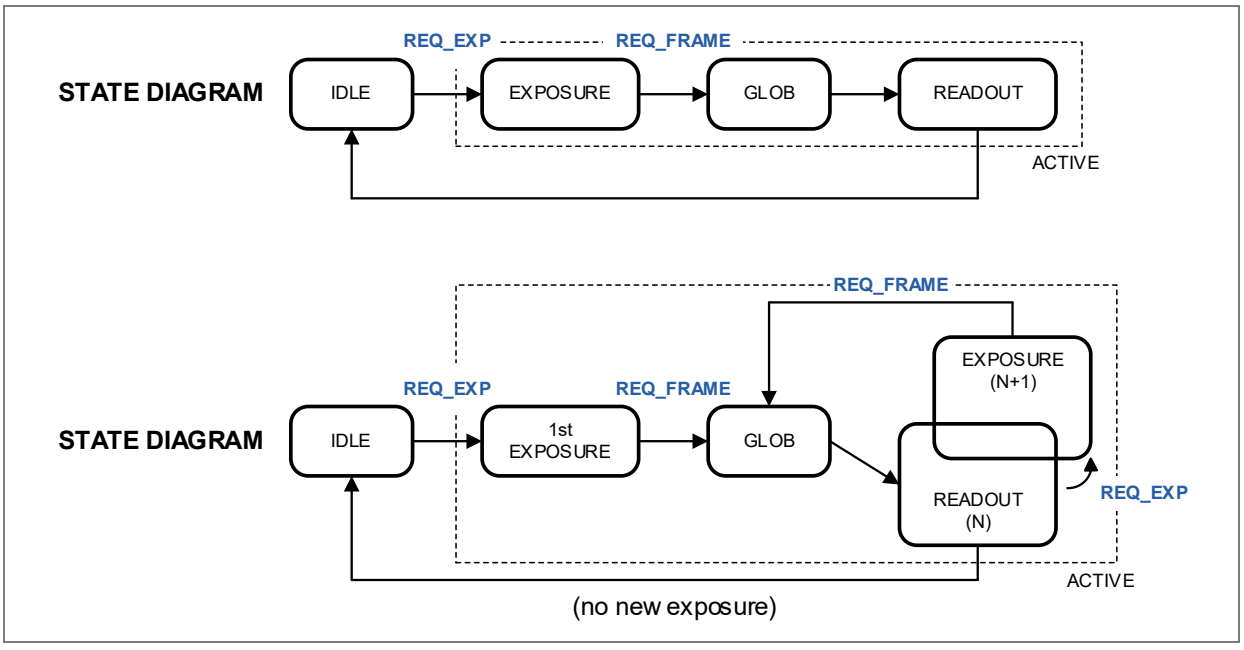
6.8.2 Full external

In the Full External control mode, all timing except the internal readout details is controlled through the REQ_EXP and REQ_FRAME commands. The REQ_EXP command moves the sensor to the EXPOSURE state. The REQ_FRAME command moves the sensor to the GLOB state, which is automatically followed by the READOUT.

The Full External mode provides maximum external control to the user. For example, the exposure can be started and ended at any time, and the exposure time can be varied from frame to frame. All request commands are processed immediately with minimal latency. However, if the user applies improper timing to the sensor, corrupted frames and interrupted frame readouts may occur.

Figure 21 shows the state diagrams for sequential and pipelined image acquisition, with the request commands annotated.

Figure 21: State diagrams in full external mode

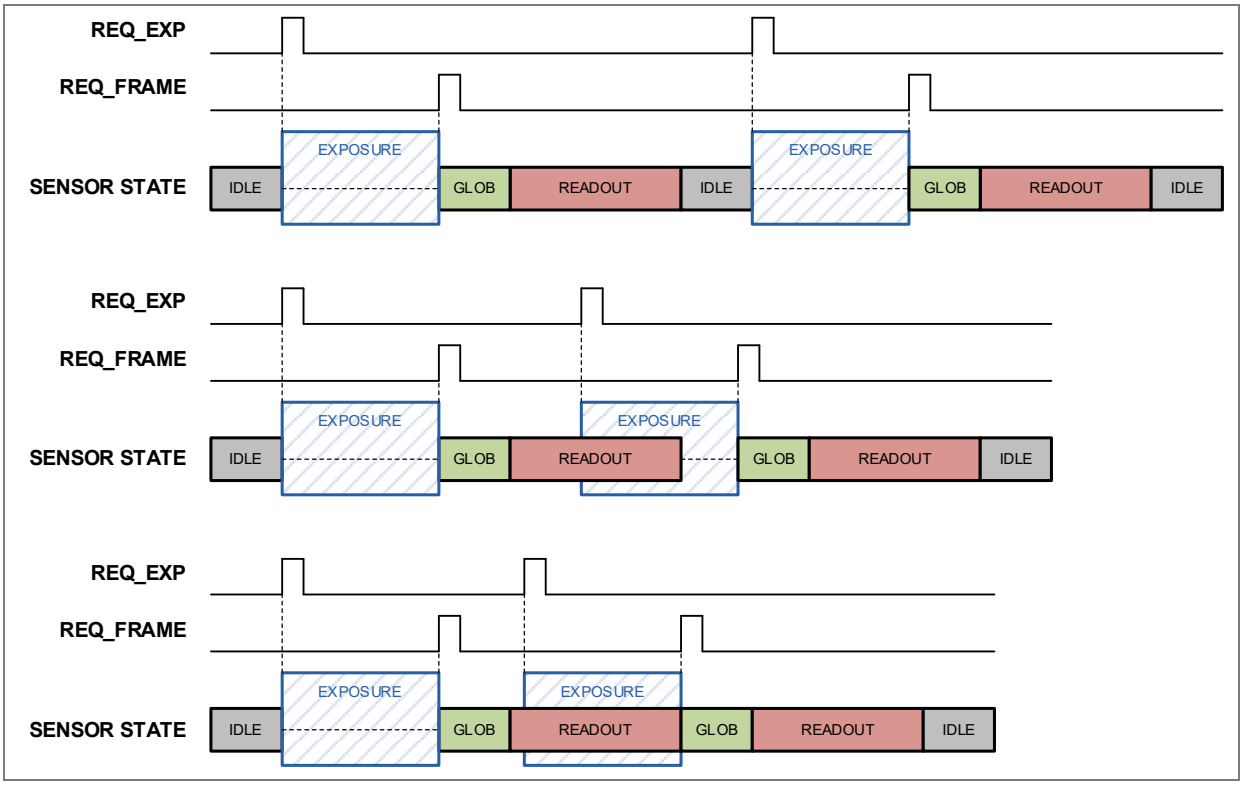


The exposure time (i.e. length of the EXPOSURE state) is equal to the time between the REQ_EXP and REQ_FRAME commands. When multiple frames are acquired, the frame time is equal to the time between two REQ_FRAME commands. Figure 22 shows a timing diagram for some common situations. The different scenarios are described below:

- Operate the sensor in sequential mode.
- Operate the sensor in pipelined mode, with the parallel exposure extending beyond the readout phase.

- Operate the sensor in pipelined mode, with the parallel exposure ending together with the readout phase. This results in maximum frame rate.

Figure 22: Timing diagrams in full external mode



The flexible control timing of the Full External mode has some invalid timings that will result in corrupted image data. These corrupted images do not contain any useful data. All invalid control timings are shown in Table 8.

Table 8: Invalid control timing in full external mode

#	Invalid control timing	Sensor response
FE_i0	REQ_EXP during GLOB	Disrupts the GLOB execution, corrupting the data of the READOUT that follows that GLOB phase.
FE_i1	REQ_FRAME during GLOB	Initiates a new GLOB followed by READOUT. The image data in this READOUT is corrupt.
FE_i2	Two consecutive REQ_FRAME without REQ_EXP in between	The second REQ_FRAME initiates a new GLOB followed by READOUT. Since there was no EXPOSURE, the image data in the second frame is corrupt.

#	Invalid control timing	Sensor response
FE_i3	REQ_FRAME when sensor is IDLE	A GLOB is started followed by READOUT. Since there was no EXPOSURE, the image data is corrupt.

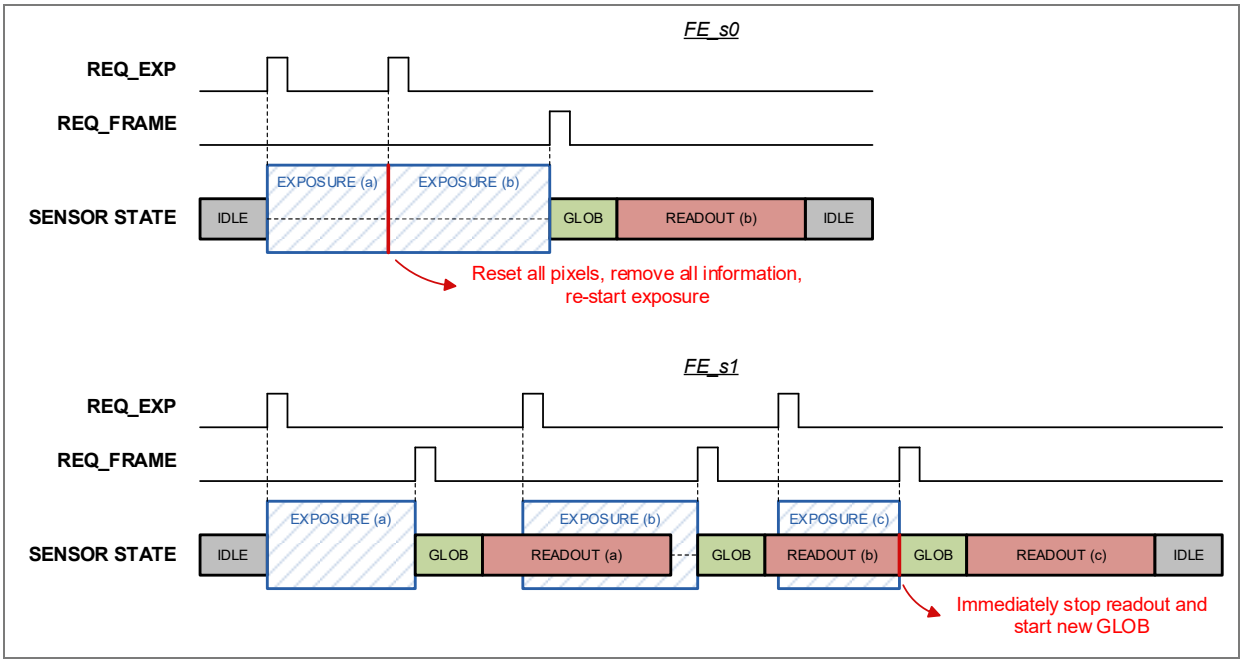
The Full External mode also has some special control timing, as shown in Table 9. These timings do not result in corrupted image data. However, data that was not yet read out is lost.

Table 9: Special control timing in full external mode

#	Invalid control timing	Sensor response
FE_s0	REQ_EXP during EXPOSURE	Initiates a new EXPOSURE, erasing all previously integrated information in the pixels. The next REQ_FRAME initiates a GLOB and READOUT that contains image data of only the second EXPOSURE.
FE_s1	REQ_FRAME during READOUT	Immediately interrupts the active READOUT to start a new GLOB (that is followed by another READOUT). The image data of the first READOUT that was not yet read is lost. The new READOUT contains valid data, if not violating FE_i2.

An example timing diagram for each of the special control timings is shown in Figure 23.

Figure 23: Special control timing diagrams in full external mode

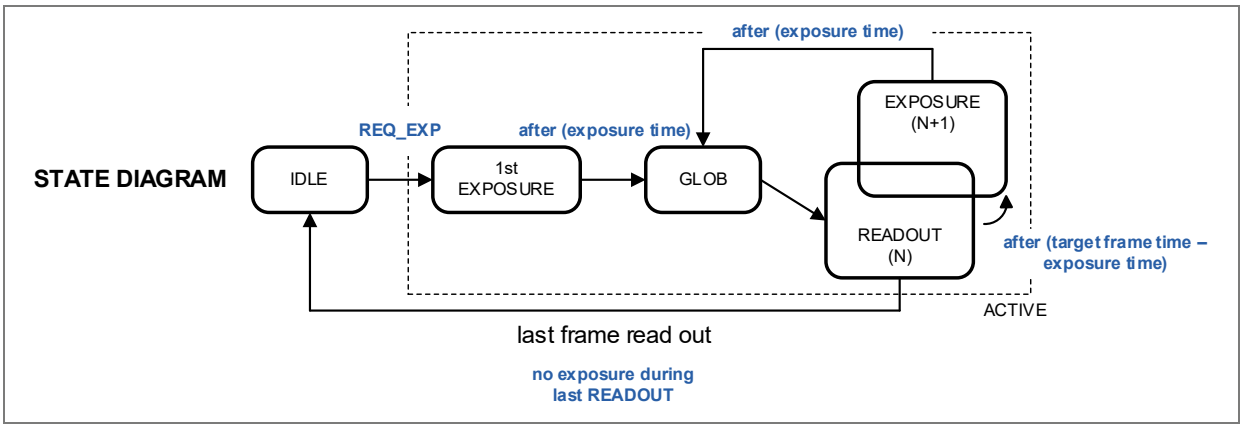


6.8.3 Triggered internal

In the Triggered Internal mode, a REQ_EXP command acquires a programmable number of frames, which are output at a programmable (target) frame rate. The exposure time of all frames is also programmed in the sensor. All REQ_FRAME commands are ignored in this control mode.

Figure 24 shows the state diagram in Triggered Internal mode with different events annotated. When the sensor is IDLE, a REQ_EXP command starts the first EXPOSURE of a sequence of frames. When the programmed exposure time elapses, the sensor automatically moves to the GLOB state, which is followed by the READOUT state. The behavior in the READOUT state depends on the number of requested frames (set by register upload) and the number of frames that have already been read during the active sequence. If the requested number of frames is not yet reached, the sensor will start a new EXPOSURE for the next frame. The start of this EXPOSURE is timed in such a way that the time between two consecutive frames is equal to the programmed (target) frame time. After the last READOUT of a requested sequence, the sensor moves back to IDLE. No new EXPOSURE is started during the last READOUT.

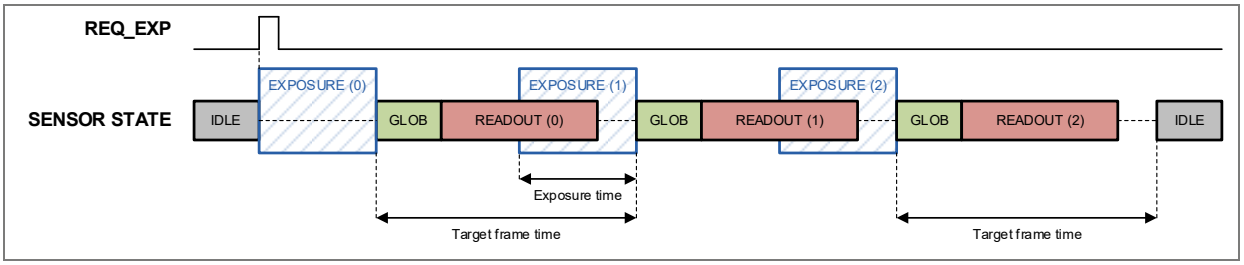
Figure 24: State diagram in triggered internal mode



An example timing diagram for the Triggered Internal mode is shown in Figure 25. The programmed number of frames in this example is three. A REQ_EXP command starts the acquisition of these three frames. The time between each frame is the target frame time and is programmed in the sensor. Note that after the last frame READOUT, the sensor only returns to IDLE when the target frame time is elapsed.

To achieve maximum frame rate, the target frame time should be equal to the glob time plus the readout time. In that case, a new GLOB is started as soon as the previous READOUT is finished.

Figure 25: Timing diagram in triggered internal mode



None of the special cases for control timing in Triggered Internal mode, as shown in Table 10, results in data loss and there is no risk of corrupted image data.

Table 10: Special control timing in triggered internal mode

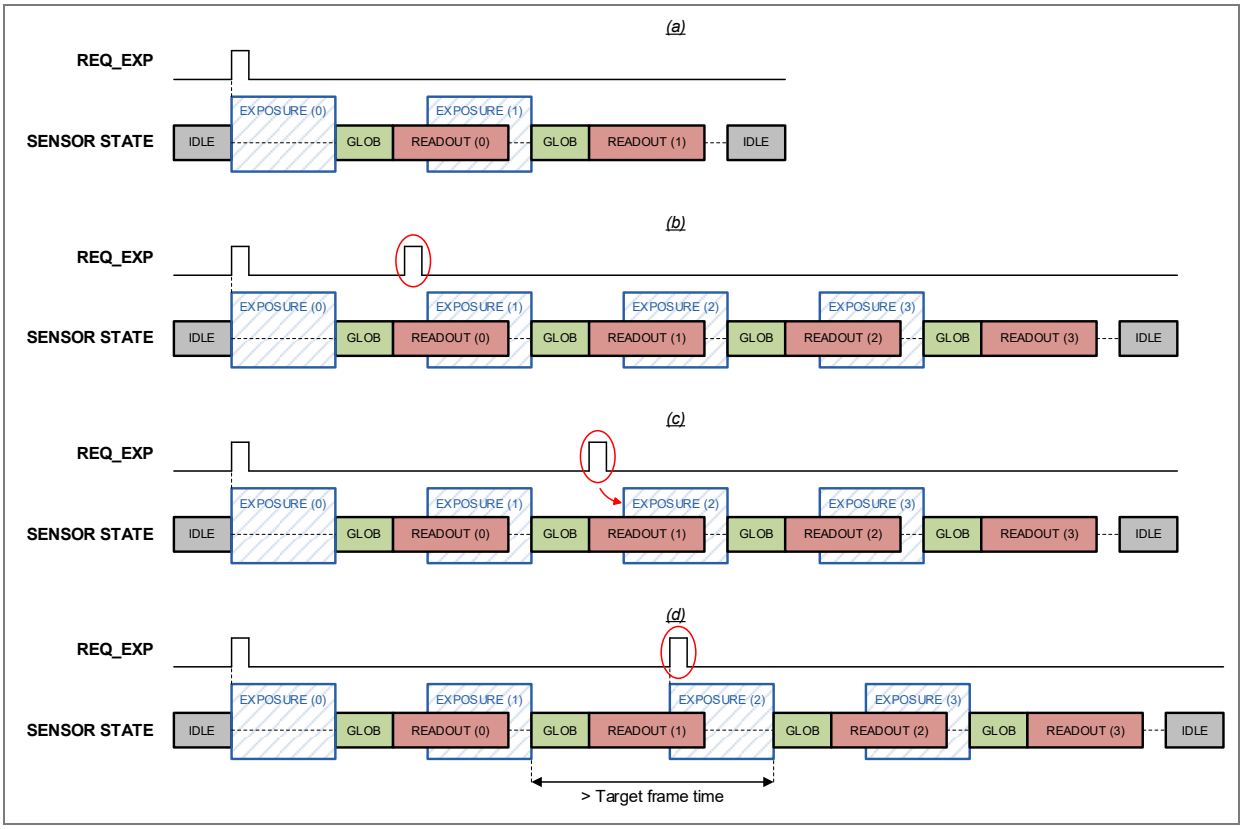
#	Invalid control timing	Sensor response
TI_s0	REQ_EXP **before** last READOUT of sequence started	Increases the active sequence length by the requested amount of frames. The maximum active sequence length is 255.
TI_s1	REQ_EXP **after** last READOUT of sequence started	Initiates a new 'first' EXPOSURE, followed by a complete new sequence. Depending on the timing of the new request, the frame rate may temporarily change.
TI_s2	REQ_FRAME command	The request is ignored.

The behavior of TI_s0 and TI_s1 is illustrated with some examples as shown in Figure 26. All examples use a sequence length of two frames. The different scenarios are:

- Normal timing: After a REQ_EXP command, two frames are acquired. The sensor returns to IDLE after the frames are acquired.
  a) TI_s0: A new request arrives **before** the last READOUT started. The sequence is extended by two frames. The sensor will output four frames in total before returning to IDLE.
  b) TI_s1: A new request arrives **after** the last READOUT started. The sequence is extended by two frames. The new EXPOSURE start is delayed to maintain the programmed target frame time.
  c) TI_s2: A new request arrives **after** the last READOUT started. The sequence is extended by two frames. The new EXPOSURE starts immediately and the frame rate is temporarily decreased to allow the exposure time to elapse.

The behavior of TI_s1 depends on when the new request arrives during the last READOUT. When the exposure time is smaller than the remaining frame time, the new exposure is delayed. This is shown in case (c). When the exposure time is larger than the remaining frame time, the new exposure starts immediately. This causes a temporary drop-in frame rate, as shown in case (d).

Figure 26: Special control timing diagrams in triggered internal mode



6.8.4 Background light cancellation

In the Background Light Cancellation mode, a REQ_EXP command acquires a programmable number of frames, which are output at a programmable (target) frame rate. All frames are acquired using on-chip Background Light Cancellation. The exposure time of the background and illuminated exposure is programmed in the sensor. Both exposure times can be set independently. All REQ_FRAME commands are ignored in this control mode.

Information:

The Background Light Cancellation mode is very similar to the normal Triggered Internal mode. The key differences are:

- Background Light Cancellation performs two exposure phases in order to do the on-chip Background Light Cancellation operation.
- With similar settings, the maximum achievable frame rate in Background Light Cancellation mode is lower. This is because of the additional exposure (and accompanying glob) phase.
- Two exposure times have to be programmed in the Background Light Cancellation mode. One for the background exposure and one for the illuminated exposure.

Figure 27 shows the state diagram in Background Light Cancellation mode with different events annotated. When the sensor is IDLE, a REQ_EXP command starts the first **background** EXPOSURE of a sequence of frames. When the programmed background exposure time elapses, the sensor automatically moves to the first GLOB state. After this, the **illuminated** EXPOSURE is started. The sensor moves to the second GLOB state after the programmed illuminated exposure time, which is then followed by the READOUT state.

The behavior in the READOUT state depends on the number of requested frames (set by register upload) and the amount of frames that have already been read during the active sequence. If the requested amount of frames is not yet reached, the sensor will start a new **background** EXPOSURE for the next frame. After the last READOUT of a requested sequence, the sensor moves back to IDLE. No new EXPOSUREs are started during the last READOUT.

Figure 27: State diagram in background light cancellation mode

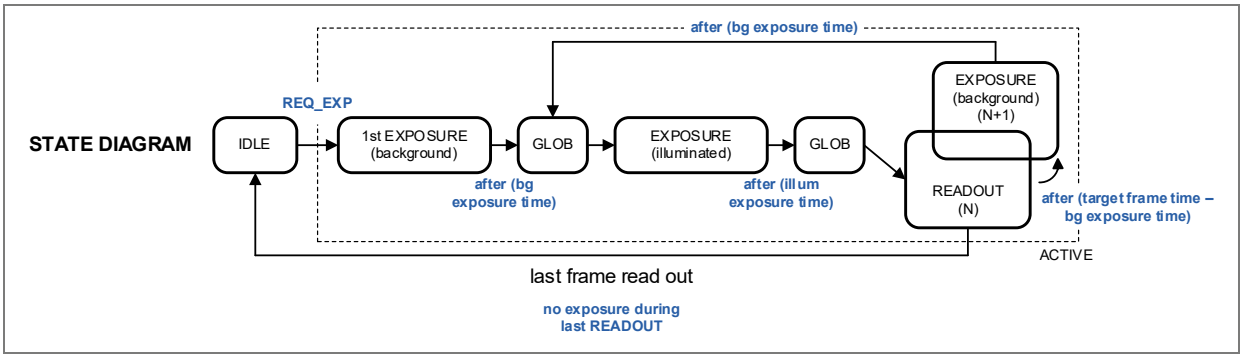
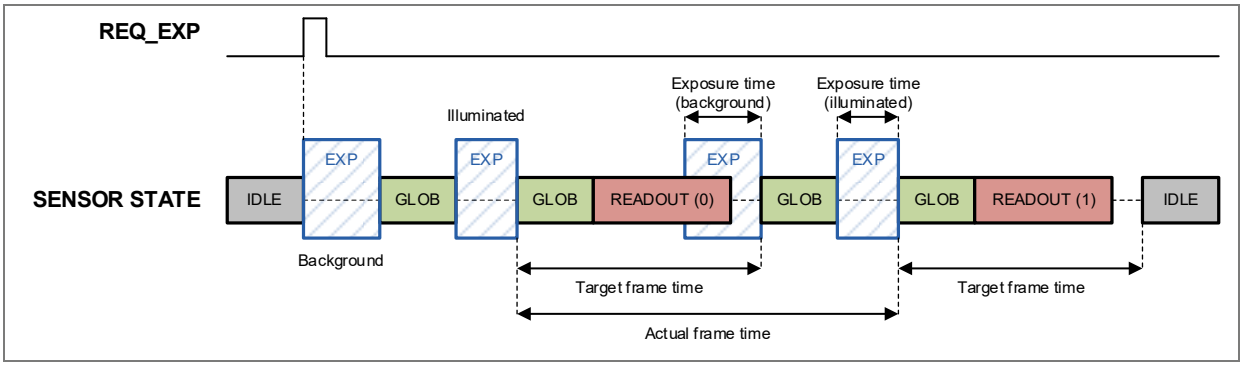


Figure 28 shows an example timing diagram for the Background Light Cancellation mode. The programmed amount of frames in this example is two. A REQ_EXP command starts the acquisition of these two frames. The actual frame time (as seen on the output interface) is greater than the programmed target frame time because of the additional EXPOSURE/GLOB phase. The actual frame time is the programmed target frame time plus the illuminated exposure time and the glob time.

Note that after the last frame READOUT, the sensor only returns to IDLE when the target frame time is elapsed.

To achieve maximum frame rate, the target frame time should be equal to the glob time plus the readout time.

Figure 28: Timing diagram in background light cancellation mode



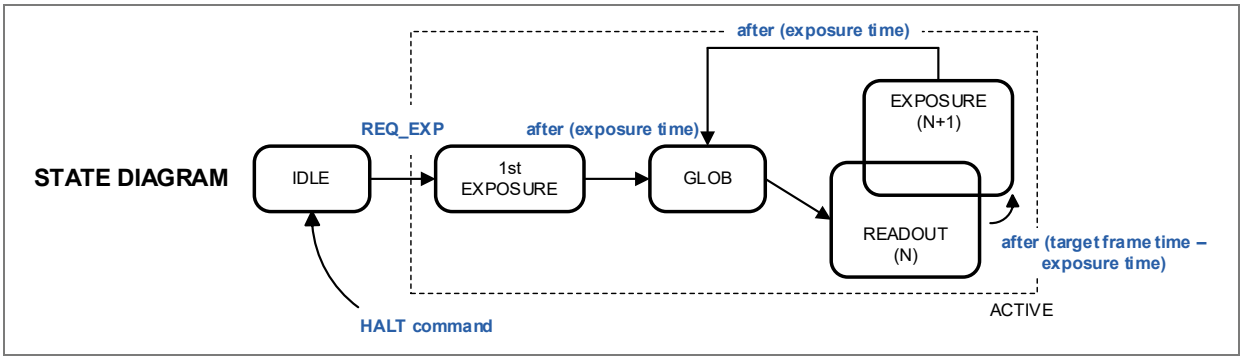
The Background Light Cancellation mode has no invalid control timing. The special control timing is identical to the normal Triggered Internal mode, as shown in Table 10.

6.8.5 Streaming

In the Streaming mode, a REQ_EXP command starts the acquisition of an infinite amount of frames. The frames are output at a programmable (target) frame rate. The exposure time is also programmed in the sensor. The Streaming mode behaves like the Triggered Internal mode with an infinite sequence length. All REQ_FRAME commands are ignored in this control mode.

Figure 29 shows the state diagram for Streaming mode with different events annotated. After the first EXPOSURE is started, the sensor cycles indefinitely between READOUT/EXPOSURE and GLOB to acquire new frames. To exit Streaming mode, the user has to upload a HALT software command to the sensor. This puts the sensor back in the IDLE state. Refer to section 6.9 for more information about software commands.

Figure 29: State diagram in streaming mode



The Streaming mode has no invalid control timing and no special control timing. After entering the Streaming mode, all REQ_EXP commands are ignored.

6.9 Software commands

Software commands are internal sensor commands that are triggered through register upload. Table 11 gives an overview of all available software commands.

The CMD_HALT_BLOCK command can be used to get the sensor out of Streaming mode without a need to reset the on-chip logic.

Table 11: Software commands

Software commands	Description
CMD_REQ_1	• A rising edge on this bit triggers a REQ_EXP command. When using *single pin control*, a falling edge on this bit triggers a REQ_FRAME command. • See section 6.8.1 for details on request commands.
CMD_REQ_2	• When using *dual pin control*, a rising edge on this bit triggers a REQ_FRAME command. • See section 6.8.1 for details on request commands.
CMD_HALT_BLOCK	• A rising edge on this bit triggers a blocking halt command. The sensor finishes the active frame readout and moves to the IDLE state afterwards.
CMD_ENTER_LP_STATE	• Manual Low Power State (LPS) entry. A rising edge on this bit starts the LPS entry sequence.
CMD_EXIT_LP_STATE	• Manual Low Power State (LPS) exit. A rising edge on this bit starts the LPS exit sequence.

7 CSP package

7.1 CSP drawings

Figure 30: Visual CSP package drawing

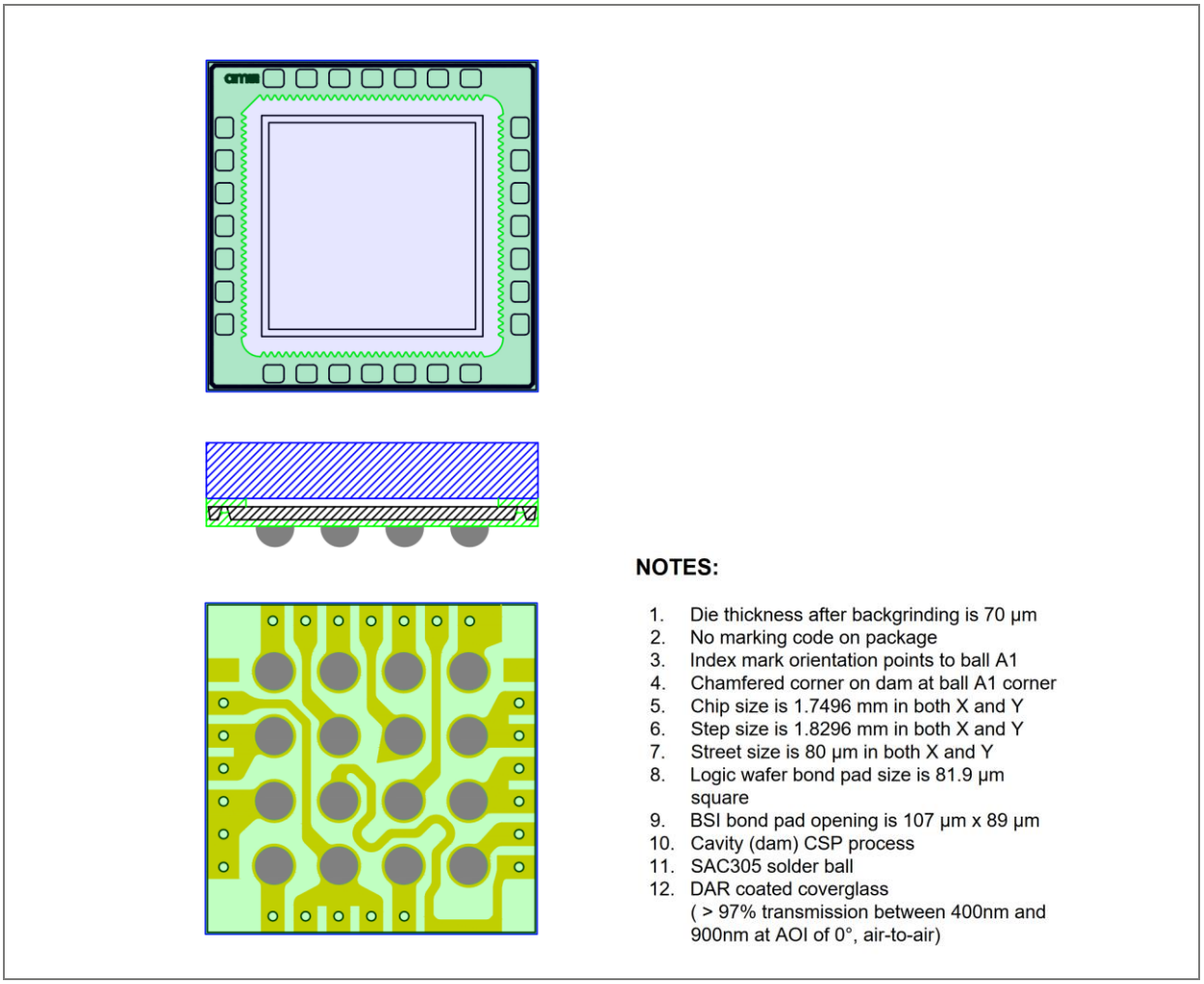


Figure 31: Mechanical CSP package drawing Mira016

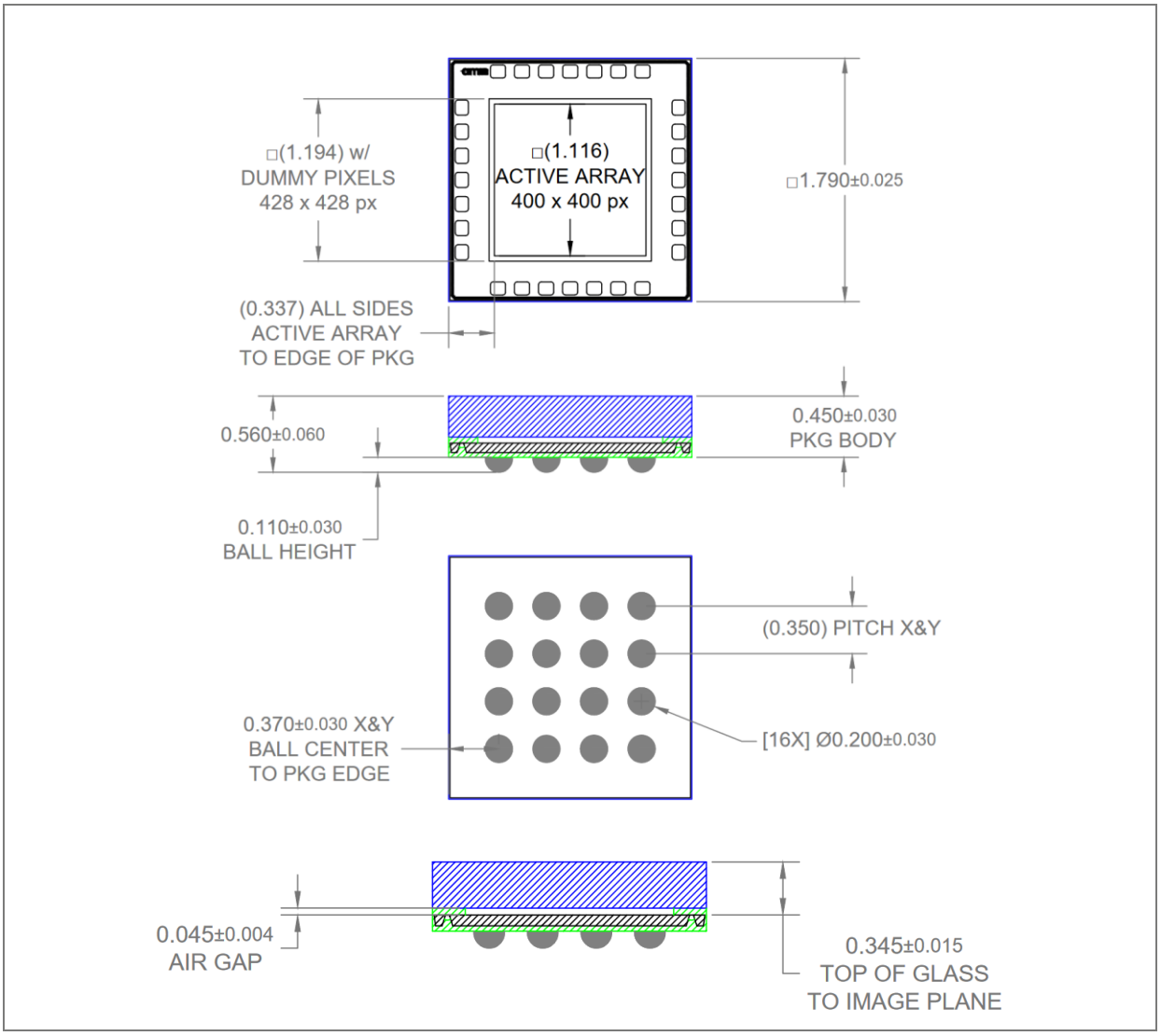
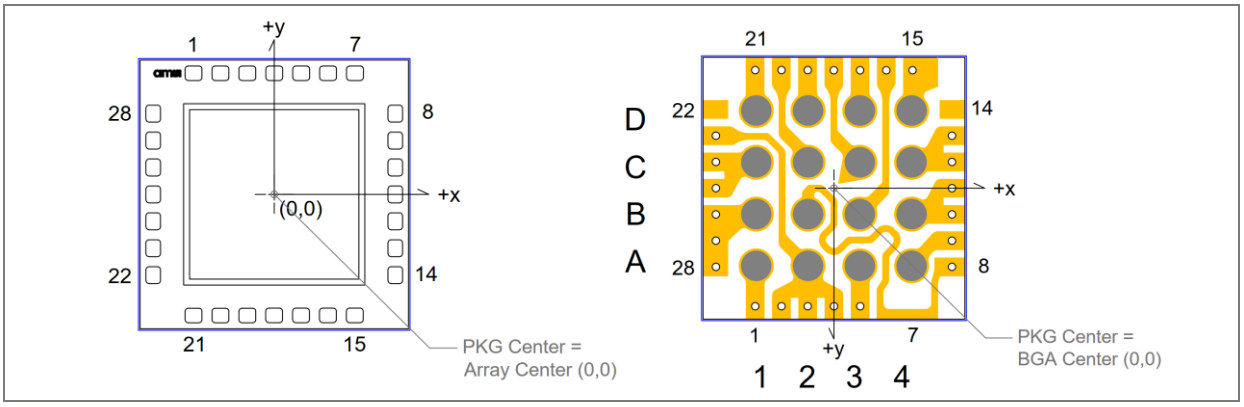


Figure 32: Pinout drawing, front- and backside, with pad names and CSP ball names



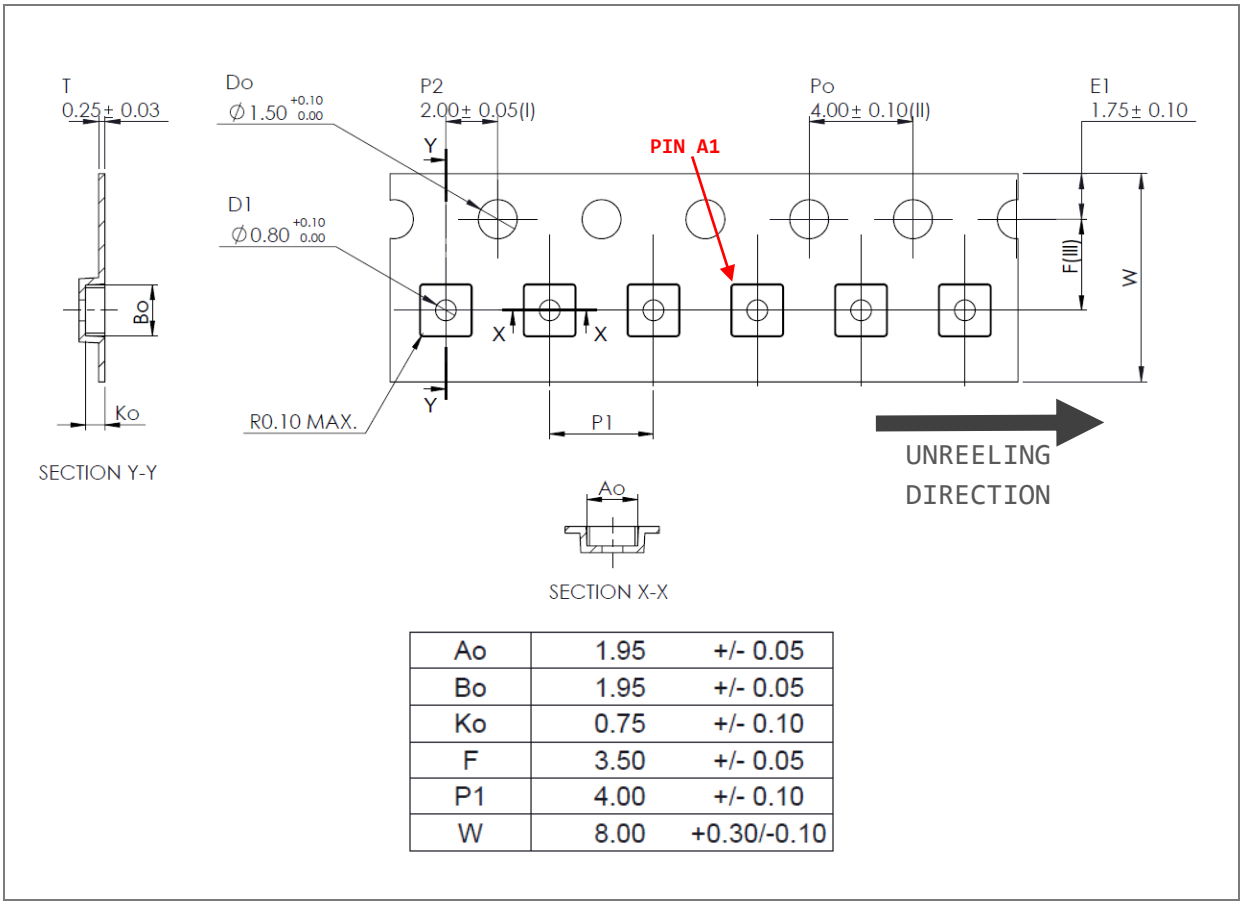
7.2 Pin description

Table 12: Pin description of Mira016 CSP package

CSP pin no.	Pin name	Type	Description
A2	VDD28	Power	Analog 2.8V supply
B4	VDD11	Power	Digital 1.1V supply
A3	VINT3	Power	Internally generated supply. Connect to external passive as suggested in “Biasing” paragraph.
C1	VINT2	Power	Internally generated supply. Connect to external passive as suggested in “Biasing” paragraph.
B2	VINT1	Power	Internally generated supply. Connect to external passive as suggested in “Biasing” paragraph.
B1	VSS28	Ground	Analog ground
C4	VSS11	Ground	Digital ground
C2	SCL	I²C	CCI clock
D1	SDA	I²C	CCI data
B3	MIPI_DP	Data	MIPI data out P
D4	MIPI_DN	Data	MIPI data out N
C3	MIPI_CLKP	Clock	MIPI clock out P
D3	MIPI_CLKN	Clock	MIPI clock out N
D2	CLK_IN	Clock	Input clock to PLL
A1	REQ_1	I/O	Request exposure (input)/CCI ID (input)/Illumination trigger (output). Connect to ground if pin functionality is not required by application.
A4	RST_N	Input	Hard reset input signal

7.3 Tape & reel information

Figure 33: Tape and reel dimensions (for CSP only)



Ao	1.95	+/- 0.05
Bo	1.95	+/- 0.05
Ko	0.75	+/- 0.10
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+0.30/-0.10

(1) 10 sprocket hole pitch cumulative tolerance ±0.2.
(2) Measured from centerline of sprocket hole to centerline of pocket.
(3) Ao AND Bo are measured on a plane at a distance "R" above the bottom of the pocket.
(4) All dimensions are in millimeters.
(5) Material: Polystyrene.

8 Lens chief ray angle (CRA)

To improve light sensitivity in the pixel towards under high incident light angles, the microlenses on top of the pixels are shifted. The shift is designed so the CRA curve is nearly linear as shown in Figure 34, and reaches 27° at maximum image height of 0.558mm (equivalent to 200 pixels).

Figure 34: CRA vs image height

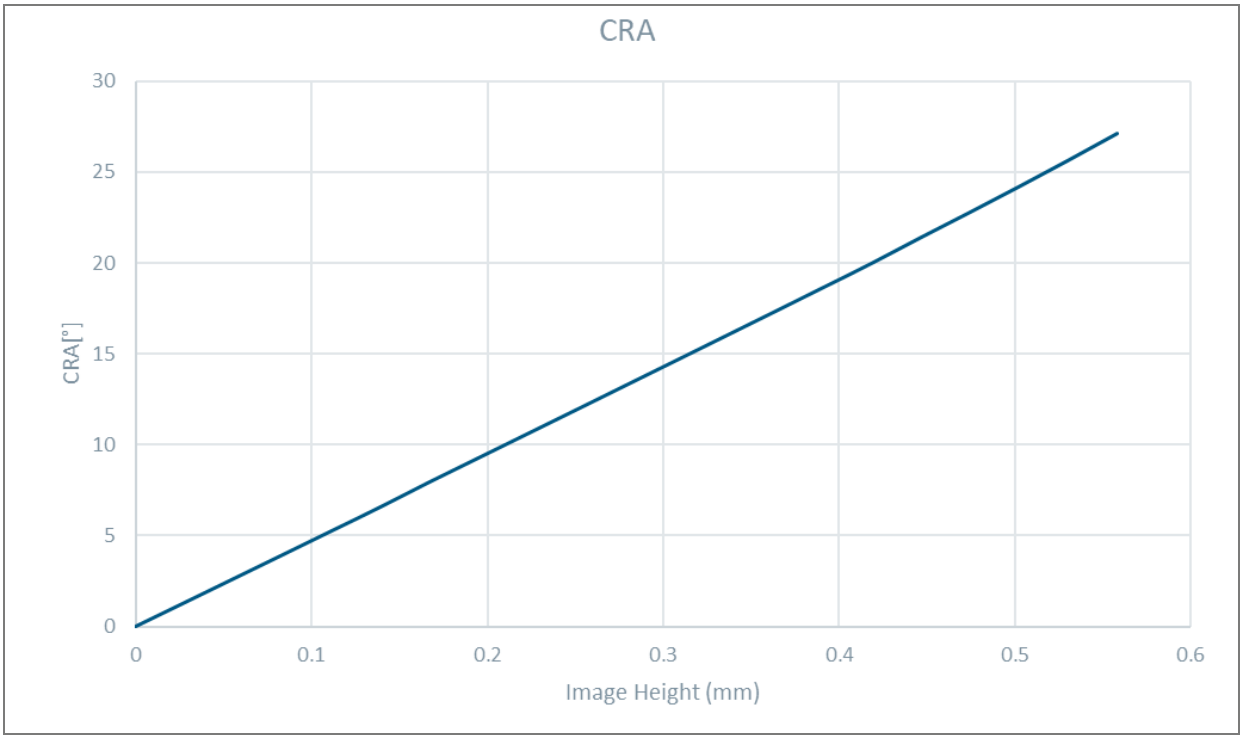


Table 13: Image height vs CRA

Image height (mm)	CRA (°)
0 (0%)	0
0.140 (25%)	6.6
0.279 (50%)	13.3
0.419 (75%)	20.0
0.558 (100%)	27.1

Information:

- The microlens shift is only applicable for the CSP package and bare die with part numbers MIRA016-▪▪M2▪▪. Please confirm the correct part number of the sensor in chapter 2.

9 Bare die and reconstructed wafer

9.1 Bare die drawing

Figure 35: Bare die drawing

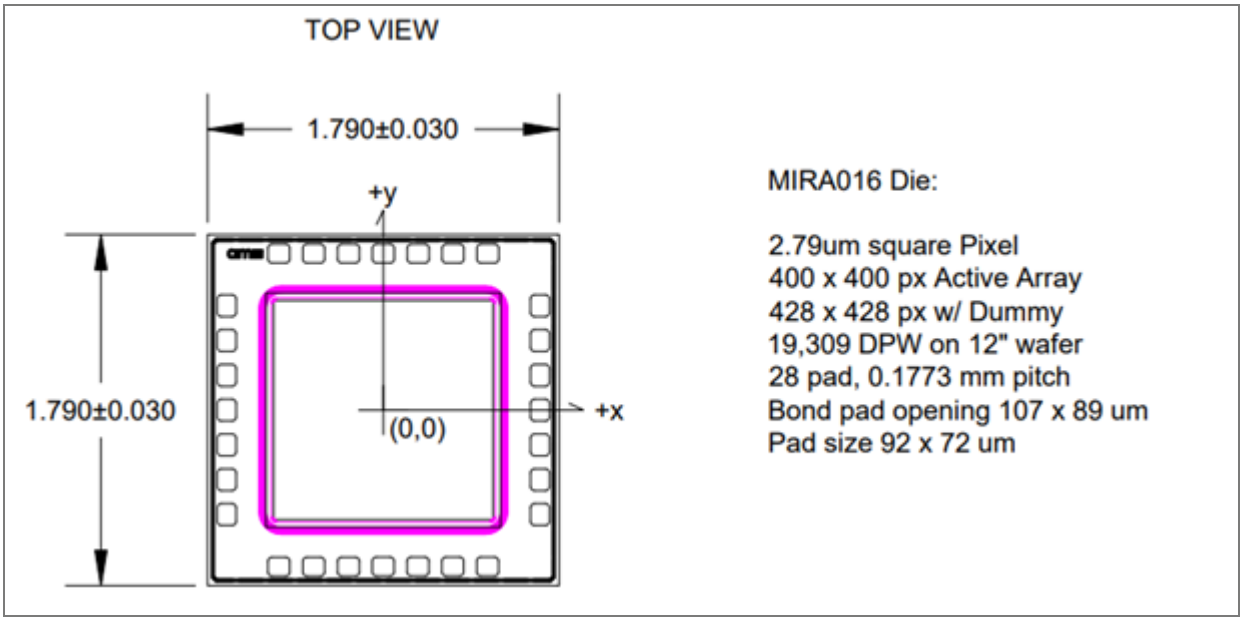


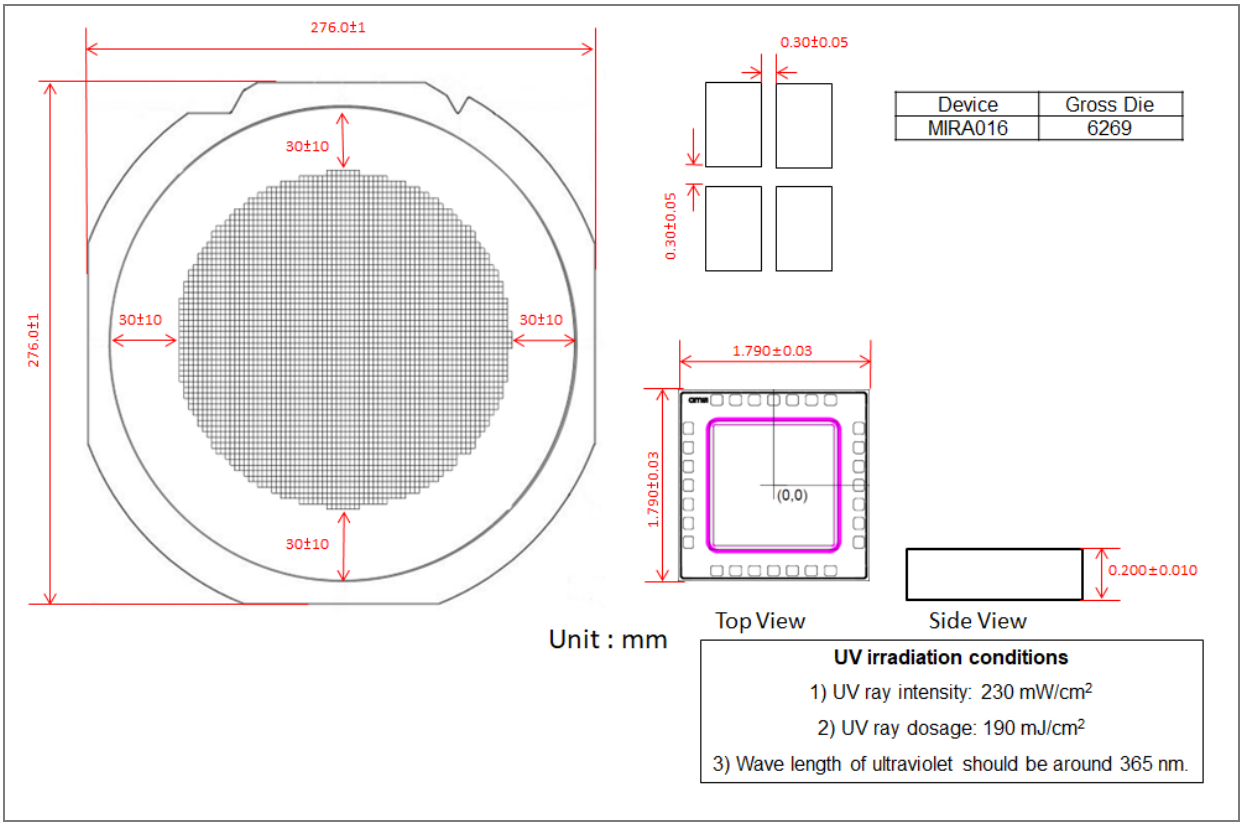
Table 14: Additional pin information

Pad #	Function	X coordinate [1]	Y coordinate [1]	Description
1	REQ_1	-0.5319	0.7973	
2	VDD28	-0.3546	0.7973	
3	VDD28	-0.1773	0.7973	
4	TEST1	0.0000	0.7973	Connect to VDD28

Pad #	Function	X coordinate (1)	Y coordinate (1)	Description
5	VINT3	0.1773	0.7973	
6	TEST4	0.3546	0.7973	NC
7	TEST5	0.5319	0.7973	NC
8	VINT1	0.7973	0.5319	
9	RST_N	0.7973	0.3546	
10	VDD11	0.7973	0.1773	
11	VDD11	0.7973	0.0000	
12	VSS11	0.7973	-0.1773	
13	VSS11	0.7973	-0.3546	
14	TEST2	0.7973	-0.5319	TDIG2, NC if not used
15	MIPI_DN	0.5319	-0.7973	
16	MIPI_DP	0.3546	-0.7973	
17	MIPI_CLKN	0.1773	-0.7973	
18	MIPI_CLKP	0.0000	-0.7973	
19	CLK_IN	-0.1773	-0.7973	
20	SCL	-0.3546	-0.7973	
21	SDA	-0.5319	-0.7973	
22	TEST3	-0.7973	-0.5319	TDIG1, NC if not used
23	VDD28	-0.7973	-0.3546	
24	VINT2	-0.7973	-0.1773	
25	VINT2	-0.7973	0.0000	
26	VSS28	-0.7973	0.1773	
27	VSS28	-0.7973	0.3546	
28	VSS28	-0.7973	0.5319	

(1) Bond pad coordinates in mm. Measured from center of package.
(2) Description of pin connection is provided in Pin description paragraph.
(3) Only additional pin information is provided in this table.

Figure 36: Reconstructed wafer



10 Appendix

10.1 Glossary

Table 15: Glossary

Abbreviation	Definition
ACK	Acknowledge
ADC	Analog to Digital Convertor
AR	Augmented Reality
BSI	Back-Side Illumination
BSP	Black Sun Protection
CCI	Camera Control Interface
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide Semiconductor
CRA	Chief Ray Angle
CSI	Camera Serial Interface
CSP	Chip Scale Package
DC	Dark Current
DDR	Double Data Rate
DP/DN	Data Positive/Data Negative
D-PHY	MIPI Physical Layer Protocol
DR	Dynamic Range
DTN	Dark Temporal Noise
ESD CDM	Electrostatic Discharge Charge Device Model
ESD HBM	Electrostatic Discharge Human Body Model
FPS	Frames per Second
FWC	Full Well Capacity
GLOB	Closing global shutter state by sampling all integrated pixel values
IO	Input-Output
LP	Low Power
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSL	Moisture Sensitivity Level
NACK	Not Acknowledge
NIR	Near Infrared
OTP	One Time Programmable
PLL	Phase-Locked Loop

Abbreviation	Definition
QE	Quantum Efficiency
RH	Relative Humidity
ROI	Region of Interest
RW	Reconstructed Wafer
SCL	Serial Clock
SDA	Serial Data
ULPS	Ultra-Low Power State

11 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous released version to current revision v2-00	Page
Updated document security class to “PUBLIC” from “CONFIDENTIAL”	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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