AS1163 – Details on design, handling and assembly

Application Note

Published by ams-OSRAM AG
Tobelbader Strasse 30,
8141 Premstaetten Austria
Phone +43 3136 500-0
ams-osram.com

AS1163 – Details on design, handling and assembly

Application Note No. AN001078

Valid for:
AS1163

Abstract

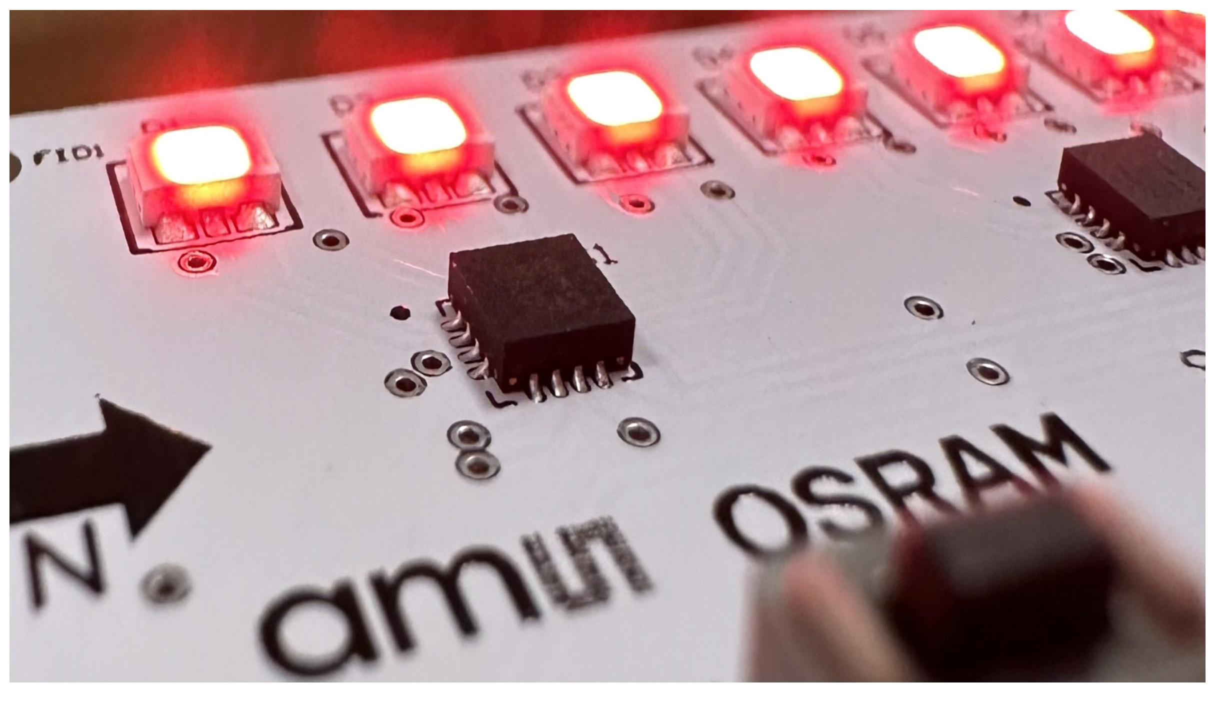
The AS1163 (SAID) is a robust mixed-signal silicon device designed for dynamic lighting applications, notably in automotive environments. The device operates using the Open System Protocol (OSP), enabling seamless integration into various systems. This application note provides essential design guidelines and technical product documentation to assist customers in implementing AS1163 (SAID) into their applications.

Table of contents

1 Basic information

The **AS1163,** also referred here as **SAID,** is primarily designed for automotive interior applications that require high dynamic RGB lighting scenarios. The AS1163 (SAID) from ams OSRAM integrates drivers for three RGB LED channels. An external microcontroller can address and control each AS1163 (SAID) device in a daisy chain architecture via the **Open System Protocol (OSP)**. This open protocol allows the microcontroller to read back data and to run any color mixing algorithm. It also permits reading back temperature values to optimize the color setting algorithm.

Figure 1: AS1163 QFN16 soldered on board



1.1 Design and technical advantages

The **AS1163** (SAID) is a compact LED driver designed for automotive and dynamic lighting applications. By integrating 9 PWM drivers into a single component, it significantly reduces the space requirements compared to traditional light sources, which typically use separate external drivers. This allows for efficient single-layer PCB designs.

The AS1163 (SAID) supports dynamic control of color and brightness with an independent PWM dimming range of up to **16 bits**. Furthermore, users can create a controllable chain of multi-color LEDs, enabling additional functions such as providing situational information to drivers.

Figure 2: AS1163 pin diagram

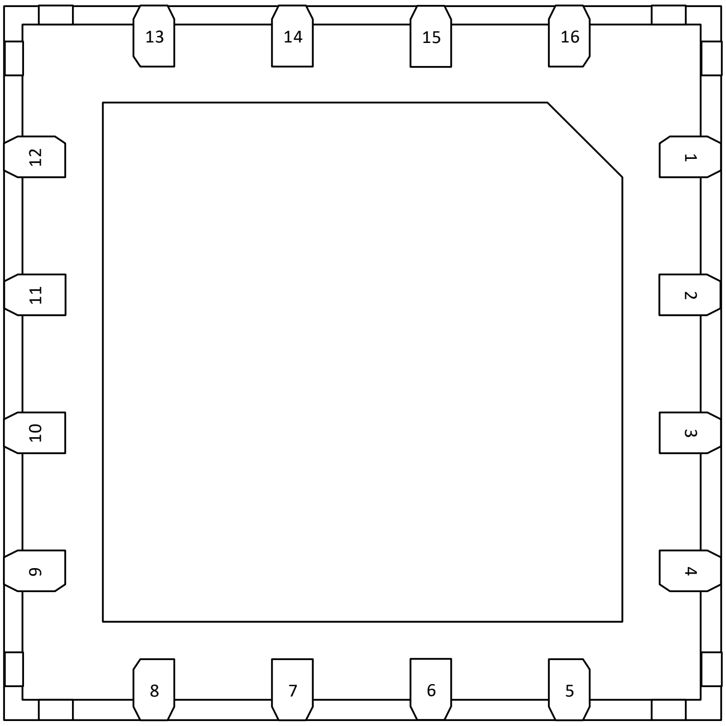


Table 1: Pin description

Pin number	Pin name	Pin type(1)	Description(2)
QFN 3x3 16			
1	G0	ANA	Driver 1 of channel 0 (Green)
2	R0	ANA	Driver 0 of channel 0 (Red)
3	GNDP	PWR	Power ground
4	VDD	PWR	5 V power supply
5	SIO1P	ANA/DIO	Positive digital IO for SIO1 interface
6	SIO1N	ANA/DIO	Negative digital IO for SIO1 interface
7	GNDA	PWR	Analog ground
8	SIO2N	ANA/DIO	Negative digital IO for SIO2 interface, test-bus
9	SIO2P	ANA/DIO	Positive digital IO for SIO2 interface, test-bus
10	B2	ANA	Driver 2 of channel 2 (Blue), also INT
11	G2	ANA	Driver 1 of channel 2 (Green), also SCL
12	R2	ANA	Driver 0 of channel 2 (Red), also SDA
13	B1	ANA	Driver 2 of channel 1 (Blue), also SYNC
14	G1	ANA	Driver 1 of channel 1 (Green), also for parallel address configuration

Pin number	Pin name	Pin type(1)	Description(2)
QFN 3x3 16			
15	R1	ANA	Driver 0 of channel 1 (Red), also for parallel address configuration
16	B0	ANA	Driver 2 of channel 0 (Blue)

(1) Explanation of abbreviations:

DIO	Digital input and output
ANA	Analog pin
PWR	Power pin

(2) Pin name: R, G and B are only for naming purposes, not necessarily to be bound to red, green or blue color.

2 PCB design recommendations

A well-designed PCB layout is crucial for optimal performance of the AS1163 (SAID) device. To ensure electromagnetic compatibility (EMC) and signal integrity, consider the following guidelines specific to AS1163 (SAID):

- **General layout principles:**
  - Maintain short traces for high-speed signals to minimize inductance and capacitance.
  - Ensure all traces in high-speed differential interfaces (like SIO) are of equal length to prevent signal reflections.
  - Avoid vias and trace crossings whenever possible to reduce signal integrity issues.
- **Power and ground considerations:**
  - Given the potential current draw of up to 288 mA from the LEDs, the supply and ground traces must be appropriately sized to avoid voltage drops.
  - Use decoupling capacitors close to the VDD pins of the AS1163 (SAID). Recommended values include:
  - **1 µF** low ESR ceramic capacitor for general decoupling.
  - **100 nF** capacitor placed as close as possible to the VDD pin.
- **Single-ended signal line guidelines:**
  - Keep the lines as short as possible.
  - Minimize the loop area between the line and ground to reduce interference.
  - Do not cross signal lines and avoid vias between them.
  - Off-board designs should be avoided unless absolutely necessary.
- **LVDS signal line guidelines (specific to communication with other OSP devices):**
  - Keep LVDS pairs (SIOxP and SIOxN) close together and parallel to each other to minimize electromagnetic interference.
  - Ensure that the lengths of SIOxP and SIOxN are balanced to maintain differential signaling integrity.
  - Minimize stubs and junction taps to avoid reflections.
  - Avoid right-angle traces to reduce radiated emissions.

2.1 Recommendations for external components

When integrating external components with the AS1163 (SAID), consider the following:

- Connect a minimum of 1 µF low ESR ceramic capacitor as close as possible to the 5V IC supply (PIN4).
- Place a 100 nF capacitor as close as possible to the 5V IC supply (PIN4).
- Use pull-up resistors as needed for selecting the MCU and transceiver communication mode (consult the AS1163 (SAID) documentation for specific resistor values).
- Ensure that the maximum supply voltage rating of 5.5 V is not exceeded.

2.2 Thermal PCB guidelines

In addition to their primary function as a mechanical substrate and electrical contacting element, circuit boards have the task to efficiently dissipate the heat which is generated. Design PCB layouts to facilitate heat spread from the junctions of the LEDs. This can be achieved through thermal vias in pads and copper pours.

Use the integrated temperature sensor for real-time monitoring and adjustments to PWM settings to mitigate thermal stress and choose PCB materials that offer good thermal conductivity.

2.2.1 Typical thermal characteristics

Thermal characteristics obtained on a FR-4 PCB with the following specifications:

Table 2: Layer stack layout used for thermal testing

PCB information	JEDEC 2s2p PCB
PCB dimensions	76.2x114.3x1.6mm^3
Top signal layer thickness	0.070mm
GND plane layer thickness	0.035mm
Power plane layer thickness	0.035mm
Bottom signal layer thickness	0.070mm
Solder mask thickness	0.020mm
Thermal via diameter	0.3mm
Thermal via pitch	1.2mm
Thermal via count	1

PCB information	JEDEC 2s2p PCB
Core thickness	0.6mm

By using a board with the previous characteristics, a Φ_{JA} of 64°C/W (Junction to Ambient thermal resistance) in still air at 125°C is expected.

3 Handling recommendations

Handling the AS1163 should be done with care to prevent stresses that could affect their functionality and lifespan. Here are some key points to consider:

1. **Mechanical stresses:** AS1163 (SAID) devices can be sensitive to mechanical stresses during processing and operation. Excessive stress may lead to device failure, so handling should be done with care.
2. **Avoid sharp objects:** The use of sharp tools or objects should be avoided to prevent any damage to the components. Direct contact with sensitive structures beneath the encapsulation should be minimized.
3. **General precautions:** Follow standard ESD (Electrostatic Discharge) handling precautions. The AS1163 (SAID) device is rated for ESD protection up to 4 kV, but additional protection measures should be implemented at the system level to ensure overall device safety. The devices are classified as "Class 2 HBM," making them suitable for standard SMT (Surface Mount Technology) assembly processes, provided that common ESD safety precautions are followed.

3.1 Cleaning procedures

- **Direct cleaning:** Avoid any direct mechanical or chemical cleaning of the AS1163 (SAID) device to prevent damage. If cleaning is necessary, the use of Isopropyl Alcohol (IPA) is recommended.
- **Compressed air:** For dust removal, purified compressed air can be used. Ensure that the maximum pressure does not exceed 4 bar at a distance of 20 cm from the component to prevent any potential damage. Also, the compressed air should prevent electrical charging to avoid ESD damages
- **Material testing:** Always test cleaning materials and methods on sample components before applying them to the actual devices.

3.2 Storage and handling practices

AS1163 (SAID) devices should be stored in vacuum-sealed dry bags with desiccants. The recommended relative humidity during storage is ≤ 10% RH.

The device has a moisture sensitivity level (MSL) of 2 according to JEDEC J-STD-020E.

Usually, devices should remain in their original packaging until ready for assembly to minimize exposure to moisture and contamination.

3.3 Handling guidelines

- All devices should be allowed to return to room temperature after soldering before proceeding to the next handling step.
- Avoid stacking assembled LED boards to prevent compression and potential damage.
- Ensure that mechanical stress, such as shear forces, is minimized during handling. This is particularly important due to the sensitive nature of the encapsulation.
- Automated placement of the AS1163 (SAID) devices is strongly recommended to reduce the risk of damage during manual handling.
- If manual handling is unavoidable, use ESD-safe tweezers to grasp the package frame only, applying even pressure to avoid stress to the encapsulation or sensitive internal components.

3.4 Compliance and environmental considerations

The AS1163 (SAID) device complies with current RoHS guidelines and does not contain hazardous substances as outlined by European Union and China regulations.

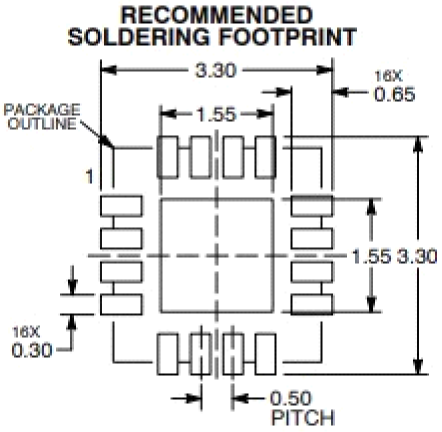
4 Processing

4.1 Solder pad design

The solder pad effectively creates the direct contact between the AS1163 (SAID) and the circuit board, the design of the solder pad contributes decisively to the performance of the solder connection. The design has an influence on solder joint reliability and heat dissipation, particularly due to the thermal characteristics of the QFN16 package.

In most cases, it is therefore advantageous to use the recommended solder pad since it is individually adapted to the properties and conditions of the AS1163 (SAID). The corresponding solder pad can also be found in the datasheet of the device. Based on the given solder pad design, an optimized balance between good processability, the smallest possible positioning tolerance, and a reliable solder connection can be achieved. During PCB manufacturing, a typical registration tolerance of ±50µm between the copper trace pattern and solder mask needs to be respected. To achieve an optimal solder joint contact area and to limit the impact of the expansion effect of the solder mask, it is recommended to use a NSMD pad (Non Solder Mask Defined) for all electrical signal pads. Nevertheless, it is recommended to check and re-measure the solder pad dimensions.

Figure 3: Recommended footprint



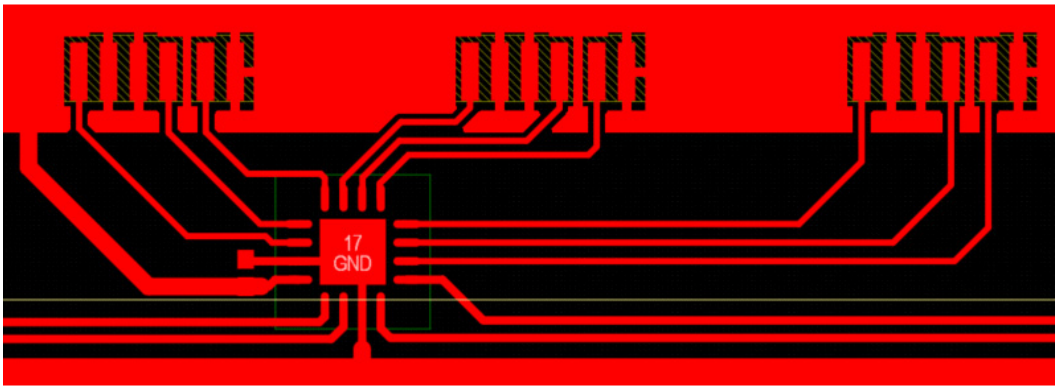
4.2 Solder stencil

In the SMT process, solder paste is normally applied by stencil printing. The design of the printing stencil and an accurate working process influence the applied amount and quality of the paste deposit.

A proper solder paste printing increases the solder quality. Effects such as solder bridges, solder spray, and/or other soldering defects are largely determined by the design of the stencil apertures and the quality of the stencil printing (e.g., positioning, cleanliness of the stencil, etc.). For the AS1163 (SAID), a stencil thickness of 120 µm is recommended. Further optimization to improve the amount of solder paste volume should take place. A uniform solder joint thickness is recommended in order to produce reliable solder joints and obtain an appropriate optical alignment. An automatic stencil printing with proper fiducial and electro-polished or fine grain material stencil results in proper printing deposits.

Use standard lead-free SAC 305 (Sn 96.5% / Ag 3% / Cu 0.5%) no-clean solder paste for the paste printing process.

Figure 4: Real PCB layout



4.3 Pick and place nozzle design

When processing by means of automated placement machines, care should be taken to use an appropriate pick-and-place tool and to ensure that the process parameters conform to the package's characteristics, specifically the QFN16 package used for the AS1163 (SAID). Care should generally be taken that an appropriate pick-and-place tool is used and that process parameters conform to package characteristics. The placement force applied to the top of the package should be kept to a minimum.

4.4 Reflow soldering

Since the SAID (AS1163) is compatible with existing industrial SMT processing methods, state-of-the-art populating techniques can be used for the mounting process. The individual soldering conditions for each AS1163 (SAID) type according to JEDEC can be found in the respective data sheet. A standard reflow soldering process with forced convection under a standard N_2 atmosphere is recommended for mounting the component, in which a typical lead-free SnAgCu metal alloy is used as solder. For superior solder joint connectivity results, it is recommended to use a nitrogen atmosphere <500ppm O_2.

In this context, it is recommended to check the profile on all new PCB materials and designs. As a good starting point, the recommended temperature profile provided by the solder paste manufacturer can be used. The maximum temperature and ramp-up and cool-down gradient for the profile, as specified in the datasheet, should, however, not be exceeded. Please check and verify the reflow profile for every new design.

Ensure you not to apply any stress during soldering or while the AS1163 (SAID) is cooling down to ambient temperature.

Figure 5: Soldering profile

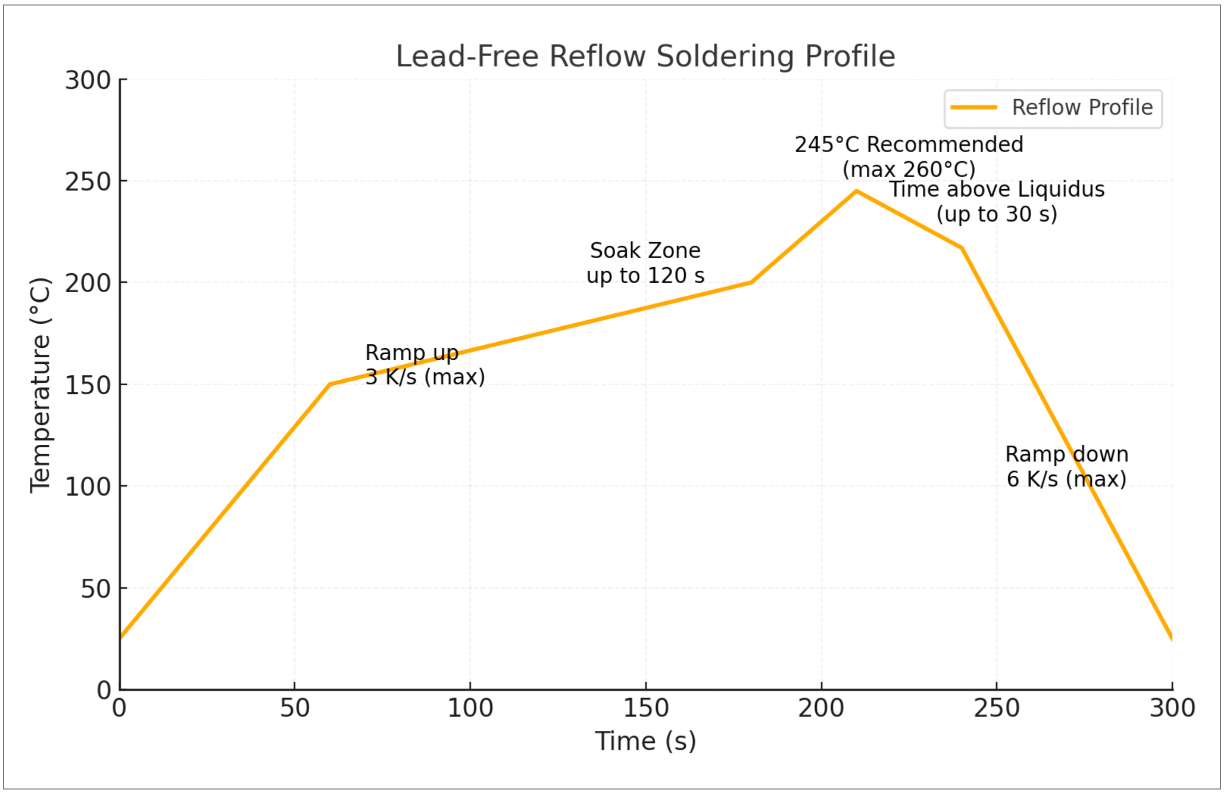


Table 3: Soldering profile

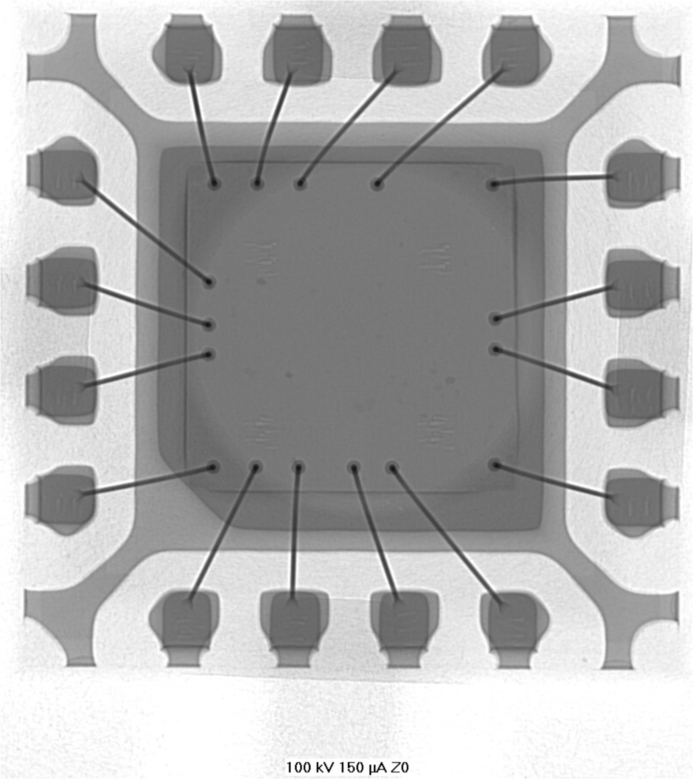
Profile feature	Symbol	Min	Recommended	Max	Unit
Ramp-up rate to preheat		2	3	3	K/s
Time to preheat (25°C to 150°C)	tst_sts	60	100	120	s
Ramp-up rate to peak		2	3	3	K/s
Liquidus temperature	TLT_LTL	217	217	217	°C
Time above liquidus	tLt_LtL	30	60	90	s
Peak temperature	TPT_PTP	245	250	260	°C
Time within 5°C of peak temperature	tpt_ptp	10	20	30	s
Ramp-down rate		3	4	6	K/s
Total time (25°C to peak)		-	300	300	s

4.5 Solder joint inspection

A visual inspection in combination with X-ray inspection ensures proper solder joint quality and helps to identify common solder joint issues or defects such as solder balls, solder bridges, high void level, or placement position. In addition, a proper inspection ensures to determine correct design (PCB solder pad and stencil) or assembly process settings (printing parameter, pick-and-place position and settings). As a common industry standard, it is recommended to inspect the solder joint quality for every new product or design and therefore indicate design or manufacturing issues at an early stage. The AS1163 (SAID) package design is featured with integrated wettable side flanks or so-called solder control structures which enable excellent self-alignment during reflow soldering. The solder wetting structure enhances the solder wetting to form a solder fillet and minimize the risk of rotation and tilting of the component. Uniform solder fillets are therefore beneficial to enable visual inspection and usage of automatic optical inspection systems (AOI). As an established practice during in-house tests, X-ray inspection should be performed twice, before the reflow process and after. Before soldering, an X-ray image gives an optimal indication of proper component placement. For example, if solder paste squeeze out can be seen, it is an indication for high placement force. Since the distances between the solder pads are relatively small, it is possible to see in early stages whether solder balls or solder bridges are formed.

X-ray inspection after reflow soldering is typically used to check void levels but also confirms that there are no solder balls or solder bridges under the components.

Figure 6: X-Ray image



5 Summary

The AS1163, also referred to as SAID (Stand-alone Intelligent Driver), is a compact mixed-signal silicon device primarily designed for high dynamic RGB lighting applications, especially in automotive environments. It integrates nine PWM drivers organized in three RGB channels, allowing for efficient single-layer PCB designs. The device operates using the Open System Protocol (OSP), which supports seamless communication and control of up to 1000 nodes in a daisy chain configuration. Integrates multiple drivers, minimizing space requirements compared to traditional systems. Supports independent PWM dimming with a range of up to 16 bits, enabling intricate color mixing and brightness adjustments. Capable of providing situational information through controllable multi-color LEDs.

6 Revision information

Changes to current revision v1-00	Page
Initial production version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

ABOUT ams OSRAM Group (SIX: AMS)

The ams OSRAM Group (SIX: AMS) is a global leader in intelligent sensors and emitters. By adding intelligence to light and passion to innovation, we enrich people's lives. With over 110 years of combined history, our core is defined by imagination, deep engineering expertise and the ability to provide global industrial capacity in sensor and light technologies. Our around 20,000 employees worldwide focus on innovation across sensing, illumination and visualization to make journeys safer, medical diagnosis more accurate and daily moments in communication a richer experience. Headquartered in Premstaetten/Graz (Austria) with a co-headquarters in Munich (Germany), the group achieved EUR 3.6 billion revenues in 2023. Find out more about us on https://ams-osram.com

DISCLAIMER

PLEASE CAREFULLY READ THE BELOW TERMS AND CONDITIONS BEFORE USING THE INFORMATION SHOWN HEREIN. IF YOU DO NOT AGREE WITH ANY OF THESE TERMS AND CONDITIONS, DO NOT USE THE INFORMATION.

The information provided in this general information document was formulated using the utmost care; however, it is provided by ams-OSRAM AG or its Affiliates* on an "as is" basis. Thus, ams-OSRAM AG or its Affiliates* does not expressly or implicitly assume any warranty or liability whatsoever in relation to this information, including – but not limited to – warranties for correctness, completeness, marketability, fitness for any specific purpose, title, or non-infringement of rights. In no event shall ams-OSRAM AG or its Affiliates* be liable – regardless of the legal theory – for any direct, indirect, special, incidental, exemplary, consequential, or punitive damages arising from the use of this information. This limitation shall apply even if ams-OSRAM AG or its Affiliates* has been advised of possible damages. As some jurisdictions do not allow the exclusion of certain warranties or limitations of liabilities, the above limitations and exclusions might not apply. In such cases, the liability of ams-OSRAM AG or its Affiliates* is limited to the greatest extent permitted in law.

ams-OSRAM AG or its Affiliates* may change the provided information at any time without giving notice to users and is not obliged to provide any maintenance or support related to the provided information. The provided information is based on special conditions, which means that the possibility of changes cannot be precluded.

Any rights not expressly granted herein are reserved. Other than the right to use the information provided in this document, no other rights are granted nor shall any obligations requiring the granting of further rights be inferred. Any and all rights and licenses regarding patents and patent applications are expressly excluded.

It is prohibited to reproduce, transfer, distribute, or store all or part of the content of this document in any form without the prior written permission of ams-OSRAM AG or its Affiliates* unless required to do so in accordance with applicable law.

* ("Affiliate" means any existing or future entity: (i) directly or indirectly controlling a Party; (ii) under the same direct, indirect or joint ownership or control as a Party; or (iii) directly, indirectly or jointly owned or controlled by a Party. As used herein, the term "control" (including any variations thereof) means the power or authority, directly or indirectly, to direct or cause the direction of the management and policies of such Party or entity, whether through ownership of voting securities or other interests, by contract or otherwise.)

For further information on our products
please see the Product Selector and
scan this QR Code.

Published by ams-OSRAM AG
Tobelbader Strasse 30, 8141 Premstaetten, Austria
ams-osram.com © All Rights Reserved.

Published by ams-OSRAM AG
Tobelbader Strasse 30,
8141 Premstaetten Austria
Phone +43 3136 500-0
ams-osram.com