CMV2000

Datasheet

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CMV2000 Global shutter CMOS image sensor for machine vision

1 General description

The CMV2000 is a high sensitivity, pipelined global shutter CMOS image sensor with 2048 by 1088 pixels (2/3 optical inch) developed for machine vision applications. Pipeline global shutter pixels allow exposure during read-out, while performing CDS operation. The image sensor has sixteen 10 or 12-bit digital LVDS outputs (serial). The image sensor also integrates a programmable gain amplifier and offset regulation. Each channel runs at 480 Mbps maximum which results in 340 fps frame rate at full resolution. Higher frame rates can be achieved in row-windowing mode or row-subsampling mode. These modes are all programmable using the SPI interface. All internal exposure and read-out timings are generated by a programmable on-board sequencer. External triggering and exposure programming is also possible. Extended optical dynamic range can be achieved by multiple integrated high dynamic range modes.

1.1 Key benefits & features

The benefits and features of CMV2000, Global shutter CMOS image sensor for machine vision are listed below:

Table 1: Added value of using CMV2000

Benefits	Features
Freeze moving objects	Global shutter with excellent parasitic light sensitivity of 1/50000
Track moving objects accurately and high inspection rate	High speed 340 fps
Easy HW design	Pin compatible to CMV4000
Choose between maximum frame rate (10-bit) or better image quality (12-bit)	Selectable ADC Resolution
See bright and dark objects at the same time	High dynamic range mode with dual exposure and piecewise linear response option

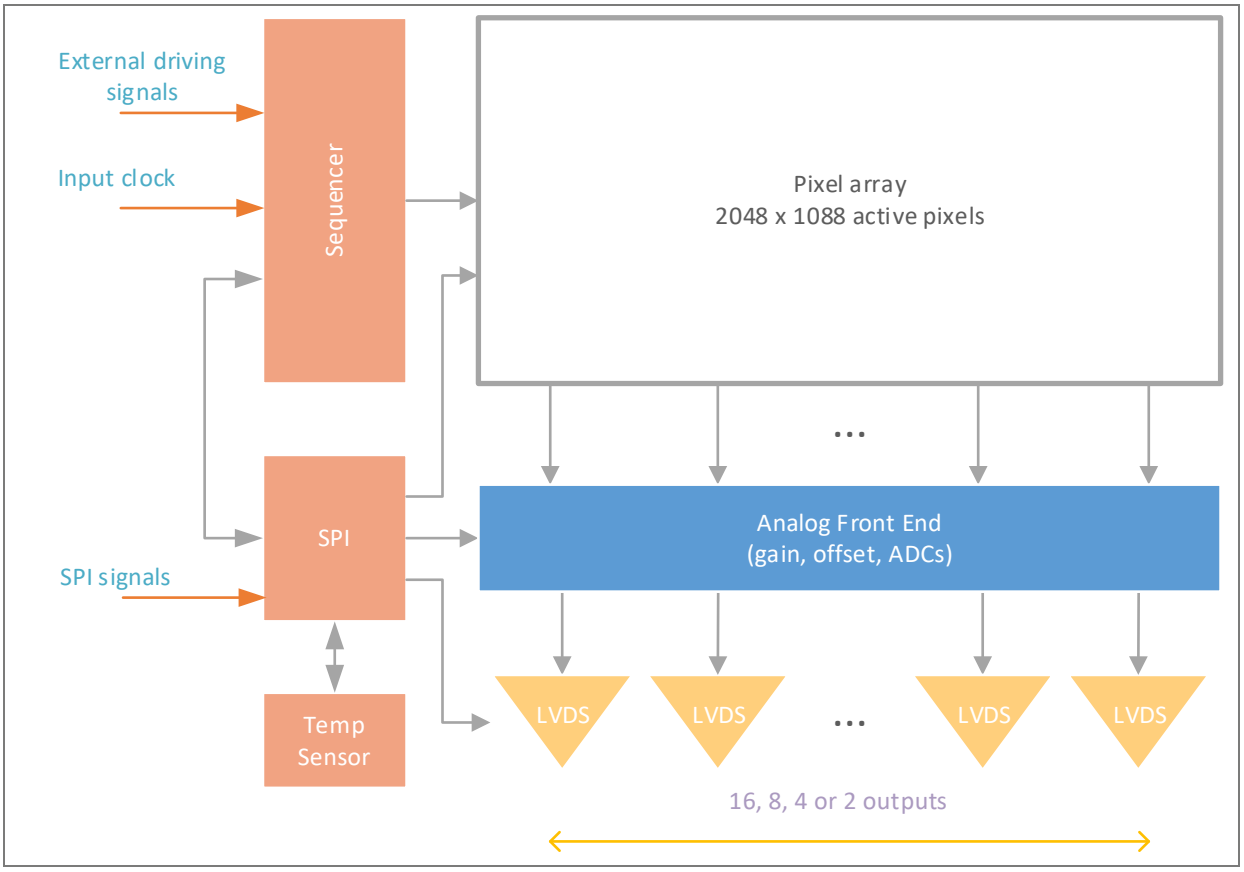
1.2 Applications

- Machine Vision
- 3D Imaging
- Motion Capture
- Bar and 2D Code Scanning
- Intelligent traffic systems
- Video and Broadcast
- Biometrics

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 2: Functional blocks of CMV2000



2 Ordering information

Product type/Marking	Ordering code	Mono/Color	Glass type	Package	Delivery quantity
CMV2000-2E12M1PP	Q65114A0002	Mono	Plain glass	PGA	60 pcs/tray
CMV2000-2E5C1PP	Q65114A0005	Color	Plain glass	PGA	60 pcs/tray
CMV2000-2E5M1LP	Q65114A0009	Mono	Plain glass	LGA	60 pcs/tray
CMV2000-2E5C1LP	Q65114A0004	Color	Plain glass	LGA	60 pcs/tray
CMV2000-2E5M1PP	Q65114A0010	Mono	Plain glass	PGA	60 pcs/tray
CMV2000-3E12M1CA	Q65114A0029	Mono	AR coating	LCC	60 pcs/tray
CMV2000-3E12M1PP	Q65114A0031	Mono	Plain glass	PGA	60 pcs/tray
CMV2000-3E5C1CA	Q65114A0023	Color	AR coated	LCC	60 pcs/tray
CMV2000-3E5C1PP	Q65114A0024	Color	Plain glass	PGA	60 pcs/tray
CMV2000-3E5M1CA	Q65114A0025	Mono	AR coated	LCC	60 pcs/tray
CMV2000-3E5M1PA	Q65114A0027	Mono	AR coated	PGA	60 pcs/tray
CMV2000-3E5M1PP	Q65114A0028	Mono	Plain glass	PGA	60 pcs/tray

Figure 3: Ordering code information

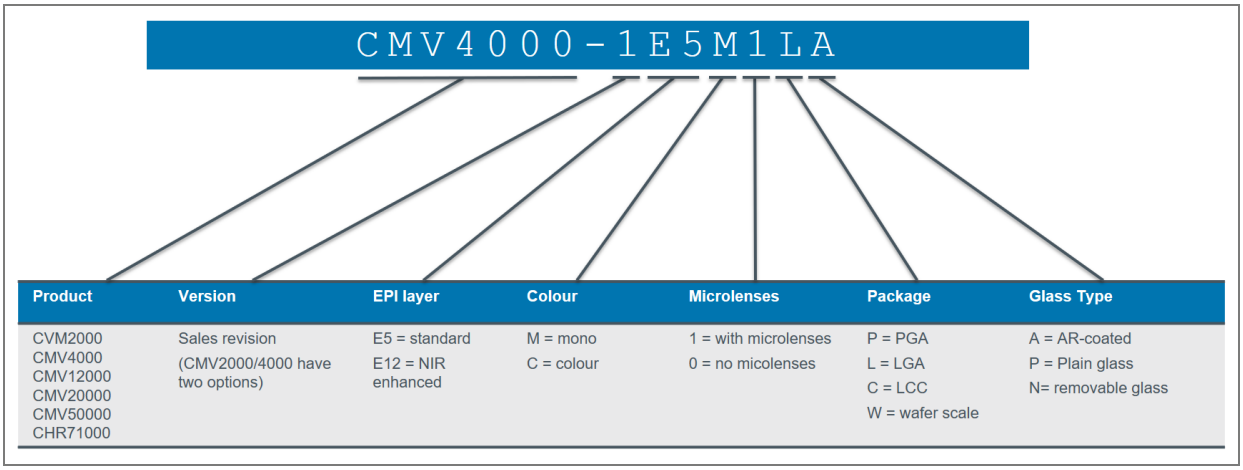


Table 1: Differences between versions

Topic	Version2	Version3
PGA		Additional gain steps
Horizontal line effect	There shall not be a line read out when exposure starts	Horizontal line effect can be avoided by inserting dummy lines at the moment the exposure of the next frame is started.
Black sun effect	Avoiding effect with reduction of the brightness of light falling on the sensor	Actively removing effect
Electrical black columns		Enable by setting the appropriate SPI register for reducing the row noise.
Register settings	The registers addresses and contents are different from version to version. See chapter 8 “Register Description”. Version 3 has different recommended register settings than version 2.	
Integration in single shot mode		Improved integration single shot mode to reduce horizontal line artifact.
PRNU pattern		The pattern will only be visible in grey images starting from around 150DN. Correction can be done with applying a gain correction to each column, which compensates the FPN.
Column patterns in the non-linear part of the response curve		This can be solved by increasing gain to clip the response in its linear part. But setting it too high can cause a drop in saturation value and full well capacity.

3 Pinout

Pins that are marked as optional are not strictly required for sensor operation, they are test pins or pins that are only needed for using a certain feature. When these pins are not used, they can be left floating.

When all 16 LVDS channels are not used, and the sensor is configured for multiplexing, the unused output channels can also be left floating.

3.1 µPGA and LGA pinout

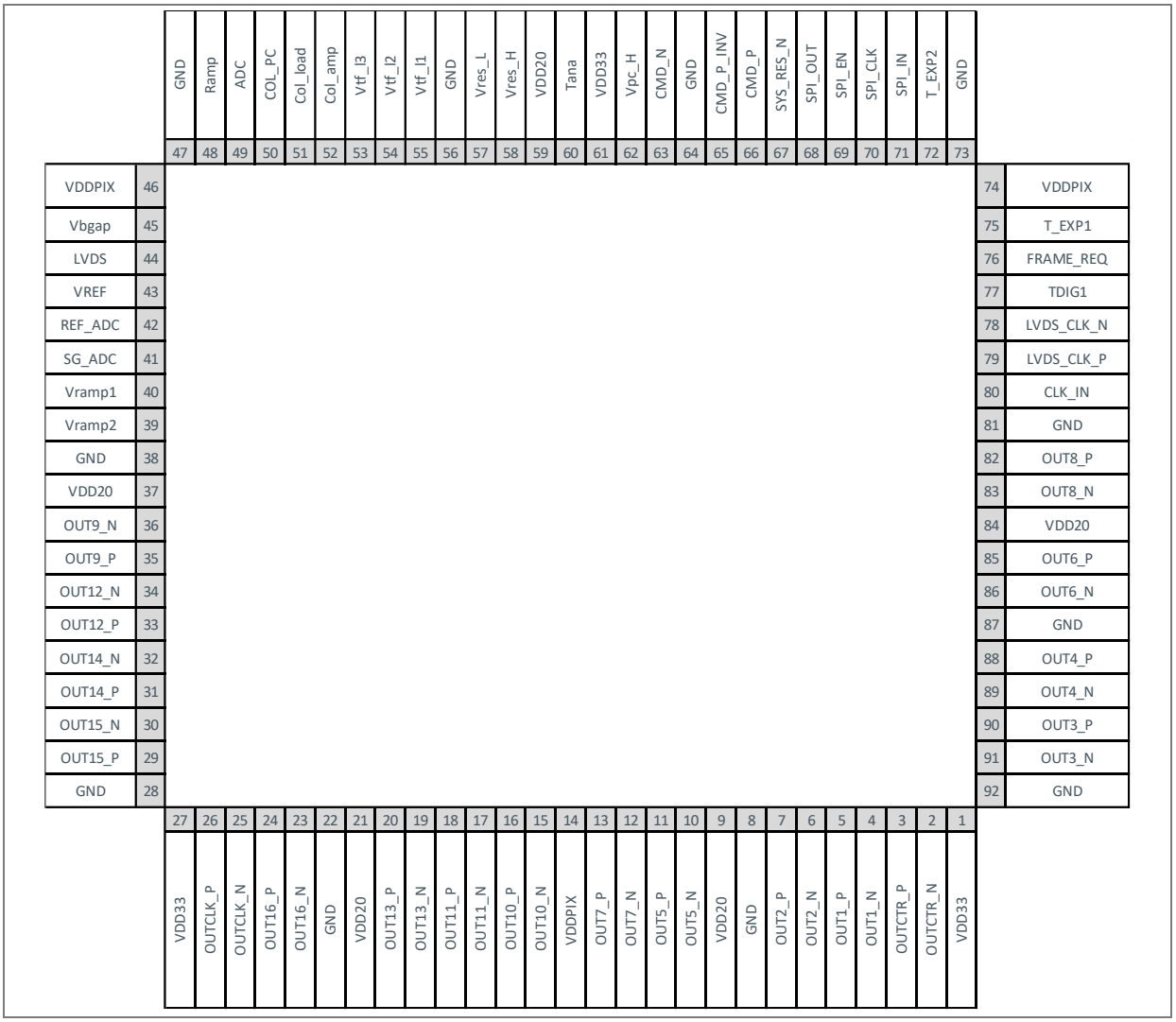
This is the pin layout as seen from the top.

Table 2: µPGA and LGA pinout

	1	2	3	4	5	6	7	8	9	10	11	12
H	VDD33	TDIG1	T_EXP1	SPI_CLK	SYS_RES_N	VDD33	GND	Vres_L	Vtf_l3	COL_PC	LVDS	DIO2
G	VDDPIX	TDIG2	T_EXP2	SPI_EN	CMD_P	CMD_N	Tana	Vtf_l1	Col_amp	ADC	Vbgap	VDDPIX
F	GND	FRAME_REQ	SPI_IN	SPI_OUT	CMD_P_INV	Vpch_H	Vres_H	Vtf_l2	Col_load	Ramp	DIO1	GND
E	CLK_IN	VDD33	GND	VDD20	GND	VDDPIX	VDD20	VDD20	GND	SG_ADC	Vramp1	Vramp2
D	LVDS_CLK_P	LVDS_CLK_N	OUT3_N	OUT3_P	OUT8_N	OUT8_P	OUT9_N	OUT9_P	OUT14_N	OUT14_P	VREF	REF_ADC
C	GND	OUT1_N	OUT1_P	OUT6_N	OUT6_P	GND	VDD20	OUT11_N	OUT11_P	OUT16_N	OUT16_P	GND
B	OUTCTR_N	OUTCTR_P	OUT4_N	OUT4_P	OUT7_N	OUT7_P	OUT10_N	OUT10_P	OUT13_N	OUT13_P	OUTCLK_N	OUTCLK_P
A		OUT2_N	OUT2_P	OUT5_N	OUT5_P	GND	VDD20	OUT12_N	OUT12_P	OUT15_N	OUT15_P	GND

3.2 LCC pinout

Figure 4: LCC pinout



3.3 Pining list

The pin list of the CMV2000 can be found below for the µPGA and LCC packages. The pin list for the LGA package is the same as for the µPGA package.

Table 3: Pinout in detail

µPGA	LCC	Pin name	Description	Type
G7	60	Tana	Test pin for analog signals (optional)	Analog output
D12	42	REF_ADC	Reference for ADC testing (decouple with 100 nF to ground)	Bias
E10	41	SG_ADC	Signal for ADC testing (decouple with 100 nF to ground)	Bias
E11	40	Vramp1	Start voltage first ramp (decouple with 100 nF to ground)	Bias
E12	39	Vramp2	Start voltage second ramp (decouple with 100 nF to ground)	Bias
F6	62	Vpch_H	Precharge high voltage (decouple with 100 nF to ground)	Bias
H8	57	Vres_L	Reset low voltage (decouple with 100 nF to ground)	Bias
F8	54	Vtf_l2	Transfer low voltage 2 (decouple with 100 nF to ground)	Bias
H9	53	Vtf_l3	Transfer low voltage 3 (decouple with 100 nF to ground)	Bias
D11	43	VREF	Reference for column amps (decouple with 100 nF to ground)	Bias
F9	51	Col_load	Decouple with 100 nF to ground	Bias
G9	52	Col_amp	Decouple with 100 nF to ground	Bias
G6	63	CMD_N	Decouple with 100 nF to ground	Bias
G11	45	Vbgap	Decouple with 100 nF to ground	Bias
H10	50	COL_PC	Decouple with 100 nF to ground	Bias
H11	44	LVDS	Decouple with 100 nF to ground	Bias
G5	66	CMD_P	Decouple with 100 nF to VDD33	Bias
F5	65	CMD_P_INV	Decouple with 100 nF to VDD33	Bias
F10	48	ramp	Decouple with 100 nF to VDD33	Bias
G10	49	ADC	Decouple with 100 nF to VDD33	Bias
G8	55	Vtf_l1	Transfer low voltage 1 (connect to ground)	Bias
H5	67	SYS_RES_N	Input pin for sequencer reset	Digital input
E1	80	CLK_IN	Master input clock	Digital input
F2	76	FRAME_REQ	Frame request pin	Digital input
G3	72	T_EXP2	Input pin for external exposure mode (optional)	Digital input

µPGA	LCC	Pin name	Description	Type
H3	75	T_EXP1	Input pin for external exposure mode (optional)	Digital input
G4	69	SPI_EN	SPI enable input pin	Digital input
H4	70	SPI_CLK	SPI clock input pin	Digital input
F3	71	SPI_IN	SPI data input pin	Digital input
F4	68	SPI_OUT	SPI data output pin	Digital output
G2	N.E.	TDIG2	Test pin for digital signals (optional)	Digital output
H2	77	TDIG1	Test pin for digital signals (optional)	Digital output
A6	8	GND	Ground pin	Ground
A12	22	GND	Ground pin	Ground
C1	28	GND	Ground pin	Ground
C6	38	GND	Ground pin	Ground
C12	47	GND	Ground pin	Ground
E3	56	GND	Ground pin	Ground
E5	64	GND	Ground pin	Ground
E9	73	GND	Ground pin	Ground
F1	81	GND	Ground pin	Ground
F12	87	GND	Ground pin	Ground
H7	92	GND	Ground pin	Ground
D1	79	LVDS_CLK_P	LVDS positive input clock	LVDS input
D2	78	LVDS_CLK_N	LVDS negative input clock	LVDS input
B11	25	OUTCLK_N	LVDS negative clock output channel	LVDS output
B12	26	OUTCLK_P	LVDS positive clock output channel	LVDS output
B1	2	OUTCTR_N	LVDS negative control output channel	LVDS output
B2	3	OUTCTR_P	LVDS positive control output channel	LVDS output
C2	4	OUT1_N	LVDS negative data output channel 1	LVDS output
C3	5	OUT1_P	LVDS positive data output channel 1	LVDS output
A2	6	OUT2_N	LVDS negative data output channel 2	LVDS output
A3	7	OUT2_P	LVDS positive data output channel 2	LVDS output
D3	91	OUT3_N	LVDS negative data output channel 3	LVDS output
D4	90	OUT3_P	LVDS positive data output channel 3	LVDS output
B3	89	OUT4_N	LVDS negative data output channel 4	LVDS output
B4	88	OUT4_P	LVDS positive data output channel 4	LVDS output
A4	10	OUT5_N	LVDS negative data output channel 5	LVDS output
A5	11	OUT5_P	LVDS positive data output channel 5	LVDS output
C4	86	OUT6_N	LVDS negative data output channel 6	LVDS output
C5	85	OUT6_P	LVDS positive data output channel 6	LVDS output

µPGA	LCC	Pin name	Description	Type
B5	12	OUT7_N	LVDS negative data output channel 7	LVDS output
B6	13	OUT7_P	LVDS positive data output channel 7	LVDS output
D5	83	OUT8_N	LVDS negative data output channel 8	LVDS output
D6	82	OUT8_P	LVDS positive data output channel 8	LVDS output
D7	36	OUT9_N	LVDS negative data output channel 9	LVDS output
D8	35	OUT9_P	LVDS positive data output channel 9	LVDS output
B7	15	OUT10_N	LVDS negative data output channel 10	LVDS output
B8	16	OUT10_P	LVDS positive data output channel 10	LVDS output
C8	17	OUT11_N	LVDS negative data output channel 11	LVDS output
C9	18	OUT11_P	LVDS positive data output channel 11	LVDS output
A8	34	OUT12_N	LVDS negative data output channel 12	LVDS output
A9	33	OUT12_P	LVDS positive data output channel 12	LVDS output
B9	19	OUT13_N	LVDS negative data output channel 13	LVDS output
B10	20	OUT13_P	LVDS positive data output channel 13	LVDS output
D9	32	OUT14_N	LVDS negative data output channel 14	LVDS output
D10	31	OUT14_P	LVDS positive data output channel 14	LVDS output
A10	30	OUT15_N	LVDS negative data output channel 15	LVDS output
A11	29	OUT15_P	LVDS positive data output channel 15	LVDS output
C10	23	OUT16_N	LVDS negative data output channel 16	LVDS output
C11	24	OUT16_P	LVDS positive data output channel 16	LVDS output
A7	9	VDD20	2.1 V supply	Supply
C7	21	VDD20	2.1 V supply	Supply
E4	37	VDD20	2.1 V supply	Supply
E7	59	VDD20	2.1 V supply	Supply
E8	84	VDD20	2.1 V supply	Supply
E6	14	VDDPIX	3.0 V supply	Supply
G1	46	VDDPIX	3.0 V supply	Supply
G12	74	VDDPIX	3.0 V supply	Supply
F7	58	Vres_H	3.3 V supply	Supply
E2	1	VDD33	3.3 V supply	Supply
H1	27	VDD33	3.3 V supply	Supply
H6	61	VDD33	3.3 V supply	Supply
F11	N.E(1)	DIO1	Diode 1 for test (not connected)	Test
H12	N.E(1)	DIO2	Diode 2 for test (not connected)	Test

(1) Not equipped

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5: Absolute maximum ratings of CMV2000

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
VDD20	Digital supply LVDS, ADC	2.0	2.2	V	
VDD33	Analog supply ADC, PGA	3.0	3.6	V	
VDDPIX	Analog pixel supply	2.3	3.6	V	
Vres_h	Analog pixel reset supply	3.0	3.6	V	
Continuous power dissipation (T_A = 70 °C)					
P_T	Continuous power dissipation		4.2	W	At max. frame rate
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM		± 2	kV	JS-001-2014
Temperature ranges and storage conditions					
T_J	Operating junction temperature	-30	70	°C	
T_{STRG}	Storage temperature range	20	40	°C	
RH_{NC}	Relative humidity (non-condensing)	30	60	%	

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 6: Electrical characteristics of CMV2000

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supplies						
VDD20	Digital supply LVDS, ADC	Version2	2.05	2.1	2.15	V
		Version3	2.0	2.0	2.15	V
VDD33	Analog supply ADC, PGA		3.2	3.3	3.4	V
VDDPIX	Analog pixel supply		2.9	3.0	3.1	V
Vres_h	Analog pixel reset supply		3.2	3.3	3.4	V
IDD20	Supply current	Readout @ Version2		370		mA
		Readout @ Version3		300		mA
IDD33	Supply current	Readout @ Version2		65		mA
		Readout @ Version3		80		mA
IDDPIX	Supply current	Readout @ Version2		20		mA
		Readout @ Version3		20		mA
Ires_h	Supply current	Readout		15		mA
P20	Power consumption	Version2		780		mW
		Version3		640		mW
P33	Power consumption	Version2		220		mW
		Version3		270		mW
PPIX	Power consumption			60		mW
Pres_h	Power consumption			50		mW
Digital I/O CMOS/TTL DC						
V_{IH}	High level input voltage		2.0		VDD33	V
V_{IL}	Low level input voltage		GND		0.8	V
V_{OH}	High level output voltage	VDD=3.3 V I_{OH}=-2 mA	2.4			V
V_{OL}	Low level output voltage	VDD=3.3 V I_{OH}=-2 mA			0.4	V
Ci	Input load				2	pF
Co	Output load				2	pF
f_{CLK_IN}	CLK_IN frequency		5		48	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TIA/EIA-644A LVDS - driver specifications (OUTX_N/P, OUTCLK_N/P, OUTCTR_N/P)						
V_{OD}	Differential output voltage	Steady State, RL = 100 Ω	247	350	454	mV
ΔV_{OD}	Difference in V_{OD} between complementary output states	Steady State, RL = 100 Ω			50	mV
V_{OC}(1)	Common mode voltage	Steady State, RL = 100 Ω	1.26	1.37	1.50	V
ΔV_{OC}	Difference in V_{OC} between complementary output states	Steady State, RL = 100 Ω			50	mV
$I_{OS,GND}$	Output short circuit current to ground	$V_{OUTP} = V_{OUTN} = GND$			24	mA
$I_{OS,PN}$	Output short circuit current	$V_{OUTP} = V_{OUTN}$			12	mA
TIA/EIA-644A LVDS-receiver specifications (LVDS_CLK_N/P)						
V_{ID}	Differential input voltage	Steady state	100	350	600	mV
V_{IC}	Receiver input range	Steady state	0.0		2.4	V
I_{ID}	Receiver input current	$V_{INP\|INN} = 1.2\ V \pm 50\ mV$, $0 \le V_{INP\|INN} \le 2.4\ V$			20	µA
ΔI_{ID}	Receiver input current difference	$\|I_{INP} - I_{INN}\|$			6	µA
Timing						
CLK_IN			5		48	MHz
LVDS_CLK_N/P			50		480	MHz
SPI_CLK					48	MHz

(1) V_{oc} is dependent on the 2.1 V supply voltage; therefore, these values differ from the TIA/EIA-644A spec.

6 Specification overview

Below are the typical electro-optical specifications of CMV2000. These are typical values with typical supplies at room temperature.

Table 7: Electro-optical characteristics

Specification	Value	Comment
Effective pixels	2048 x 1088	
Pixel pitch	5.5 x 5.5 µm^2	
Optical format	2/3”	
Full well charge	13.5 ke$^-$	Pinned photodiode pixel
Conversion gain	0.075 LSB/e$^-$	10-bit mode, unity gain
Sensitivity	5.56 V/lux.s 0.27 A/W	With microlenses @ 550 nm
Temporal noise (analog domain)	13 e$^-$	Pipelined global shutter (GS) with correlated double sampling (CDS). Read noise
Dynamic range	60 dB	
Pixel type	Global shutter pixel	Allows fixed pattern noise correction and reset (kTC) noise canceling through correlated double sampling.
Shutter type	Pipelined global shutter	Exposure of next image during read-out of the previous image.
Parasitic light sensitivity - Shutter efficiency	<1/50 000 >99.998%	
Color filters	Optional	RGB Bayer pattern
Micro lenses	Yes	
Fill factor	42%	W/o micro lens
QE * FF	60%	@ 550 nm with micro lenses.
Dark current signal	125 e$^-$/s	@ 25 °C die temperature. The dark current doubles with every 6.5 °C increase
DSNU	3 LSB/s	10-bit mode
Fixed pattern noise	<1 LSB RMS	<0.1% of full swing, 10-bit mode
PRNU	< 1% RMS of signal	
LVDS output channel	16	Each data output running @ 480 Mbit/s. 8, 4 and 2 outputs selectable at reduced frame rate
Frame rate	340 frames/s	Using a 10-bit/pixel and 480 Mbit/s LVDS. Higher frame rate possible in row windowing mode.
Timing generation	On-chip	Possibility to control exposure time through external pin.
PGA	Yes	4 analog gain settings
Programmable registers	Sensor parameters	Window coordinates, Timing parameters, Gain & offset, Exposure time, flipped read-out in X and Y direction …

Specification	Value	Comment
Supported HDR modes	Multi-frame read-out with different exposure time	Successive frames are read out with increasing exposure times. The final image is a combination (externally) of these frames.
	Interleaved integration times	Interleaved exposure times for different rows: Odd rows (double rows for color) have a different exposure compared to even rows (double rows for color). Final image is a combination of the two (through interpolation).
	Piecewise linear response	Response curve with two knee points.
ADC	10-bit/12-bit	Column ADC
Interface	LVDS	Serial output data + synchronization signals
I/O logic levels	LVDS = 1.8 V Dig. I/O = 3.3 V	
Supply voltages	Version 2: 2.1 V Version 3: 2.0 V	LVDS, ADC
	3.0 V	Pixel array supply
	3.3 V	Dig. I/O, SPI, PGA
Clock inputs	CLK_IN	Between 5 and 48 MHz
	LVDS_CLK_N/P	Between 50 and 480 MHz, LVDS
	SPI_CLK	Max. 48 MHz
Power	550 mW to 1200 mW	Actual wattage is dependent on the used configuration
Package	Custom ceramic package	µPGA (95 pins)
		LGA (95 pins)
		LCC (92 pins)
Operating range	-30 °C to 70 °C	Dark current and noise performance will degrade at higher temperature
Cover glass	D263	Plain or AR glass, no IR cut-off filter on color devices
ESD	Class 1A HBM	
	Class 4C CDM	
RoHS	Compliant	

6.1 Spectral characteristics

The cover glass of the CMV2000 is plain D263 glass with a transmittance as shown in Figure 8. Refraction index of the glass is 1.52.

When a color sensor is used an IR-cutoff filter should be placed in the optical path of the sensor.

Figure 8: Transmittance curve offer D263 cover plain glass

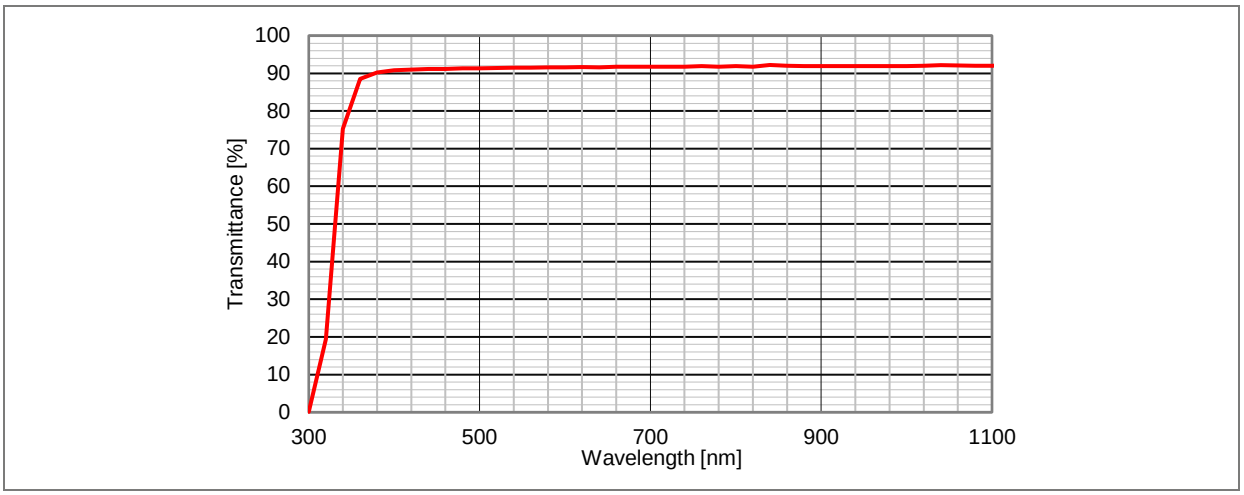
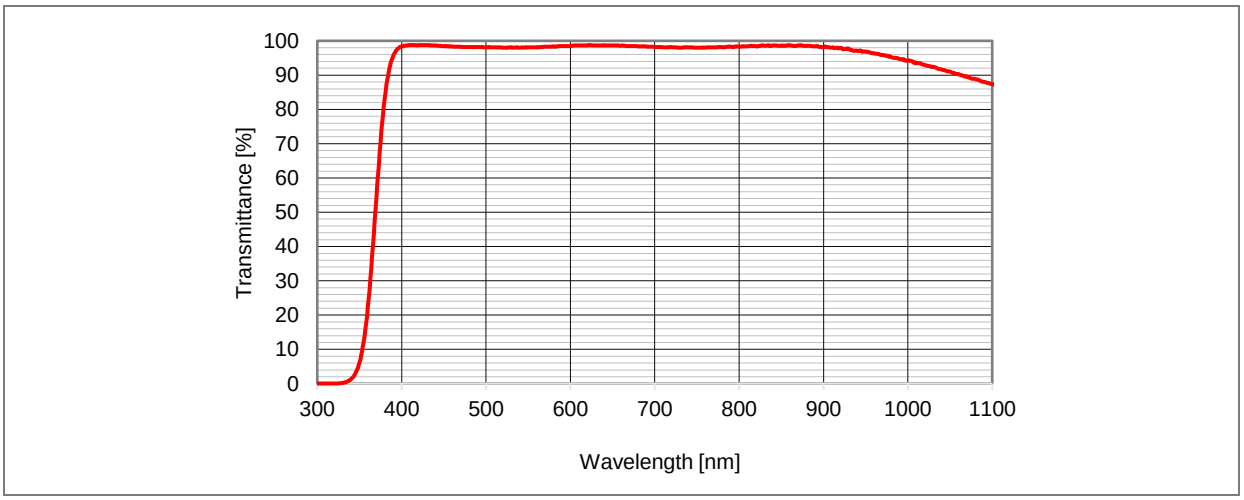
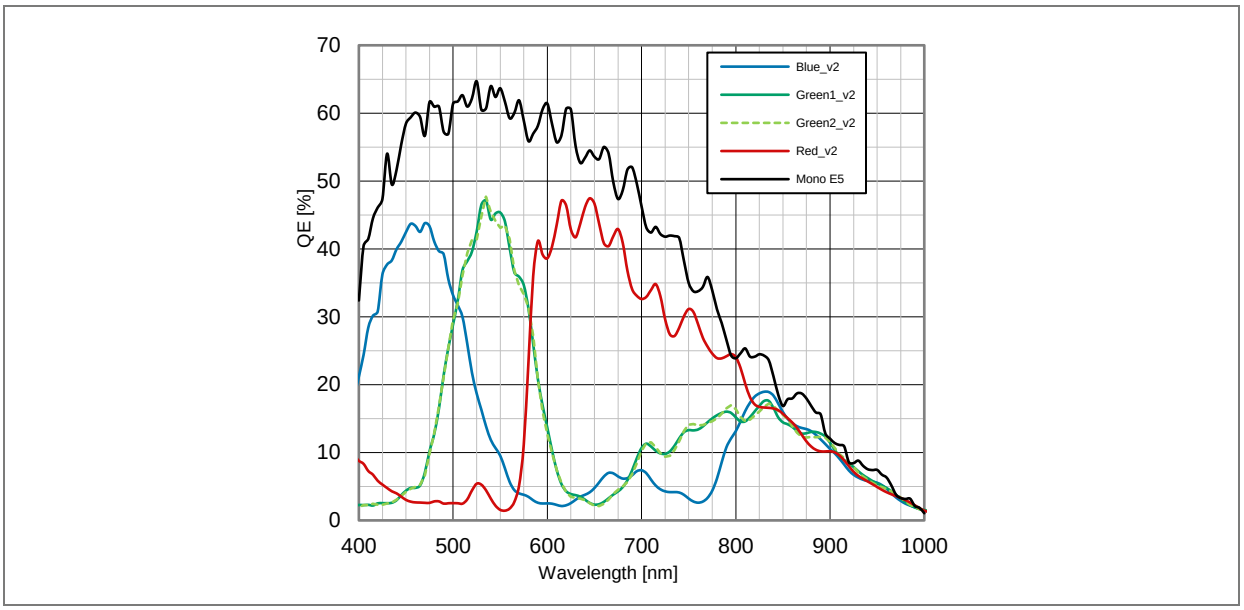


Figure 9: Transmittance curve for D263 AR coated glass



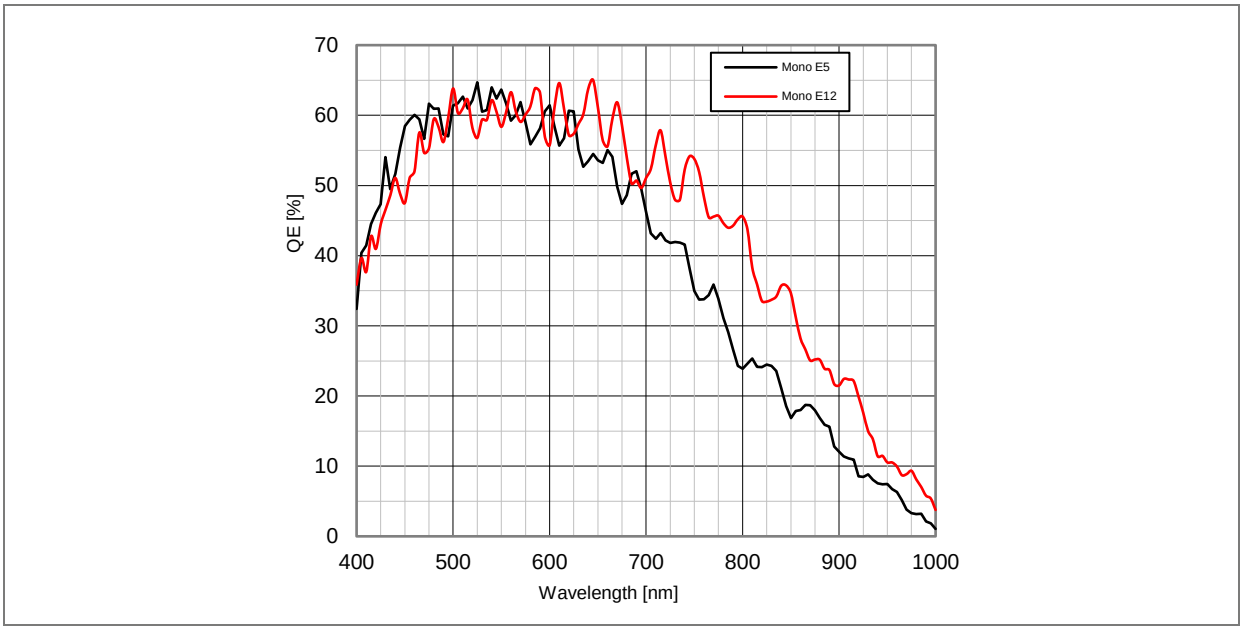
When a color version of the CMV2000 is used, the color filters are applied in a Bayer pattern. The color version of the CMV2000 always has microlenses. The typical spectral response of the CMV with color filters and D263 cover glass is shown in Figure 10. The use of an IR cut-off filter in the optical path of the CMV2000 image sensor is necessary to obtain good color separation when using light with an NIR component. The typical spectral response of a monochrome CMV2000 with microlenses can be found in Figure 10 as well.

Figure 10: Typical spectral response of CMV2000 with RGB color filters and D263 cover glass



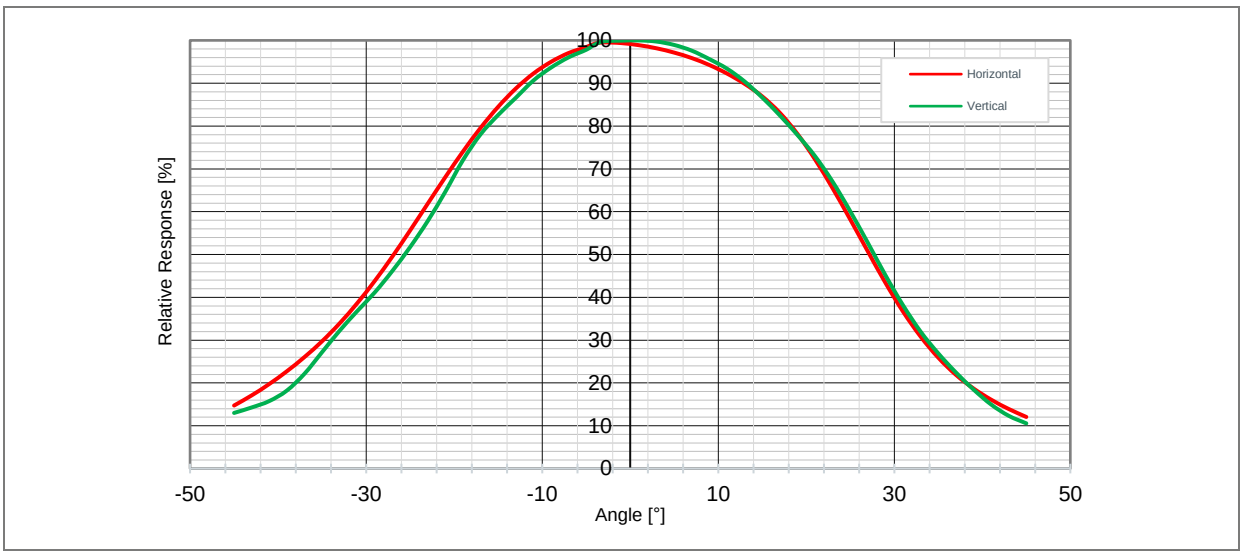
A variation from the standard CMV2000 image sensors is processed on 12 µm epi (E12) Si wafers. The thicker epi-layer wafer starting material increases significantly the QE for wavelengths above 600 nm. Around 900 nm the QE is about doubled and increases from 8% to 16%. This is shown in Figure 11.

Figure 11: Response of E12 devices and normal devices



The typical angular response for a CMV2000 sensor can be seen in Figure 12. The data includes horizontal and vertical angles.

Figure 12: Horizontal and vertical angular response



7 Functional description

7.1 Sensor architecture

Figure 2 shows the image sensor architecture. The internal sequencer generates the necessary signals for image acquisition. The image is stored in the pixel (global shutter) and is then read out sequentially, row-by-row. On the pixel output, an analog gain of x1, x1.2, x1.4 and x1.6 is possible. The pixel values then passes to a column ADC cell, in which ADC conversion is performed. The digital signals are then read out over multiple LVDS channels. Each LVDS channel reads out 128 adjacent columns of the array. In the Y-direction, rows of interest are selected through a row-decoder which allows a flexible windowing. Control registers are foreseen for the programming of the sensor. These register parameters are uploaded via a four-wire SPI interface. A temperature sensor which can be read out over the SPI interface is also included.

7.1.1 Pixel array

The pixel array consists of 2048 x 1088 square global shutter pixels with a pitch of 5.5 µm (5.5 µm x 5.5 µm). This results in an optical area of close to 2/3 optical inch (12.7 mm). This means that most off-the-shelf C-mount lenses can be used.

The pixels are designed to achieve maximum sensitivity with low noise and low PLS specifications. Micro lenses are placed on top of the pixels for improved fill factor and quantum efficiency (>50%).

7.1.2 Analog front end

The analog front end consists of 2 major parts, a column amplifier block and a column ADC block.

The column amplifier prepares the pixel signal for the column ADC and applies analog gain if desired (programmable using the SPI interface). The column ADC converts the analog pixel value to a 10 or 12-bit value. A digital offset can also be applied to the output of the column ADC’s. All gain and offset settings can be programmed using the SPI interface.

7.1.3 LVDS block

The LVDS block converts the digital data coming from the column ADC into standard serial LVDS data running at maximum 480 Mbps. The sensor has 18 LVDS output pairs:

- 16 Data channels
- 1 Control channel
- 1 Clock channel

The 16 data channels are used to transfer 10-bit or 12-bit data words from sensor to receiver. The output clock channel transports a DDR clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. The data on the control channel contains status information on the validity of the data on the data channels, among other useful sensor status information. Details on the LVDS timing and format can be found in chapter 7.3 of this document.

LVDS requires parallel termination at the receiver side. So, between LVDS_CLK_P (pin D1) and LVDS_CLK_N (pin D2) should be an external 100Ω resistor. Also, all the LVDS outputs should all be externally terminated at the receiver side. See the TIA/EIA-644A standard for details.

7.1.4 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control clocks. This sequencer can be activated and programmed through the SPI interface. A detailed description of the SPI registers and sensor (sequencer) programming can be found in chapter 7.3.1 of this document.

7.1.5 SPI interface

The SPI interface is used to load the sequencer registers with data. The data in these registers are used by the sequencer while driving and reading out the image sensor. Features like windowing, subsampling, gain and offset are programmed using this interface. The data in the on-chip registers can also be read back for test and debug of the surrounding system. Chapter 7.2.2 contains more details on SPI programming and timing.

7.1.6 Temperature sensor

A 16-bit digital temperature sensor is included in the image sensor and can be controlled by the SPI-interface. The on-chip temperature can be obtained by reading out the registers with address 126 and 127 (in burst mode, see chapter 7.2.8.2 for more details on this mode).

A calibration of the temperature sensor is needed for absolute temperature measurements per device because the offset differs from device to device. The temperature sensor requires a running input clock (CLK_IN), the other functions of the image sensor can be operational or in standby mode. The output value of the sensor is dependent on the input clock. A typical temperature sensor output vs. temperature curve at 40 MHz can be found in Figure 13. The die temperature will be about 10 °C~15 °C higher than ambient temperature. The ceramic package has about the same temperature as the die.

The typical (offset) value of the temperature sensor at 0 °C would be: 1000* (f [MHz])/40 DN. This offset can differ per device. A typical slope would be around 0.3*40/f[MHz] °C/DN.

Figure 13: Typical output of the temperature sensor of the CMV2000

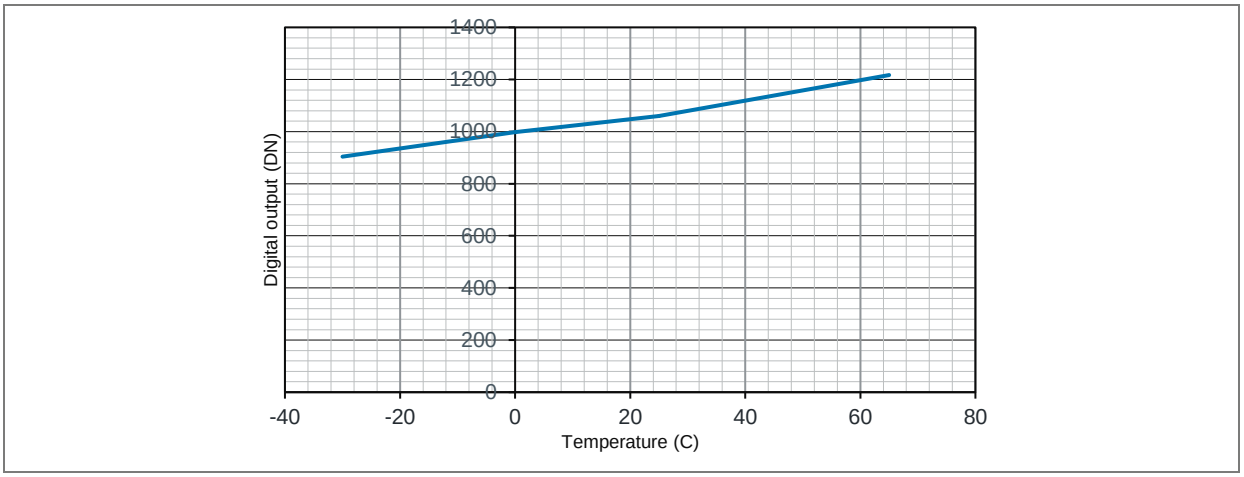
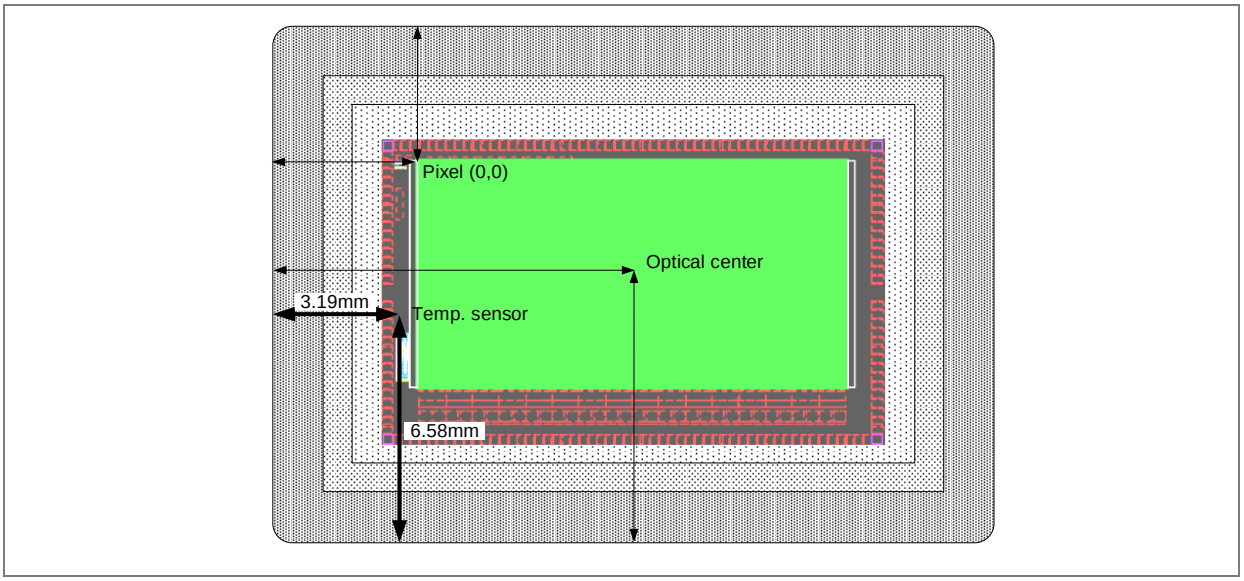


Figure 14: Location of the temperature sensor



7.2 Operating the sensor

This section explains how to connect and power the sensor, as well as basic recipes of how to configure the sensor in a certain operation mode.

7.2.1 Power supplies

To power the sensor, eight externally generated supplies are required as listed in Table 6.

Table 4: Different power supplies

Supply name	Usage	Description
VDD20	LVDS, ADC	Digital supply
VDD33	Dig. I/O, PGA, SPI, ADC	Analog supply
VDDPIX	Pixel array power supply	Analog pixel supply
Vres_h	Pixel reset pulse	Analog pixel reset supply

The power figures are measured at 48 MHz CLK_IN speed in 16 channels mode while constantly grabbing images. When idle, the sensor will consume about 30% less energy. Reducing the amount of output channels will reduce power consumption of the VDD20 supply and will have the biggest impact on the power consumption.

All variations on the VDD33 and VDDPIX can contribute to variations (noise) on the analog pixel signal, which is seen as noise in the image. During the camera design, precautions have to be taken to supply the sensor with very stable supply voltages to avoid this additional noise.

Because of the peak currents, decoupling is advised. Place large decoupling capacitors directly at the output of the voltage regulator to filter low noise and improve peak current supply. We advise 1x 330 µF electrolytic, 1x 33 µF tantalum and a 10 µF ceramic capacitor per supply, directly at the output of the regulator.

Place small decoupling capacitors as close as possible to the sensor between supply pins and ground. We advise 1x 4.7 µF and 1x 100 nF ceramic capacitor per power supply pin (see pin list) and 1x 100 µF ceramic capacitor per power supply plane (VDD20, VDDPIX, VDD33). Vres_h does not need a 100 µF capacitor. See the pin list for exact pin numbers for every supply. Analog and digital ground can be tied together.

7.2.2 Biasing

For optimal performance, some pins need to be decoupled to ground or to VDD. Please refer to the pin list for a detailed description for every pin and the appropriate decoupling if applicable.

7.2.3 Digital input pins

Table 5 gives an overview of the external pins used to drive the sensor. The digital signals are sampled on the rising edge of the CLK_IN, therefore the length of the signal applied to an input should be at least 1 CLK_IN period to assure it has been detected. All digital I/O's have a capacitance of 2 pF max.

Table 5: Digital input pins description

Pin name	Description
CLK_IN	Master input clock, frequency range between 5 and 48 MHz.
LVDS_CLK_N/P	High speed LVDS input clock, frequency range between 50 and 480 MHz.
SYS_RES_N	System reset pin, active low signal. Resets the on-board sequencer and must be kept low during start-up. This signal should be at least one period of CLK_IN long to assure detection on the rising edge of CLK_IN.
FRAME_REQ	Frame request pin. When a high level is detected on this pin the programmed number of frames is captured and sent by the sensor. This signal should be at least one period of CLK_IN long to assure detection on the rising edge of CLK_IN.
SPI_IN	Data input pin for the SPI interface. The data to program the image sensor is sent over this pin.
SPI_EN	SPI enable pin. When this pin is high the data should be written/read on the SPI.
SPI_CLK	SPI clock. This is the clock on which the SPI runs.
T_EXP1	Input pin to program the exposure time externally. Optional
T_EXP2	Input pin to program the exposure time externally in HDR mode. Optional

7.2.4 Input clock

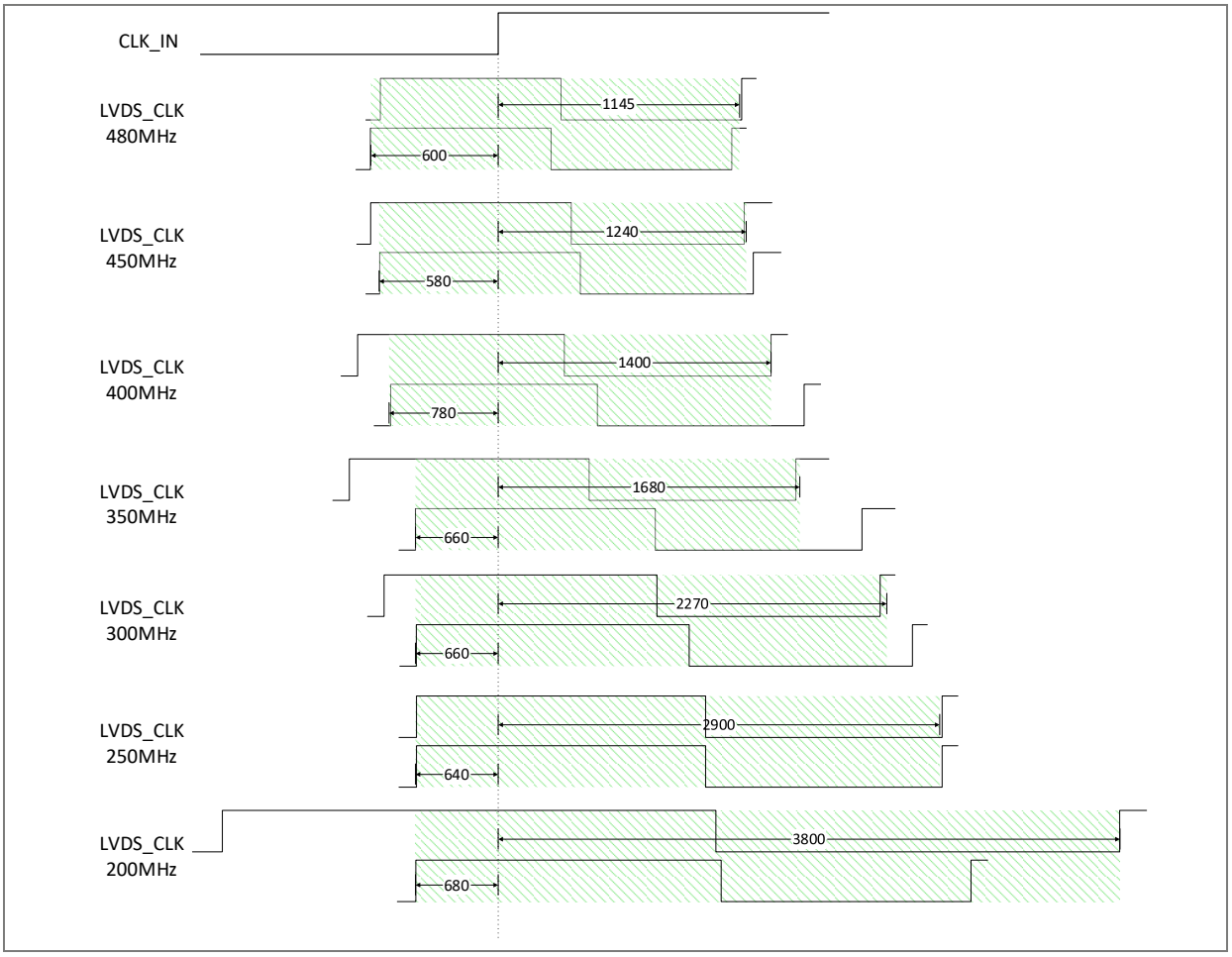
The high-speed LVDS input clock (LVDS_CLK_N/P) defines the output data rate of the CMV2000. The master clock (CLK_IN) must be 10 or 12 times slower depending on the programmed bit mode setting. The maximum data rate of the output is 480 Mbps which results in a LVDS_CLK_N/P of 480 MHz and a CLK_IN of 48 MHz in 10-bit mode and 40 MHz in 12-bit mode. The minimum frequencies are 5 MHz for CLK_IN and 50MHz for LVDS_CLK_N/P. Any frequency between the minimum and maximum can be applied by the user and will result in a corresponding output data rate, like showed in Table 6.

Table 6: Output data rate depending on the CLK_IN and bit mode

CLK_IN	LVDS_CLK 10-bit	LVDS_CLK 12-bit
5 MHz	50 MHz	60 MHz
40 MHz	400 MHz	480 MHz
48 MHz	480 MHz	N/A

The rising edge LVDS input clock can have a limited delay with respect to the rising edge of the master input clock, depending on clock speed. In Figure 15, the skew limits are shown for different clock speeds and for an LVDS clock that rises before and after the master input clock. To assure proper working of the sensor, the skew of the LVDS clock should always fall within these limits, shown as the green area.

Figure 15: LVDS clock delay versus master clock – applicable for V2 of the sensor



7.2.5 Frame rate calculation

The frame rate is defined by 2 main factors:

- Exposure time
- Read-out time

To simplify the calculation we will assume that the exposure time is shorter than the read-out time and that the sensor is operating at default settings, taking a full resolution 10-bit image at 48 MHz through 16 outputs. This means that the frame rate will be defined only by the read-out time because the exposure time happens in parallel with the read-out. The read-out time is defined by:

- Output clock speed: Max 240 MHz
- ADC mode: 10-bit or 12-bit
- Number of lines read-out
- Number of LVDS outputs used: Max 16 outputs

If any of these parameters is changed, it will have an impact on the frame rate. In default operation this will result in 340 fps. The total read-out time is composed of two parts: FOT (frame overhead time) and image read-out time.

The FOT is defined as shown in Equation 1:

Equation 1:

$$FOT = \left(fot\_length + \left(2 * \frac{16}{\#outputs\ used} \right) \right) * 129 * master\ clock\ period$$

With fot_length (register 73) at its default value of 10, this results in 32.25 µs frame overhead time.

The image read-out time is defined as shown in Equation 2:

Equation 2:

$$Image\ read - out\ time = \left(129 * master\ clock\ period * \frac{16}{\#outputs\ used} \right) * nr\_lines$$

Reading out a full resolution image, this results in 2.924 ms image read-out time.

The total read-out time is now the sum of the FOT and the image read-out time, which results in 32.25 µs + 2.924 ms or 2.9525 ms to read out a single full resolution image. The frame rate is thus 338 fps.

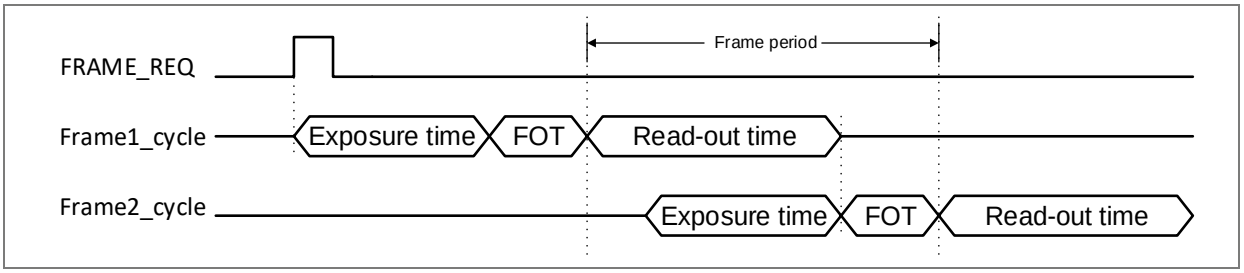
Table 7 gives some examples of how the frame rate increases when reading out a smaller frame in 10-bit mode.

Table 7: Frame rate for different frame size

Number of columns	Number of lines	Frame rate
2048	1088	338
2048	512	710
2048	70	4537

Figure 16 shows the frame period for 2 consecutive frame cycle.

Figure 16: Frame period

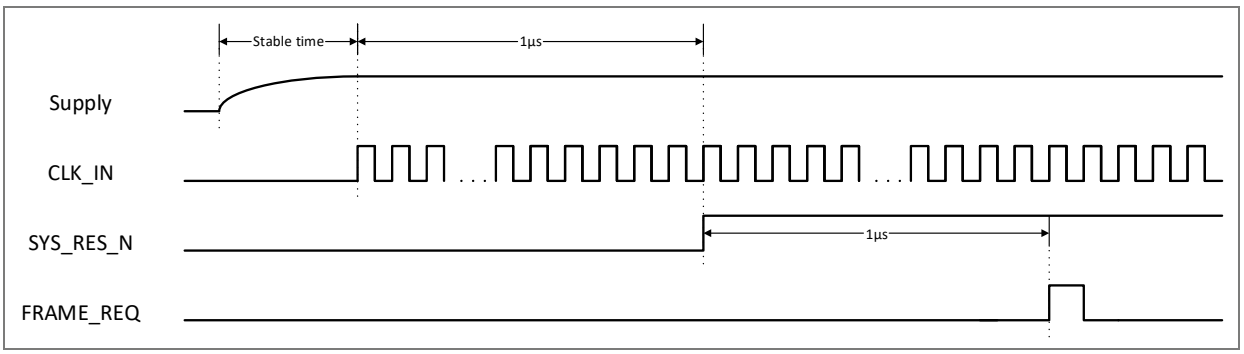


When the exposure time is greater than the read-out time, the frame rate is mostly defined by the exposure time itself (because the exposure time would be much longer than the FOT).

7.2.6 Start-up sequence

The sequence, shown in Figure 17 should be followed when the CMV2000 is started up in default output mode (480 Mbps, 10-bit resolution). There is no specific startup sequence for the power supplies needed.

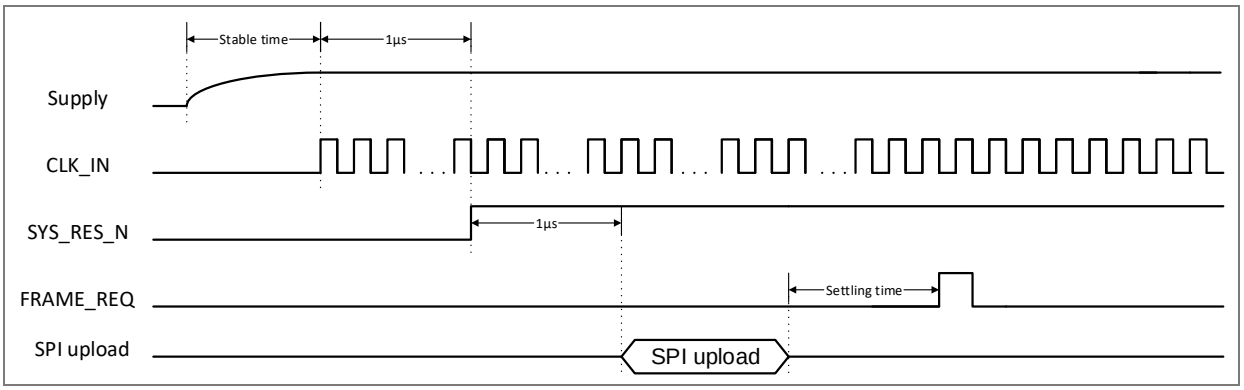
Figure 17: Start-up sequence for 480 Mbps @ 10-bit



The CLK_IN master clock (48 MHz for 480 Mbps in 10-bit mode) should only start after the rise time of the supplies. The external reset pin should be released at least 1 µs after the supplies have become stable. The first frame can be requested 1 µs after the reset pin has been released.

If the register settings need to be changed (e.g. when using 12-bit mode), this can be done through an SPI upload 1 µs after the rising edge on the SYS_RES_N pin, as described in Figure 18. In this case, the FRAME_REQ pulse must not be sent until after the SPI upload is completed, plus a settling time. This settling time is to ensure that the changes programmed in the SPI upload have taken effect before an image is captured. The main factor that determines this settling time is the change in ADC gain, because the voltage over the ramp capacitor has to settle. For typical applications, where the ADC gain is changed from the default value of 32 to a value that saturates the ADC output (40 to 45 at 48 MHz), the settling time is 5 ms. In extreme cases, when the gain is changed from default to the maximum value, the settling time will increase to 20 ms.

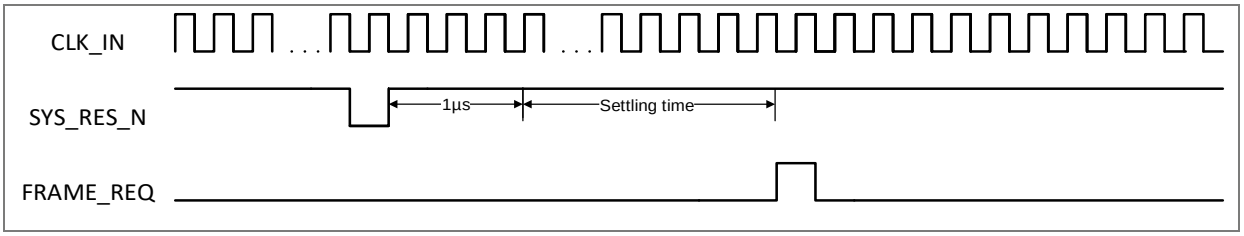
Figure 18: Start-up sequence for 12-bit mode



7.2.7 Reset sequence

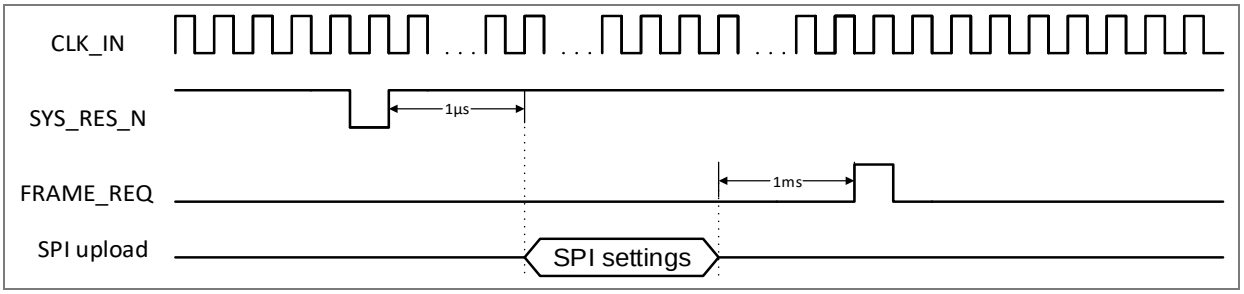
If a sensor reset is necessary while the sensor is running, the sequence in Figure 19 should be followed. The on-board sequencer will be reset and all programming registers will return to their default start-up values when a falling edge is detected on the SYS_RES_N pin. As with the start-up sequence, there is a minimum time of 1 µs plus a settling time needed before a FRAME_REQ pulse can be sent, to allow the gain settings to settle at their default value.

Figure 19: Reset sequence



When register settings are uploaded after the reset (e.g. when changing the bit mode), the sequence of Figure 20 should be followed.

Figure 20: Reset sequence when changing bit mode



7.2.8 SPI programming

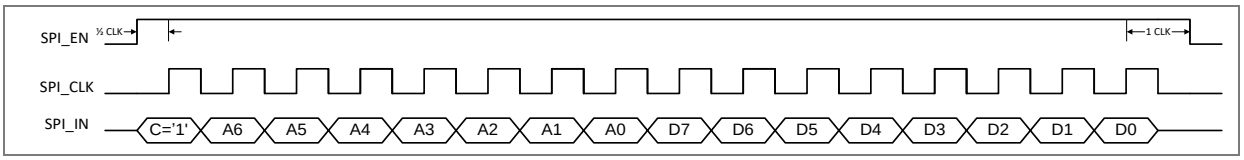
Programming the sensor is done by writing the appropriate values to the on-board registers. These registers can be written over a simple serial interface (SPI). The details of the timing and data format are described below. The data written to the programming registers can also be read out over this same SPI interface.

The details of the timing and data format are described in the following points.

7.2.8.1 SPI write

The timing to write data over the SPI interface can be found in Figure 21.

Figure 21: SPI write timing



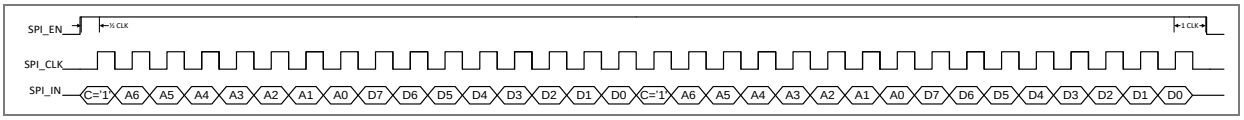
The data is sampled by the CMV2000 on the rising edge of the SPI_CLK. The SPI_CLK has a maximum frequency of 48 MHz. The SPI_EN signal has to be high for half a clock period before the first data bit is sampled. After the last data bit is sent, SPI_EN has to remain high for 1 clock period and SPI_CLK has to receive a final falling edge to complete the write operation.

One write action contains 16 bits:

- One control bit: First bit to be sent, indicates whether a read (‘0’) or write (‘1’) will occur on the SPI interface.
- 7 address bits: These bits form the address of the programming register that needs to be written. The address is sent MSB first.
- 8 data bits: These bits form the actual data that will be written in the register selected with the address bits. The MSB data is written first.

When several sensor registers need to be written, the timing above can be repeated with SPI_EN remaining high all the time. See the Figure 22 for an example of 2 registers being written in burst.

Figure 22: SPI write timing for 2 registers in burst



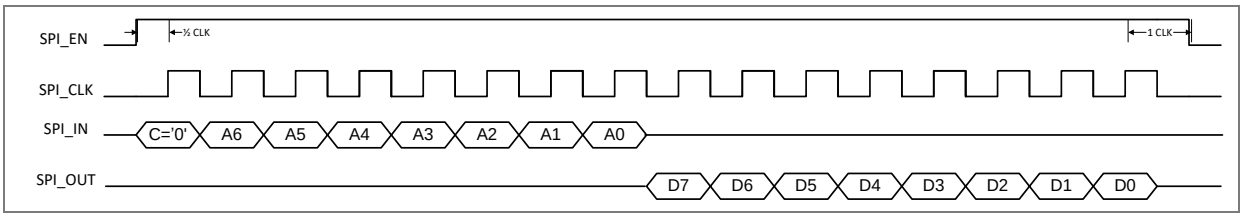
All registers should be updated during IDLE time. The sensor is not IDLE during a frame burst (between start of integration of first frame and read-out of last pixel of last frame).

Registers 35-38, 40-69, 100-103 can be updated during IDLE or FOT. Registers 1-34 and 70-71 can always be updated but it is recommended to update these during IDLE or FOT to minimize image effects. Registers 78-79 can always be updated without disrupting the imaging process.

7.2.8.2 SPI read

The timing to read data from the registers over the SPI interface can be found in Figure 23.

Figure 23: SPI read timing



To indicate a read action over the SPI interface, the control bit on the SPI_IN pin is made ‘0’. The address of the register being read out is sent immediately after this control bit (MSB first). After the LSB of the address bits, the data is launched on the SPI_OUT pin on the falling edge of the SPI_CLK. This means that the data should be sampled by the receiving system on the rising edge of the SPI_CLK. The data comes over the SPI_OUT with MSB first. When reading out the temperature sensor over the SPI, addresses 126 and 127 should de read-out in burst mode (keep SPI_EN high).

7.2.9 Requesting a frame

After starting up the sensor (see chapter 7.2.6), a number of frames can be requested by sending a FRAME_REQ pulse. The number of frames can be set by programming the appropriate register (addresses 70 and 71). The default number of frames to be grabbed is 1.

In internal-exposure-time mode, the exposure time will start after this FRAME_REQ pulse. In the external-exposure-time mode, the read-out will start after the FRAME_REQ pulse. Both modes are explained into detail in the chapters below.

7.2.9.1 Internal exposure control

In this mode, the exposure time is set by programming the appropriate registers (address 42-44).

After the high state of the FRAME_REQ pulse is detected, the exposure time will start after a delay of 133 clock cycles, see AN16 – Exposure timings for all timing details. When the exposure time ends (as programmed in the registers), the pixels are being sampled and prepared for read-out. This sequence is called the frame overhead time (FOT). Immediately after the FOT, the frame is read-out automatically. If more than one frame is requested, the exposure of the next frame starts already during the read-out of the previous one (see Figure 24).

Figure 24: Request for 2 frames in internal- exposure-time mode

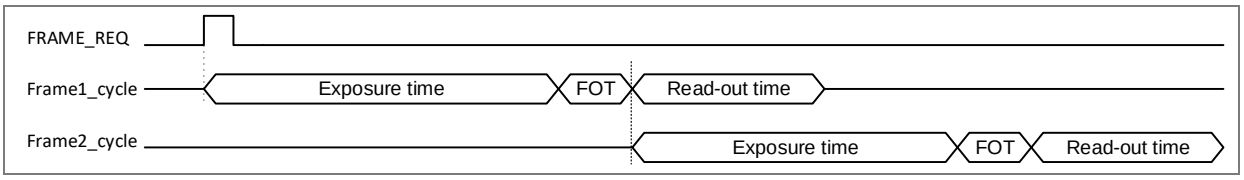
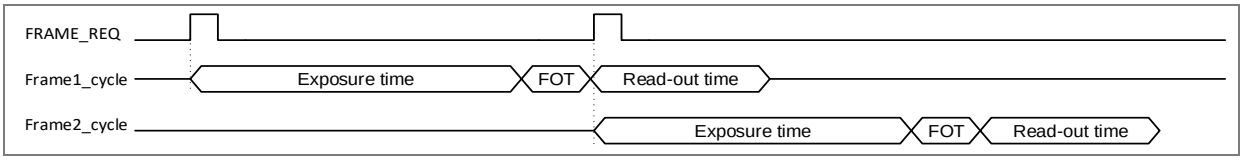


Figure 25: Two requests for 1 frame in internal exposure mode(1)



(1) This is This request form is just applicable to Version 3.

When the exposure time is shorter than the read-out time, the FOT and read-out of the next frame will start immediately after the read-out of the previous frame. Keep in mind that the next FRAME_REQ pulse has to occur after the FOT of the current frame. For an exact calculation of the exposure time, see chapter 7.4.1.

When a new FRAME_REQ is applied, the exposure of the next frame will be delayed so that the FOT begins right after the read-out time of the current frame.

Figure 26: Request for 2 frames in internal exposure mode with exposure time < read-out time

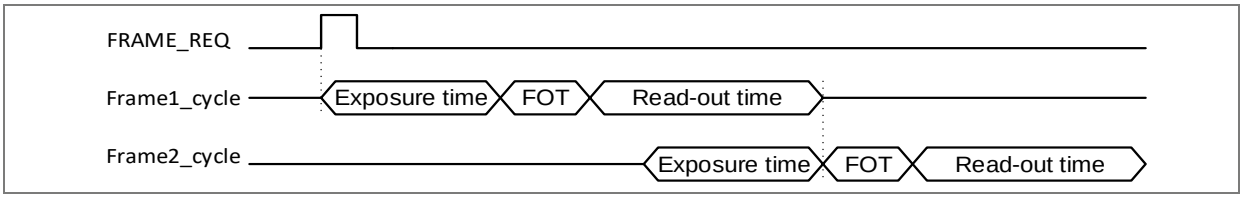
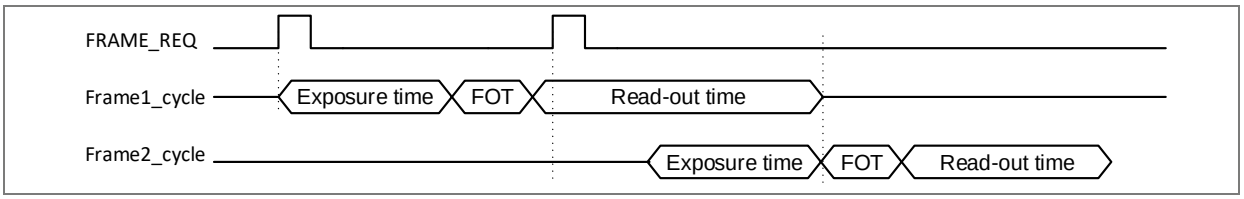


Figure 27: Two requests for 1 frame in internal exposure mode(1)



(1) Only applicable for Version 3.

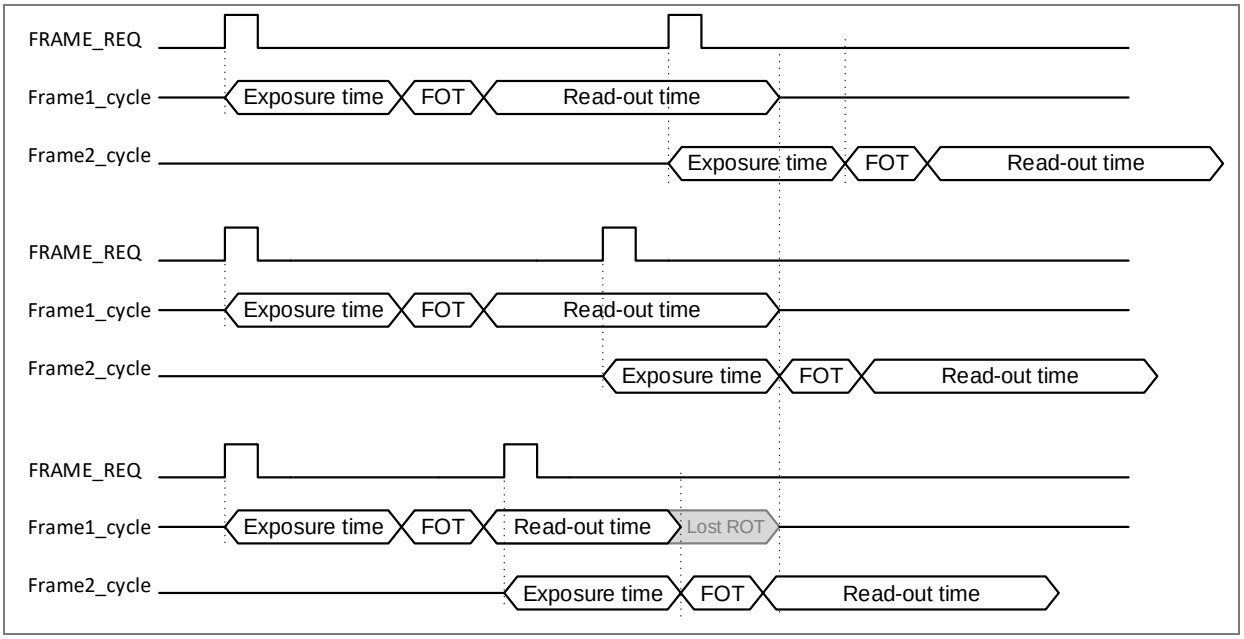
Timing calculation for version2:

If the exposure time is shorter than the read-out time, keep in mind that when you apply a next FRAME_REQ pulse during the read-out of the current frame, the exposure of that new frame will start immediately. Therefore, you have to keep enough time between the two FRAME_REQ pulses so the read-out times do not overlap. If the FOT of the next frame starts during the read-out of the current frame, that read-out will be aborted immediately, as shown in Figure 28. If the exposure time is longer than the read-out time, the read-out times of two consecutive frames cannot overlap and will not cause a problem. The minimum time between two FRAME_REQ pulses is given by Equation 3:

Equation 3:

$$min.time = exposure\ time + FOT + (Readout\ time - Exposure\ time) = FOT + Readout\ time$$

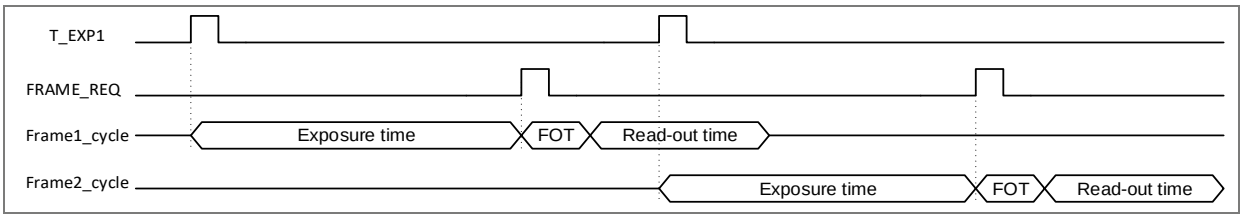
Figure 28: The timing effect of two requests for 1 frame in internal exposure mode



7.2.9.2 External exposure time

The exposure time can also be programmed externally by using the T_EXP1 input pin. This mode needs to be enabled by setting the appropriate register (address 41). In this case, the exposure starts when a high state is detected on the T_EXP1 pin. When a high state is detected on the FRAME_REQ input, the exposure time stops and the read-out will start automatically. A new exposure can start by sending a pulse to the T_EXP1 pin during or after the read-out of the previous frame. The minimum time between T_EXP1 and FRAME_REQ is 1 master clock cycle, the minimum time between FRAME_REQ and T_EXP1 pulse is FOT. For an exact calculation of the exposure time see chapter 7.4.1.

Figure 29: Request for 2 frames using external-exposure-time mode



7.3 Sensor readout format

7.3.1 LVDS data outputs

The CMV2000 has LVDS (low voltage differential signaling) outputs to transport the image data to the surrounding system. Next to 16 data channels, the sensor also has two other LVDS channels for control and synchronization of the image data. In total, the sensor has 18 LVDS output pairs (2 pins for each LVDS channel):

- 16 Data channels
- 1 Control channel
- 1 Clock channel

This means that a total of 36 pins of the CMV2000 are used for the LVDS outputs (32 for data + 2 for LVDS clock + 2 for control channel). See the pin list for the exact pin numbers of the LVDS outputs.

The 16 data channels are used to transfer the 10-bit or 12-bit pixel data from the sensor to the receiver in the surrounding system.

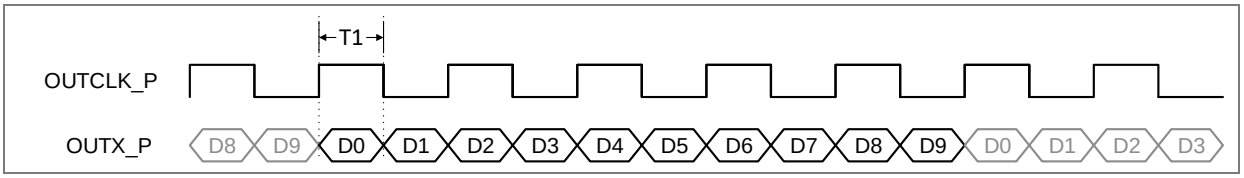
The output clock channel transports a clock, synchronous to the data on the other LVDS channels. This clock can be used at the receiving end to sample the data. This clock is a DDR clock which means that the frequency will be half of the output data rate. When 480 Mbps output data rate is used, the LVDS output clock will be 240 MHz.

The data on the control channel contains status information on the validity of the data on the data channels. Information on the control channel is grouped in 10-bit or 12-bit words that are transferred synchronous to the 16 data channels.

7.3.2 Low-level pixel timing

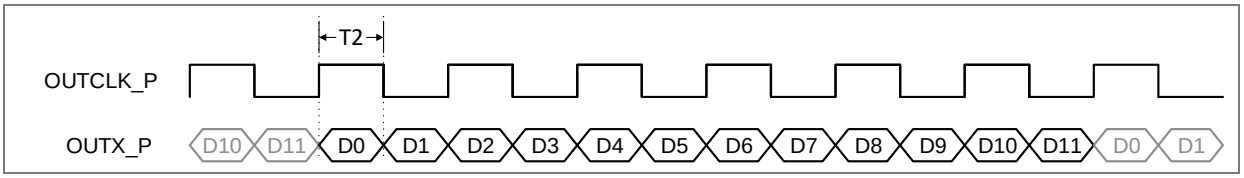
Figure 30 and Figure 31 show the timing for transfer of 10-bit and 12-bit pixel data over one LVDS output. To make the timing more clear, the figures show only the p-channel of each LVDS pair. The data is transferred to LSB first, with the transfer of bit D0 during the high phase of the DDR output clock OUTCLK.

Figure 30: 10-bit pixel data on an LVDS channel



The time ‘T1’ in Figure 30 is 1/10th of the period of the CLK_IN input clock. If a frequency of 48 MHz is used for CLK_IN (max in 10-bit mode), this results in a 240 MHz OUTCLK frequency.

Figure 31: 12-bit pixel data on an LVDS channel



The time ‘T2’ in Figure 31 is 1/12th of the period of the CLK_IN input clock. If a frequency of 40 MHz is used for CLK_IN (max in 12-bit mode), this results in a 240 MHz OUTCLK frequency.

7.3.3 Read-out timing

The read-out of image data is grouped in bursts of 128 pixels per channel. Each pixel is either 10 or 12 bits of data (see Chapter 7.3.2). One complete pixel period equals one period of the input clock CLK_IN. For details on pixel remapping and pixel vs. channel location please see chapter 7.3.4 of this document. An overhead time exists between two bursts of 128 pixels. This overhead time has the same length of one pixel read-out (i.e. the length of 10 or 12 bits at the selected data rate or one CLK_IN period). For details on how to program the sequencer for different output modes, see chapter 7.5.1.

7.3.3.1 10-bit mode

In this section, the read-out timing for the default 10-bit mode is explained. In this mode the maximum frame rate of 340 fps can be reached.

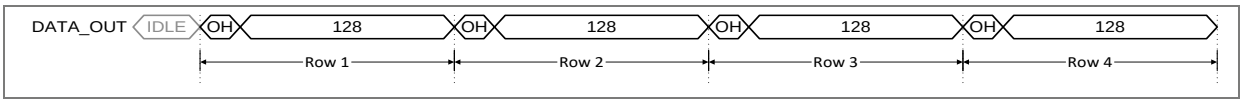
For simplification, the timing for only one LVDS channel is shown in every case in the following paragraphs:

- 16 Output Channels
- 8 Output Channels
- 4 Output Channels
- 2 Output Channels

16 output channels:

By default, all 16 data output channels are used to transmit the image data. This means that an entire row of image data is transferred in one slot of 128 pixel periods (16 x 128 = 2048). This results in a maximum frame rate of 340 fps.

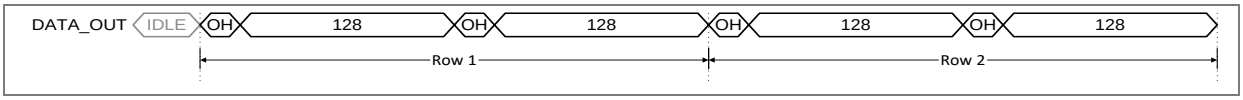
Figure 32: Output timing in default 16 channels mode



8 output channels:

When only 8 LVDS output channels are used, the read-out of one row takes (2*128) + (2*1) CLK_IN periods. The maximum frame rate is reduced with a factor of 2 compared to 16 channels mode.

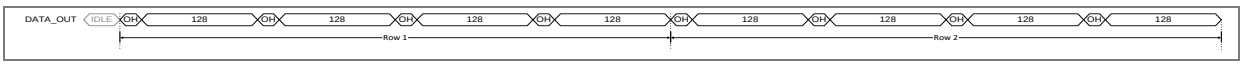
Figure 33: Output timing in 8 channels mode



4 output channels:

When only 4 LVDS output channels are used, the read-out of one row takes (4*128) + (4*1) CLK_IN periods. The maximum frame rate is reduce with a factor of 4 compared to 16 channels mode.

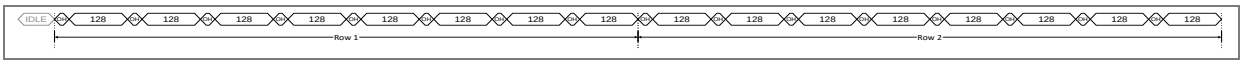
Figure 34: Output timing in 4 channels mode



2 output channels:

When only 2 LVDS output channels are used, the read-out of one row takes (8*128) + (8*1) CLK_IN periods. The maximum frame rate is reduced with a factor of 8 compared to 16 channels mode.

Figure 35: Output timing in 2 channels mode



7.3.3.2 12-bit mode

In 12-bit mode, the analog-to-digital conversion takes 4x longer to complete. This causes the frame rate to drop to 70 fps when 480 MHz is used for LVDS_CLK_N/P. Due to this extra conversion time, the sensor automatically multiplexes to 4 outputs when 12-bit is used. To simplify the figures below, the timing for only one LVDS channel is shown in every case.

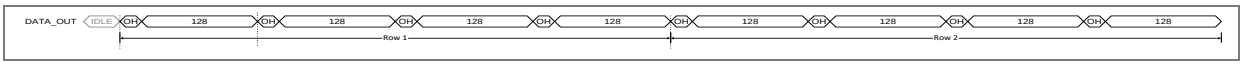
For simplification, the timing for only one LVDS channel is shown in every case in the following paragraphs:

- 4 Output Channels
- 2 Output Channels

4 output channels:

By default, the CMV2000 uses only 4 LVDS output channels in 12-bit mode. This means that the read-out of one row takes (4*128) + (4*1) CLK_IN periods.

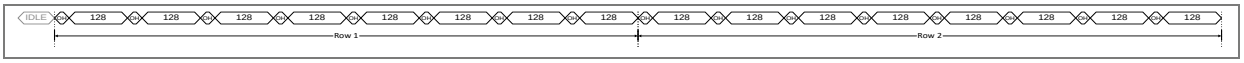
Figure 36: Output timing in 4 channels mode



2 output channels:

When only 2 LVDS output channels are used, the read-out of one row takes (8*128) + (8*1) CLK_IN periods. The maximum frame rate is reduced with a factor of 2 compared to 4 channels mode.

Figure 37: Output timing in 2 channels mode



7.3.4 Pixel remapping

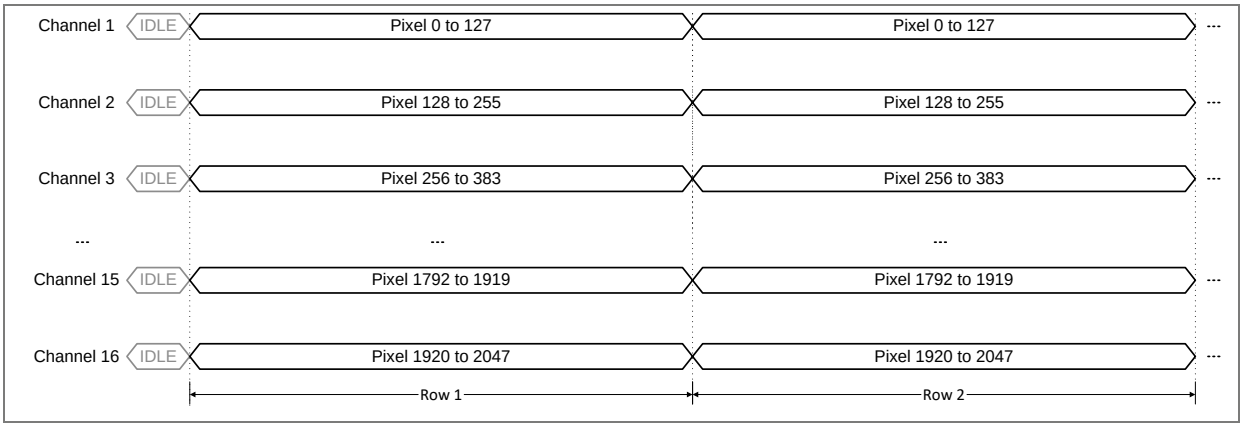
Depending on the number of output channels, the pixels are read out by different channels and come out at a different moment in time. With the details from the next chapters, the end user is able to remap the pixel values at the output to their correct image array location.

7.3.4.1 16 outputs

Figure 38 shows the location of the image pixels versus the output channel of the image sensor.

16 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in one burst. The amount of rows that will be read out depends on the value in the corresponding register. By default, there are 1088 rows being read out.

Figure 38: Pixel remapping for 16 output channels

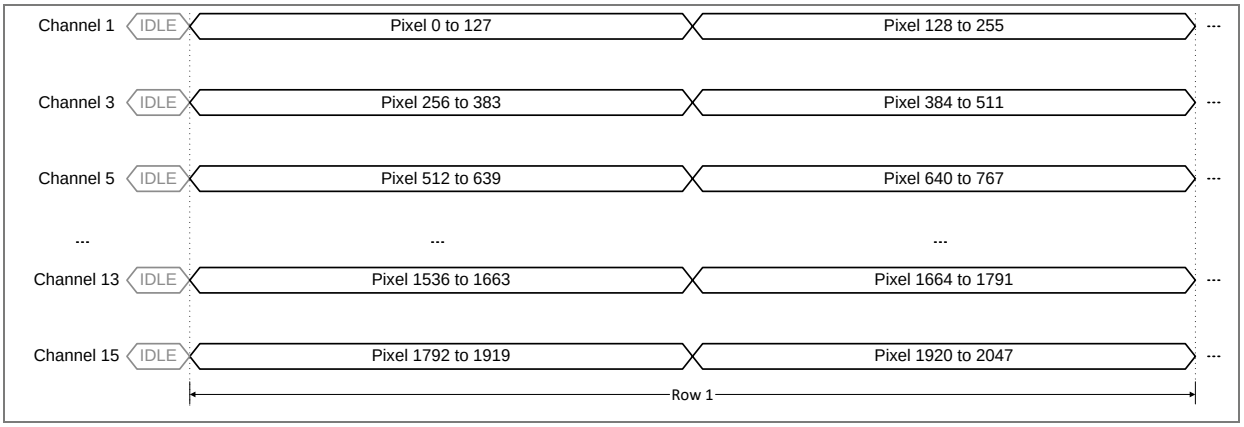


7.3.4.2 8 outputs

When only 8 outputs are used, the pixel data is placed on the outputs as detailed in Figure 39. 8 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in two bursts. The time needed to read out one row is doubled compared to when 16 outputs are used. Channel 2, 4, 6…16 are not being used in this mode, so they can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out can be set in the register. By default, 1088 rows are read out.

Figure 39: Pixel remapping for 8 output channels

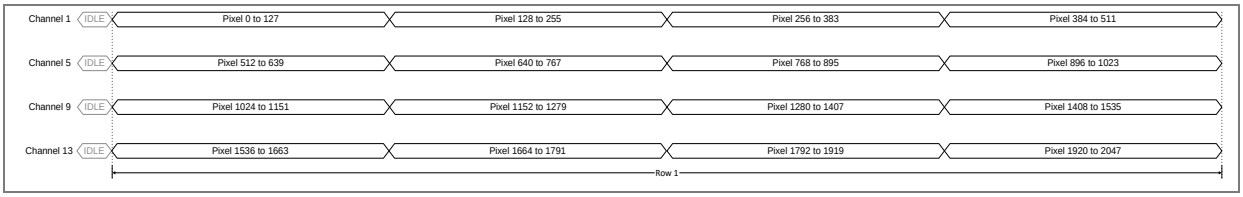


7.3.4.3 4 outputs

When only 4 outputs are used, the pixel data is placed on the outputs as detailed Figure 40. 4 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in four bursts. The time needed to read out one row is 4x longer compared to when 16 outputs are used. Only channel 1, 5, 9 and 13 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out can be set in the register. By default there are 1088 rows being read out.

Figure 40: Pixel remapping for 4 output channels



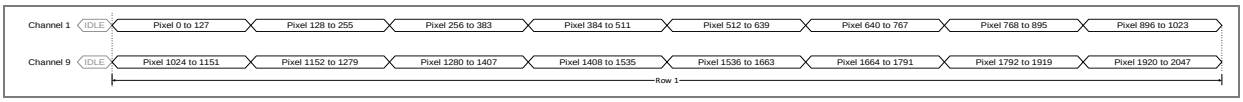
7.3.4.4 2 outputs

When only 2 outputs are used, the pixel data is placed on the outputs as detailed in Figure 41.

2 bursts of 128 pixels happen in parallel on the data outputs. This means that one complete row is read out in 8 bursts. The time needed to read out one row is 8x longer compared to when 16 outputs are used. Only channels 1 and 9 are being used in this mode, so the remaining channels can be turned off by setting the correct bits in the register with addresses 80-82. Turning off these channels will reduce the power consumption of the chip.

The amount of rows that will be read out can be set in the register. By default 1088 rows are read out.

Figure 41: Pixel remapping for 2 output channels



7.3.4.5 Overview

All outputs are always used to send data, but if you use less than 16 channels, some channels will have duplicate data. For example, if you multiplex to 4 channels, outputs 6, 7 and 8 will have identical data as output 5.

Table 8 shows an overview of which channel data is on which output at a certain output mode.

Table 8: Overview channel data – output mode

MUX to	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	OUT 6	OUT 7	OUT 8	OUT 9	OUT 10	OUT 11	OUT 12	OUT 13	OUT 14	OUT 15	OUT 16
16	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16
8	CH1	CH1	CH3	CH3	CH5	CH5	CH7	CH7	CH9	CH9	CH11	CH11	CH13	CH13	CH15	CH15
4	CH1	CH1	CH1	CH1	CH5	CH5	CH5	CH5	CH9	CH9	CH9	CH9	CH13	CH13	CH13	CH13
2	CH1	CH1	CH1	CH1	CH1	CH1	CH1	CH1	CH9	CH9	CH9	CH9	CH9	CH9	CH9	CH9

7.3.5 Control channel

The CMV2000 has one LVDS output channel dedicated for the valid data synchronization and timing of the output channels. The end user must use this channel to know when valid image data or training data is available on the data output channels.

The control channel transfers status information in 10-bit or 12-bit word format. Every bit of the word has a specific function. Next table describes the function of the individual bits, but only the DVAL, LVAL and FVAL signal are necessary to know when to sample the image data.

Table 9: Function of the individual bits

Bit	Function	Description
[0]	DVAL	Indicates valid pixel data on the outputs
[1]	LVAL	Indicates validity of the read-out of a row
[2]	FVAL	Indicates the validity of the read-out of a frame
[3]	SLOT	Indicates the overhead period before 128-pixel bursts (*)
[4]	ROW	Indicates the overhead period before the read-out of a row(1)
[5]	FOT	Indicates when the sensor is in FOT (sampling of image data in pixels)(1)
[6]	INTE1	Indicates when pixels of integration block 1 are integrating(1)
[7]	INTE2	Indicates when pixels of integration block 2 are integrating(1)
[8]	‘0’	Constant zero
[9]	‘1’	Constant one

Bit	Function	Description
[10]	‘0’	Constant zero
[11]	‘0’	Constant zero

(1) The status bits are purely informational. These bits are not required to know when the data is valid. The DVAL, LVAL and FVAL signals are sufficient to know when to sample the image data.

INTE1/2 will be low when FOT is high, so the exposure during the small 0.43*reg73 overlap (see formulas in 7.4.1), will not be visible in the INTE1/2 bits.

Pins H2 (TDIG1) and G2 (TDIG2) can be programmed to map the state of control channel bits [0] (DVAL), [1] (LVAL), [2] (FVAL), [6] (INTE1) or [7] (INTE2) with registers 108 (T_dig1) and 109 (T_dig2).

Table 10: Register 108/109 value

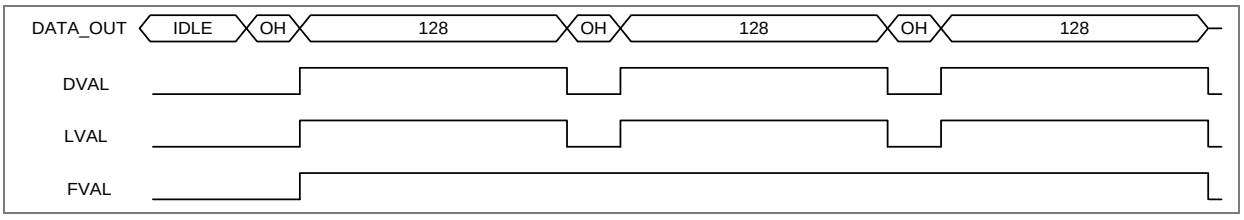
Register 108/109 value	TDIG1	TDIG2
0	INTE1	INTE1
1	INTE2	INTE2
2	DVAL	DVAL
3	LVAL	LVAL
4	FVAL	FVAL

7.3.5.1 DVAL, LVAL, FVAL

The first three bits of the control word must be used to identify valid data and the read-out status.

Figure 42 shows the timing of the DVAL, LVAL and FVAL bits of the control channel with an example of the read-out of a frame of 3 rows (default is 1088 rows). This example uses the default mode of 16 outputs in 10-bit mode.

Figure 42: DVAL, LVAL and FVAL timing in 16 outputs mode



When only 8 outputs are used, the line read-out time is 2x longer. The control channel takes this into account and the timing in this mode are shown in Figure 43 and Figure 44. The timing extrapolates identically for 4 and 2 outputs.

Figure 43: DVAL, LVAL and FVAL timing in 8 outputs mode

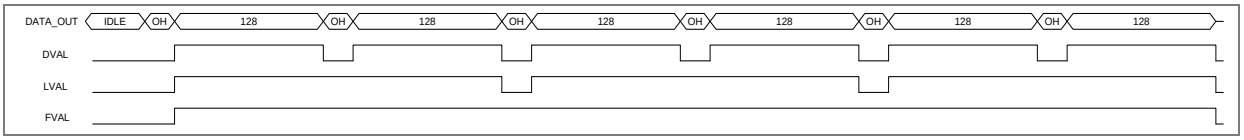
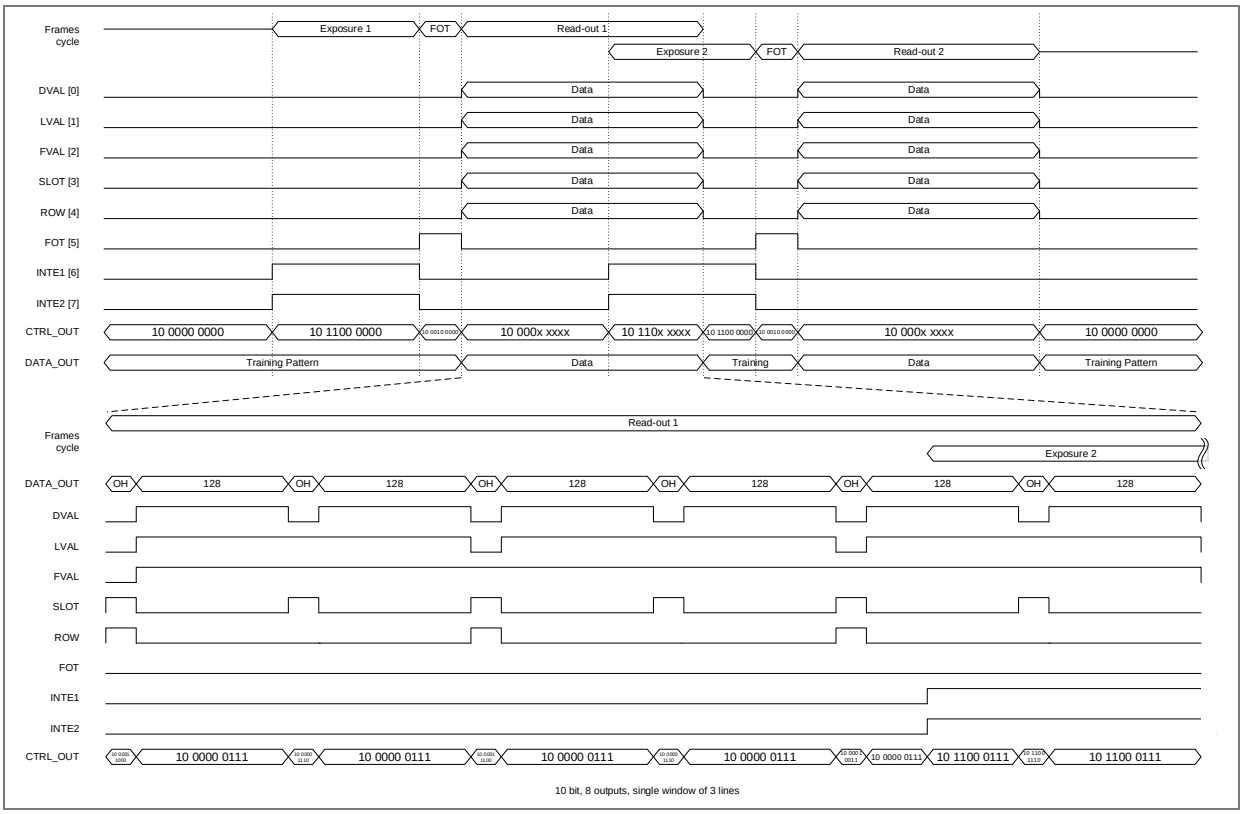


Figure 44: Detailed timings of the control channel (8 outputs, 3 lines window)



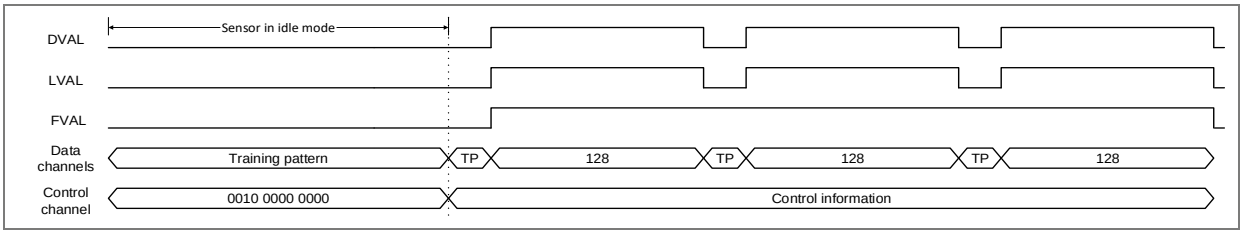
7.3.6 Training data

To synchronize the receiving side with the LVDS outputs of the CMV2000, a known data pattern can be put on the output channels. This pattern “trains” the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. This training pattern is put on all 16 output channels when no valid image data is being sent, even in between bursts of 128 pixels. The training pattern is a 10-bit or 12-bit word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 78-79) that can be used to change the contents of the 12-bit training pattern.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9] (= 0010 0000 0000 or 512 decimal).

Figure 45 shows the location of the training pattern (TP) on the data channels when the sensor is idle and when reading out 3 rows. The default mode of 16 outputs is selected.

Figure 45: Training pattern location in the data and control channels



7.4 Configuring exposure and readout

This section explains how the CMV2000 can be programmed using the on-board sequencer registers.

7.4.1 Exposure modes

The exposure time can be programmed in two ways, externally or internally. Externally, the exposure time is defined as the time between the rising edge of T_EXP1 and the rising edge of FRAME_REQ (see External exposure time for more details). Internally, the exposure time is set by uploading the desired value to the corresponding sequencer register.

Table 11: Time settings of exposure mode

Register name	Register address	Default value	Description of the value
Exp_ext	41[0]	0	0: Value in Exp_time register defines exposure time 1: Time between T_EXP1 and FRAME_REQ pulses defines exposure time
Exp_time	42[7:0] 43[7:0] 44[7:0]	2048	If Exp_ext = 0: Defines the exposure time according to the following formula: $129 * clk\_per(0.43 * fot\_length + Exp\_time)$ Where clk_per is the period of the master input clock and fot_length is the value in register 73. If Exp_ext = 1: The exposure time is: $129 * clk\_per(0.43 * fot\_length) + external\ exposure\ time$ Where external exposure time is the time between T_EXP1 and FRAME_REQ.

To calculate back from actual exposure time to the register value for internal exposure can use the following formula (exposure time and clk_per should have the same time unit):

$$Exp\_time = \frac{exposure\ time}{129 * clk\_per} - 0.43 * fot\_length$$

For very short integration times, the fot_length should be lowered to 5 and the maximum clock speed should be used. In internal exposure mode, the shortest exposure time is limited by the exp_time register, when this is set to 1, the shortest exposure time is 14.24 µs, or 8.47 µs for fot_length = 5.

In external exposure mode, the time between T_EXP1 and FRAME_REQ can be as short as one clock cycle, reducing the shortest exposure time even more to 11.58 µs, or 5.80 µs for fot_length = 5.

7.4.2 High dynamic range modes

The sensor has different ways to achieve high optical dynamic range in the grabbed image.

- Interleaved read-out: the odd and even rows have a different exposure time.
- Piecewise linear response: pixels respond to light with a piecewise linear response curve.
- Multi-frame read-out: Different frames are read-out with increasing exposure time.

All the HDR modes mentioned above can be used in both the internal and external exposure time mode.

7.4.2.1 Interleaved read-out

In this HDR mode, the odd and even rows of the image sensors will have a different exposure time. This mode can be enabled by setting the register Exp_dual.

Table 12: Interleaved read-out – HDR mode enabling

Register name	Register address	Default value	Description of the value
Exp_dual	41[1]	0	0: Interleaved exposure mode disabled 1: Interleaved exposure mode enabled

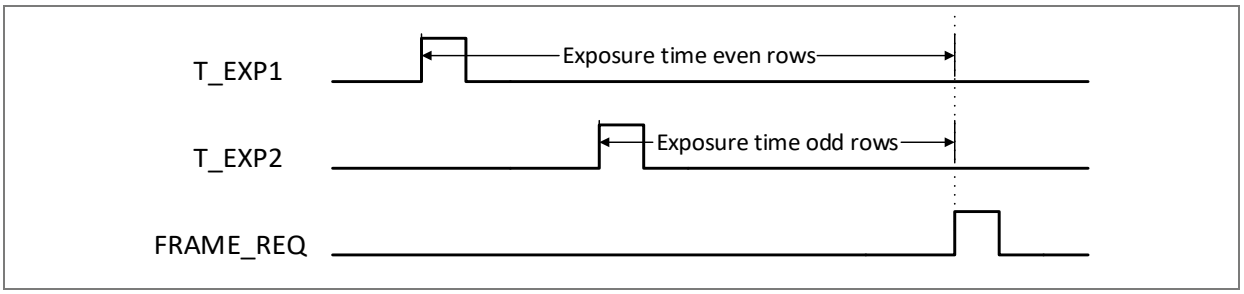
The surrounding system can combine the image of the odd rows with the image of the even rows which results in a high dynamic range image. In this image, very bright and very dark objects are made visible without clipping. The Table 13 gives an overview of the registers involved in the interleaved read-out when the internal exposure mode is selected.

Table 13: Interleaved read-out – HDR mode timing

Register name	Register address	Default value	Description of the value
Exp_time	42[7:0] 43[7:0] 44[7:0]	1088	If Exp_dual = '1' Defines the exposure time for the even rows according following formula: $129 * clk\_per(0.43 * fot\_length + Exp\_time)$ Where clk_per is the period of the CLK_IN input clock.
Exp_time2	56[7:0] 57[7:0] 58[7:0]	1088	If Exp_dual = '1' Defines the exposure time for the odd rows according following formula: $129 * clk\_per(0.43 * fot\_length + Exp\_time2)$ Where clk_per is the period of the CLK_IN input clock.

When the external exposure mode and interleaved read-out are selected, the different exposure times are achieved by using the T_EXP1 and T_EXP2 input pins. T_EXP1 defines the exposure time for the even lines, while T_EXP2 defines the exposure time for the odd lines. See Figure 46 for more details.

Figure 46: Interleaved read-out in external exposure mode



When a color sensor is used, the sequencer should be programmed to make sure it takes the Bayer pattern into account when doing interleaved read-out. This can be done by setting the appropriate register to '0'.

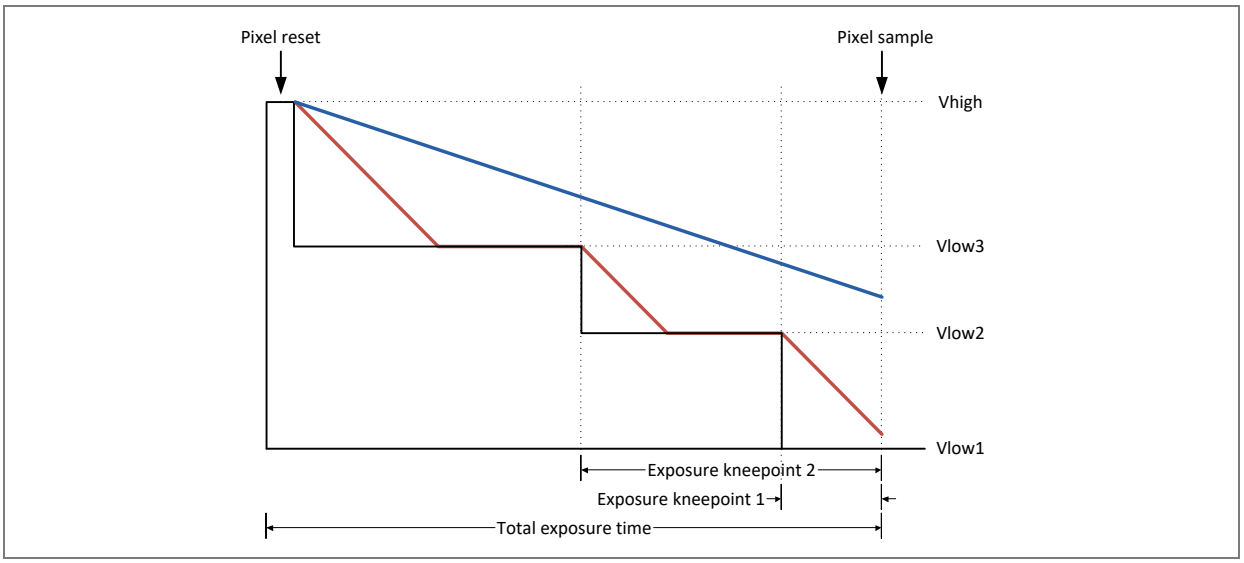
Table 14: Mono or color register selection

Register name	Register address	Default value	Description of the value
mono	39[0]	1	0: Color sensor is used 1: Monochrome sensor is used

7.4.2.2 Piecewise linear response

The CMV2000 has the possibility to achieve a high optical dynamic range by using a piecewise linear response. This will clip illuminated pixels which reach a programmable voltage, while leaving the darker pixels untouched. The clipping level can be adjusted 2 times within one exposure time to achieve a maximum of 3 slopes in the response curve, as shown in Figure 47.

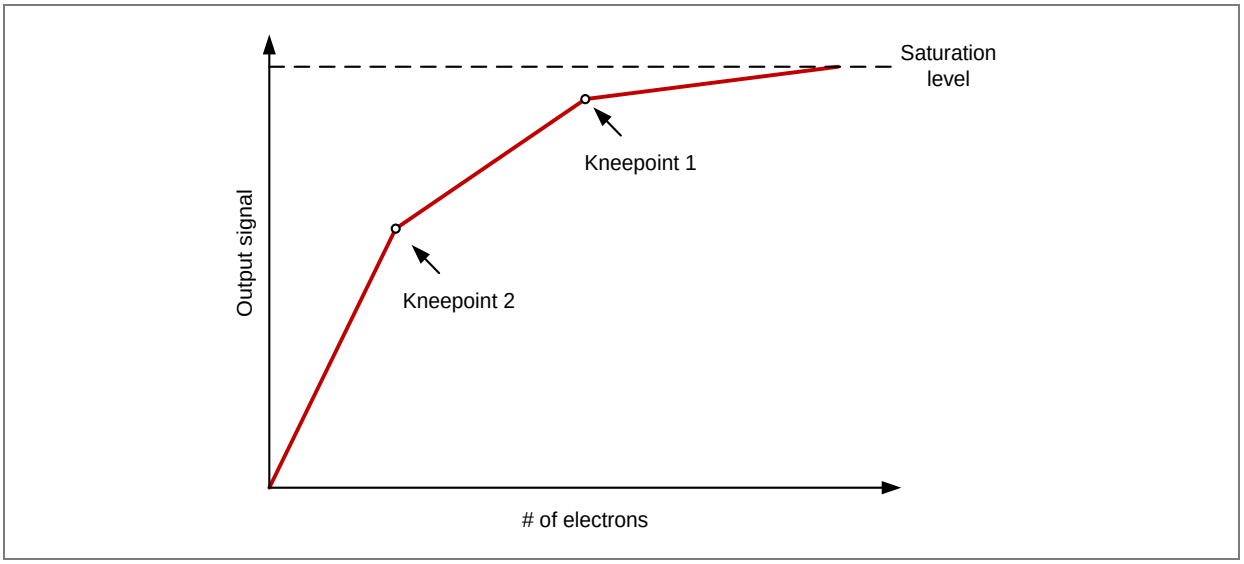
Figure 47: Piecewise linear response details



In Figure 47, the red lines represent a pixel on which a large amount of light is falling. The blue line represents a pixel on which less light is falling. The bright pixel is held to a programmable voltage for a programmable time during the exposure time. This happens two times to make sure that at the end of the exposure time the pixel is not saturated. The darker pixel is not influenced and will have a normal response. The Vlow voltages and different exposure times are programmable using the sequencer registers. Using this feature, a response as detailed in Figure 48 can be achieved.

The placement of the knee points on the X-axis is controlled by the Vlow programming, while the slope of the segments is controlled by the programmed exposure times.

Figure 48: Piecewise linear response



Piecewise linear response with INTERNAL exposure mode:

The following registers need to be programmed when a piecewise linear response in internal exposure mode is desired.

Table 15: Piecewise linear response with internal exposure mode register settings

Register name	Register address	Default value	Description of the value
Exp_time	42[7:0] 43[7:0] 44[7:0]	1088	Defines the total exposure time according following formula: $129 * clk\_per(0.43 * fot\_length + Exp\_time)$ Where clk_per is the period of the CLK_IN input clock.
Nr_slopes	54[1:0]	1	Defines the number of slopes (min=1, max=3).
Exp_kp1	48[7:0] 49[7:0] 50[7:0]	1	Defines the exposure time of kneepoint 1. Formula: $129 * clk\_per(0.43 * fot\_length + Exp\_kp1)$ Where clk_per is the period of the CLK_IN input clock.

Register name	Register address	Default value	Description of the value
Exp_kp2	51[7:0] 52[7:0] 53[7:0]	1	Defines the exposure time of kneepoint 2. Formula: $129 * clk\_per(0.43 * fot\_length + Exp\_kp2)$ Where clk_per is the period of the CLK_IN input clock.
Vlow3	90[6:0]	96	Defines the Vlow3 voltage (DAC setting). Bit [6] = Enable Bit[5:0] = Vlow3 value
Vlow2	89[6:0]	96	Defines the Vlow2 voltage (DAC setting). Bit [6] = Enable Bit[5:0] = Vlow2 value

Piecewise linear response with EXTERNAL exposure mode:

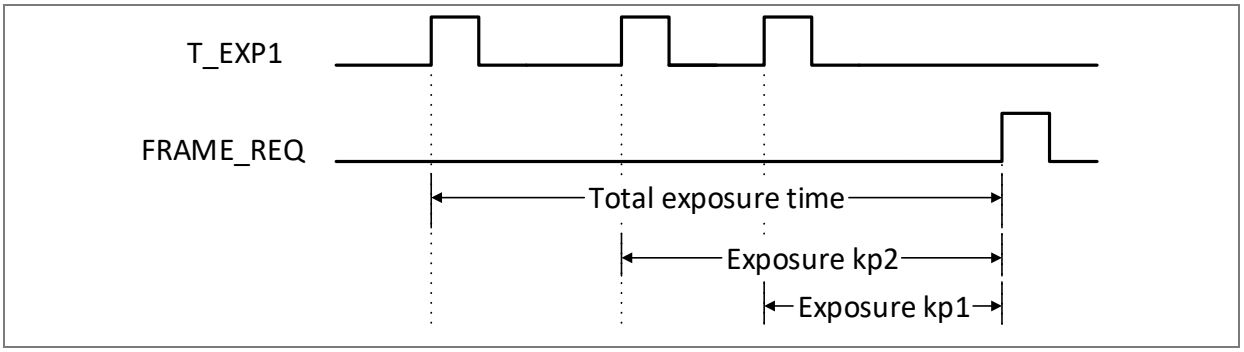
When external exposure time is used and a piecewise linear response is desired, the following registers should be programmed. Note that the combination of the piecewise linear response and interleaved read-out is not possible.

Table 16: Piecewise linear response with external exposure mode register settings

Register name	Register address	Default value	Description of the value
Nr_slopes	54[1:0]	1	Defines the number of slopes (min=1, max=3).
Vlow3	90[6:0]	96	Defines the Vlow3 voltage (DAC setting).
Vlow2	89[6:0]	96	Defines the Vlow2 voltage (DAC setting).

The timing that needs to be applied in this external exposure mode looks like the one shown in Figure 49.

Figure 49: Timing of external exposure mode



7.4.2.3 Multi-frame read-out

The sensor has the possibility to read-out multiple frames with increasing exposure time for each frame. The exposure time step and number of frames can be programmed using the appropriate registers. The frames grabbed in this mode, can be combined to create one high dynamic range image. This combination needs to be made by the receiving system.

The following registers should be used when this multi-frame read-out is selected. This mode only works with internal exposure time setting.

Table 17: Multi-frame read-out mode register settings

Register name	Register address	Default value	Description of the value
Exp_time	42[7:0] 43[7:0] 44[7:0]	1088	Defines the exposure time of the first frame in the sequence. Formula: $129 * clk\_per(0.43 * fot\_length + Exp\_time)$ Where clk_per is the period of the CLK_IN input clock.
Exp_step	45[7:0] 46[7:0] 47[7:0]	0	Defines the step size for the increasing exposure times in multi-frame read-out. This value will be added to Exp_time per frame. So the exposure time for the n^{th} frame is: $129 * clk\_per(0.43 * fot\_length + Exp\_time + (n-1) * Exp\_step)$ Where clk_per is the period of the CLK_IN input clock and n is the n^{th} frame.
Exp_seq	55[7:0]	1	Defines the number of frames to be read-out in multi-frame mode (min = 1, max = 255).

7.4.3 Windowing

To limit the amount of data or to increase the frame rate of the sensor, windowing in Y direction is possible. The number of lines and start address can be set by programming the appropriate registers. The CMV2000 has the possibility to read-out multiple (max=8) predefined sub windows in one read-out cycle. The default mode is to read-out one window with the full frame size (2048x1088).

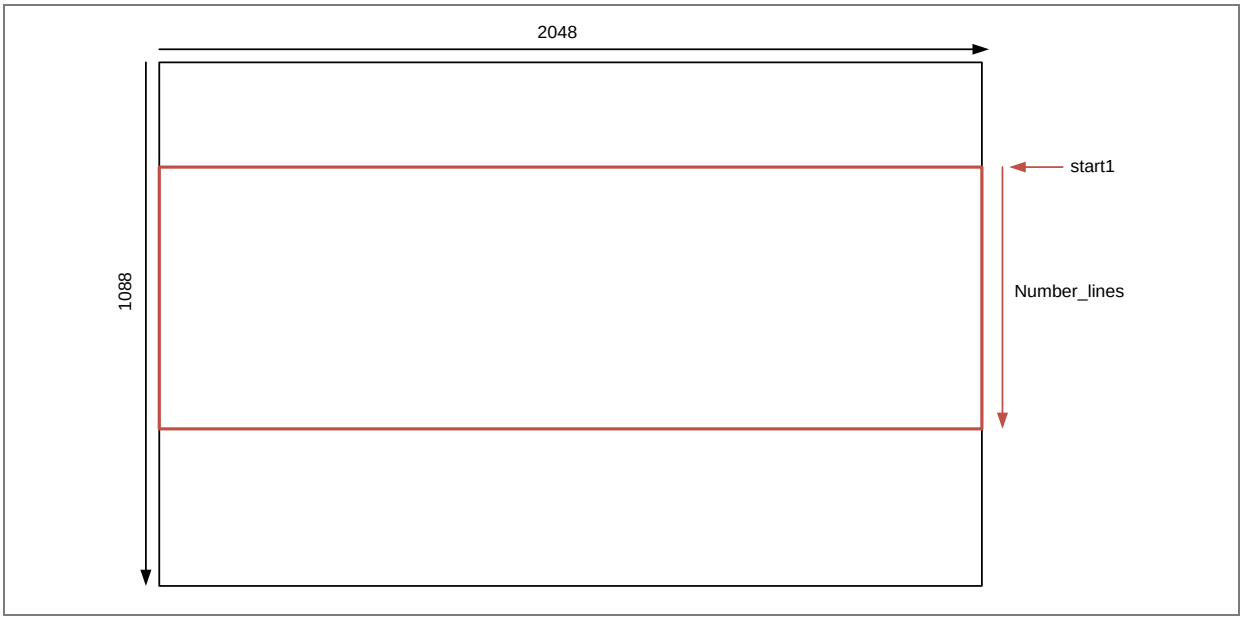
7.4.3.1 Single window

When a single window is read out, the start address and size can be uploaded in the corresponding registers. The default start address is 0 and the default size is 1088 (full frame), like shown in Table 18 and Figure 50.

Table 18: Single window register settings

Register name	Register address	Default value	Description if the value
start1	3[7:0] 4[7:0]	0	Defines the start address of the window in Y (min=0, max=1087)
Number_lines	1[7:0] 2[7:0]	1088	Defines the number of lines read-out by the sensor (min=1, max=1088)

Figure 50: Window structure



7.4.3.2 Multiple window

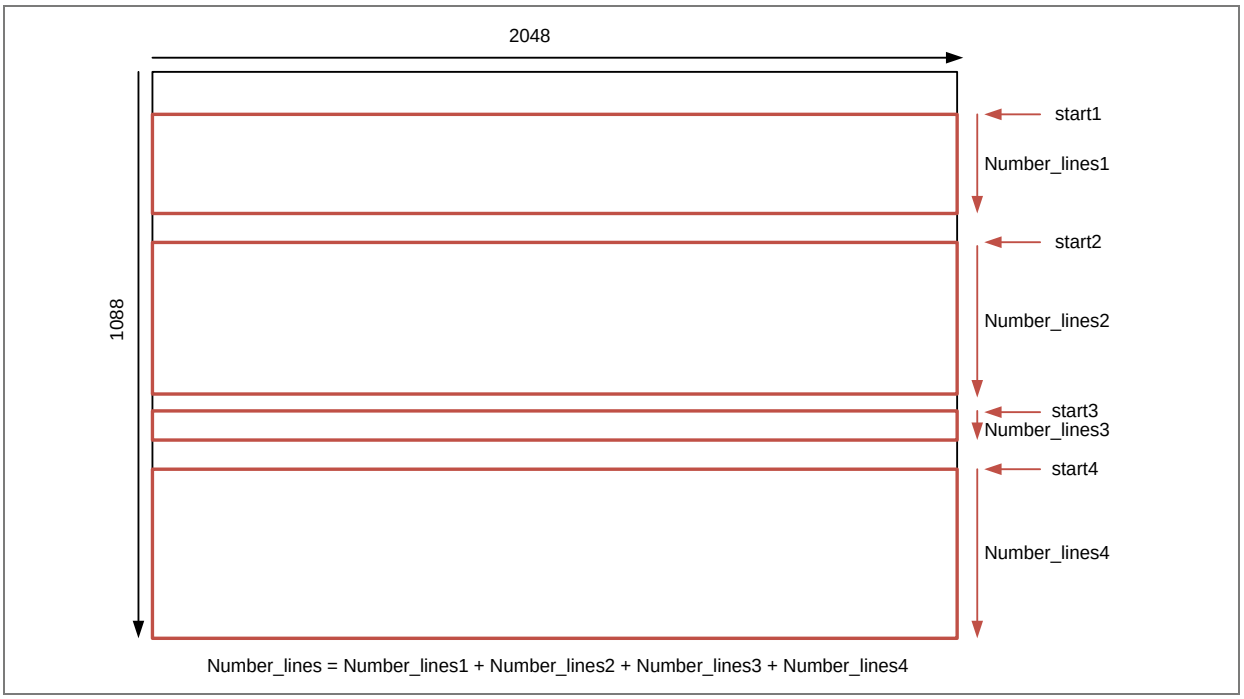
The CMV2000 can read out a maximum of 8 different sub windows in one read-out cycle. The location and length of these sub windows must be programmed in the correct registers. The total number of lines to be read-out (sum of all windows) needs to be specified in the Number_lines register. The registers which need to be programmed for the multiple windows can be found in Table 19. The default values will result in one window with 1088 lines to be read out.

Table 19: Multiple window register settings

Register name	Register address	Default value	Description of the value
Number_lines	1[7:0] 2[7:0]	1088	Defines the total number of lines read-out by the sensor (min=1, max=1088)
start1	3[7:0] 4[7:0]	0	Defines the start address of the first window in Y (min=0, max=1087)
Number_lines1	19[7:0] 20[7:0]	0	Defines the number of lines of the first window (min=1, max=1088)
start2	5[7:0] 6[7:0]	0	Defines the start address of the second window in Y (min=0, max=1087)
Number_lines2	21[7:0] 22[7:0]	0	Defines the number of lines of the second window (min=1, max=1088)
start3	7[7:0] 8[7:0]	0	Defines the start address of the third window in Y (min=0, max=1087)
Number_lines3	23[7:0] 24[7:0]	0	Defines the number of lines of the third window (min=1, max=1088)
start4	9[7:0] 10[7:0]	0	Defines the start address of the fourth window in Y (min=0, max=1087)
Number_lines4	25[7:0] 26[7:0]	0	Defines the number of lines of the fourth window (min=1, max=1088)
start5	11[7:0] 12[7:0]	0	Defines the start address of the fifth window in Y (min=0, max=1087)
Number_lines5	27[7:0] 28[7:0]	0	Defines the number of lines of the fifth window (min=1, max=1088)
start6	13[7:0] 14[7:0]	0	Defines the start address of the sixth window in Y (min=0, max=1088)
Number_lines6	29[7:0] 30[7:0]	0	Defines the number of lines of the sixth window (min=1, max=1088)
start7	15[7:0] 16[7:0]	0	Defines the start address of the seventh window in Y (min=0, max=1087)
Number_lines7	31[7:0] 32[7:0]	0	Defines the number of lines of the seventh window (min=1, max=1088)
start8	17[7:0] 18[7:0]	0	Defines the start address of the eighth window in Y (min=0, max=1087)

Register name	Register address	Default value	Description of the value
Number_lines8	33[7:0] 34[7:0]	0	Defines the number of lines of the eighth window (min=1, max=1088)

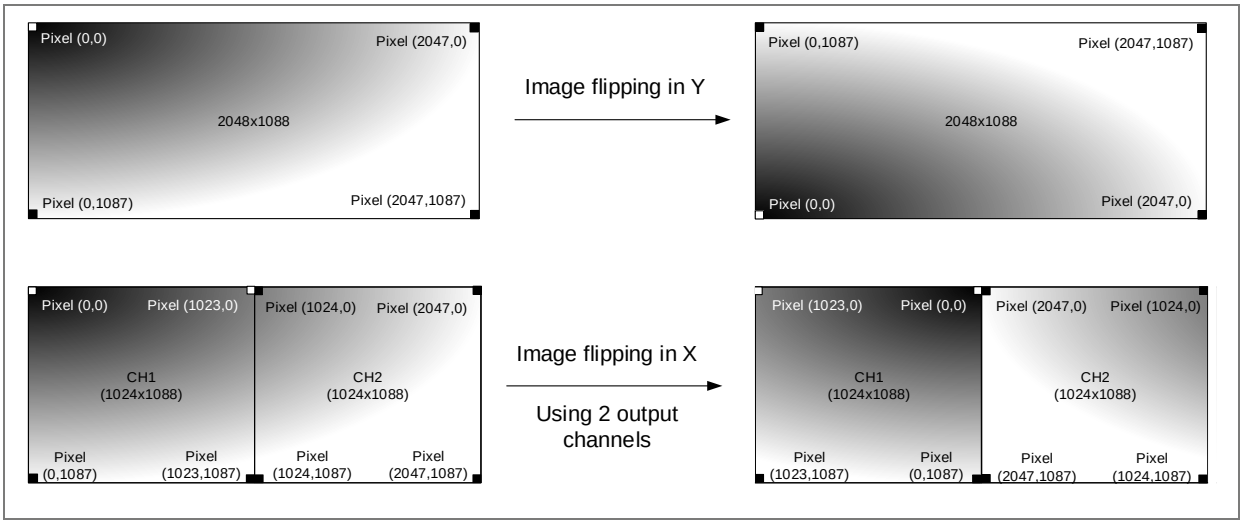
Figure 51: Example of 4 multiple frames read-out



7.4.4 Image flipping

The image coming out of the image sensor can be flipped in X (per channel) and/or Y direction. When no flipping is enabled, the pixel in the upper left corner of the screen - (pixel (0,0) - is read out first. When flipping in Y is enabled, the bottom left pixel (0,1087) is read out first instead of the top left pixel (0,0). When flipping in X is enabled, only the pixels within a channel are mirrored, not the channels themselves. Therefore, the first row in channel 1 to be read out is pixel (1023,0) to pixel (0,0). In channel 2, this is pixel (2047,0) to pixel (1024,0).

Figure 52: Image flipping



The following registers are involved in image flipping:

Table 20: Image flipping register settings

Register name	Register address	Default value	Description of the value
Image_flipping	40[1:0]	0	0: No image flipping 1: Image flipping in X 2: Image flipping in Y 3: Image flipping in X and Y

7.4.5 Image subsampling

To maintain the same field of view but reduce the amount of data coming out of the sensor, a subsampling mode is implemented on the chip. Different subsampling schemes can be programmed by setting the appropriate registers. These subsampling schemes can take into account whether a color or monochrome sensor is used to preserve the Bayer pattern information. A distinction is made between a simple and advanced mode (can be used for color devices). Subsampling can be enabled in every windowing mode.

The following paragraphs describe the registers involved in subsampling in detail.

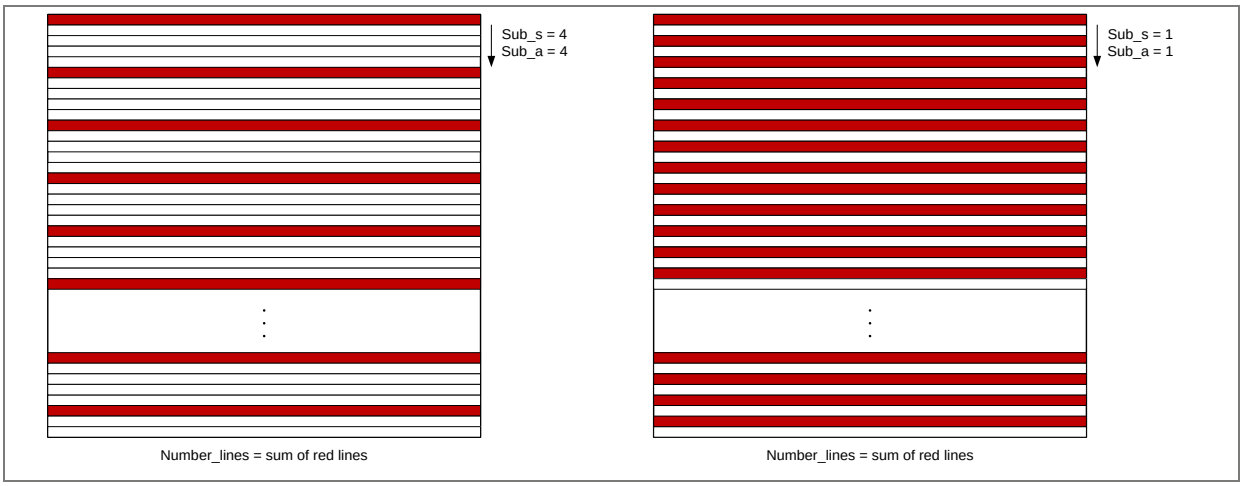
7.4.5.1 Simple subsampling

Table 21: Simple subsampling register settings

Register name	Register address	Default value	Description of the value
Number_lines	1[7:0] 2[7:0]	1088	Defines the total number of lines read-out by the sensor (min=1, max=1088)
Sub_s	35[7:0] 36[7:0]	0	Number of rows to skip (min=0, max=1086)
Sub_a	37[7:0] 38[7:0]	0	Identical to Sub_s

Figure 53 shows two subsampling examples (skip 4x and skip 1x).

Figure 53: Subsampling examples (skip 4x and skip 1x)



7.4.5.2 Advanced subsampling

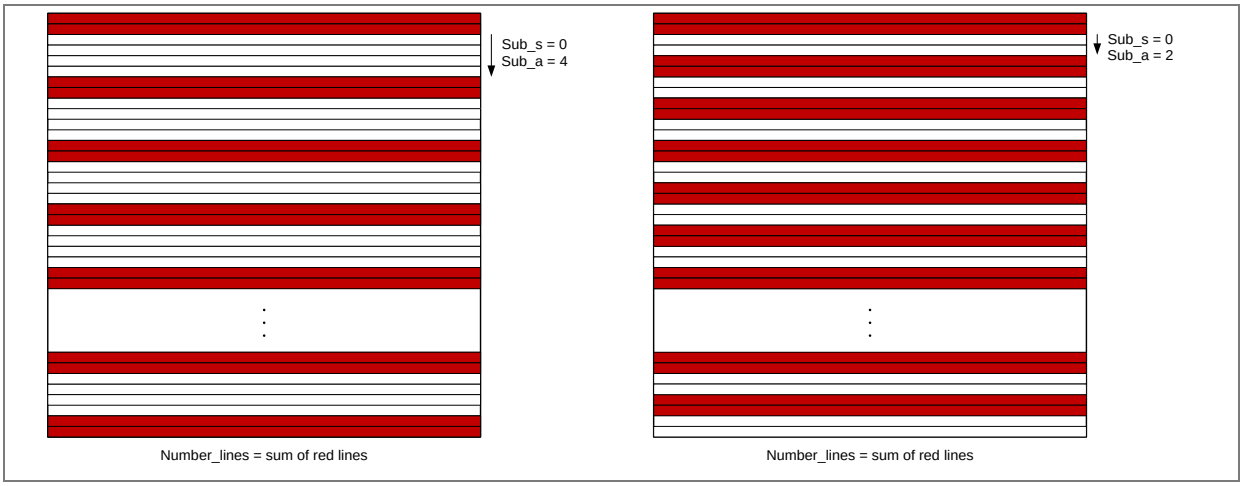
When using a color sensor, the subsampling scheme should preserve the Bayer pattern that is applied to the sensor. This means that the number of rows to be skipped should always be a multiple of two. An advanced subsampling scheme can be programmed to achieve these requirements. Of course, this advanced subsampling scheme can also be programmed in a monochrome sensor. See Table 22 for more details.

Table 22: Advanced subsampling register settings

Register name	Register address	Default value	Description of the value
Number_lines	1[7:0] 2[7:0]	1088	Defines the total number of lines read-out by the sensor (min=1, max=1088)
Sub_s	35[7:0] 36[7:0]	0	Should be '0' at all times
Sub_a	37[7:0] 38[7:0]	0	Number of rows to skip, it should be an even number between (0 and 2046).

Figure 54 shows two subsampling examples (skip 4x and skip 2x) in advanced mode.

Figure 54: Subsampling examples in advanced mode (skip 4x and skip 2x)



7.4.6 Number of frames

When internal exposure mode is selected, the number of frames sent by the sensor after a frame request can be programmed in the corresponding sequencer register.

Table 23: Number of frames register settings

Register name	Register address	Default value	Description of the value
Number_frames	70[7:0] 71[7:0]	1	Defines the number of frames grabbed and sent by the image sensor in internal exposure mode (min =1, max = 65535)

7.5 Configuring output data format

7.5.1 Output modes

The number of LVDS channels can be selected by programming the appropriate sequencer register. The pixel remapping scheme and the read-out timing for each mode can be found in chapter 7.3 of this document.

Table 24: Different output modes register settings

Register name	Register address	Default value	Description of the value
Output_mode	72[1:0]	0	0: 16 outputs 1: 8 outputs 2: 4 outputs 3: 2 outputs

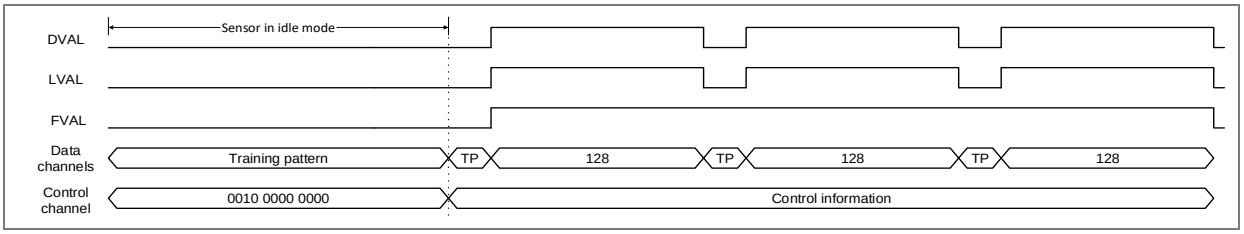
7.5.2 Training patterns

To synchronize the receiving side with the LVDS outputs of the CMV2000, a known data pattern can be put on the output channels. This pattern can be used to “train” the LVDS receiver of the surrounding system to achieve correct word alignment of the image data. Such a training pattern is put on all 16 data channel outputs when there is no valid image data to be sent (so, also in between bursts of 128 pixels). The training pattern is a 10-bit or 12-bit data word that replaces the pixel data. The sensor has a 12-bit sequencer register (address 78-79) that can be loaded through the SPI to change the contents of the 12-bit training pattern.

The control channel does not send a training pattern, because it is used to send control information at all time. Word alignment can be done on this channel when the sensor is idle (not exposing or sending image data). In this case all bits of the control word are zero, except for bit [9] (= 0010 0000 0000 or 512 decimal).

Figure 55 shows the location of the training pattern (TP) on the data channels when the sensor is idle and when reading out 3 rows. The default mode of 16 outputs is selected.

Figure 55: Training pattern location in the data and control channels



7.5.3 10-bit or 12-bit mode

The CMV2000 has the possibility to send 12 bits or 10 bits per pixel. The end user can select the desired resolution by programming the corresponding sequencer register. Always keep Bit_mode and ADC_Resolution in the same bit mode. This is shown in Table 25.

Table 25: Bit mode and ADC resolution register settings for version 2

Register name	Register address	Default value	Description of the value
Bit_mode	111[0]	1	0: 12 bits per pixel 1: 10 bits per pixel
ADC_Resolution	112[1:0]	0	0: 10 bits per pixel 1: 11 bits per pixel 2: 12 bits per pixel

Version 3 of this image sensor offers an ADC resolution of 11 bits. The bit mode must be changed like shown in Table 26.

Table 26: Bit mode and ADC resolution register settings for version 3

Register name	Register address	Default value	Description of the value
Bit_mode	111[0]	1	0: 12 bits per pixel 1: 10 bits per pixel
ADC_Resolution	112[1:0]	0	0: 10 bits per pixel 1: 11 bits per pixel 2: 12 bits per pixel
	117[7:0]	8	10-bit: Set to 8 12-bit: Set to 4
	116[3:0]	9	10-bit: Set to 9 12-bit: Set to 11

7.5.4 Data rate

Information:

This is only applicable for Version 2.

During start-up or after a sequencer reset, the data rate can be changed if a lower speed than 480 Mbps is desired. This can be done by applying a lower master input clock (CLK_IN) and high speed LVDS clock (LVDS_CLK_N/P) to the sensor. See chapter 7.2.4 for more details on the input clock and chapter 7.2.5 for details on how the data rate can be changed. No registers have to be changed when using a data rate different from 480 Mbps.

7.5.5 Power control

The power consumption of the CMV2000 can be decreased by disabling the LVDS data channels when they are not used (in 8, 4 or 2 outputs mode). The power will decrease with approximately 18 mW per channel. So, reducing the outputs from 16 to 4 will save you about 216 mW or 33%. This is the main source for saving power. Other settings (such as bitrate, fps, temperature …) will have very little to no effect on the total power consumption.

Table 27: Power control register settings

Register name	Register address	Default value	Description of the value
Channel_en	80[7:0] 81[7:0] 82[2:0]	All ‘1’	Bits 0-15 enable/disable the data output channels Bit 16 enables/disables the clock channel Bit 17 enables/disables the control channel Bit 18 enables/disables the LVDS clock input 0: Disabled 1: Enabled

Decreasing the master clock frequency and thereby the LVDS clock frequency will also decrease power consumption albeit little. Decreasing the LVDS_CLK frequency from 480 MHz to 128 MHz will decrease power consumption with about 25 mW. All power savings will happen on the VDD20 supply. Other settings or factors have little to no effect on power consumption.

7.6 Configuring on-chip data

7.6.1 Offset and gain

7.6.1.1 Offset

A digital offset can be applied to the output signal. This dark level offset can be programmed by setting the desired value in the sequencer register. The 14-bit register value is a 2-complement number, allowing to have a positive and a negative offset (from 8191 to -8192). The ADC itself has a fixed offset of 70.

So, the dark-level @ output = 70 + Offset (in 2's complement). For example, register value 16323 (11 1111 1100 0011) equals -61 in 2's complement. The default dark-level is thus set at 70 - 61 = 9 digital numbers.

Table 28: Offset

Register name	Register address	Default value	Description of the value
Offset	100[7:0] 101[5:0]	16323	Defines the dark level offset applied to the output signal (min = 0, max = 16383). The value is in 2's complement: **Decimal** / **Binary** / **2's comp.** 0 / 00 0000 0000 0000 / 0 1 / 00 0000 0000 0001 / 1 … / … / … 8191 / 01 1111 1111 1111 / 8191 8192 / 10 0000 0000 0000 / -8192 8193 / 10 0000 0000 0001 / -8191 … / … / … 16383 / 11 1111 1111 1111 / -1

7.6.1.2 Gain

An analog gain and ADC gain can be applied to the output signal. The analog gain is applied by a PGA in every column. The digital gain is applied by the ADC.

Information:

Depending on the sensor version, there is a slight difference in the register settings. Therefore, depending on the sensor version the user should follow Table 29 for version 2 and Table 30 for version 3.

Table 29: Gain settings for version 2

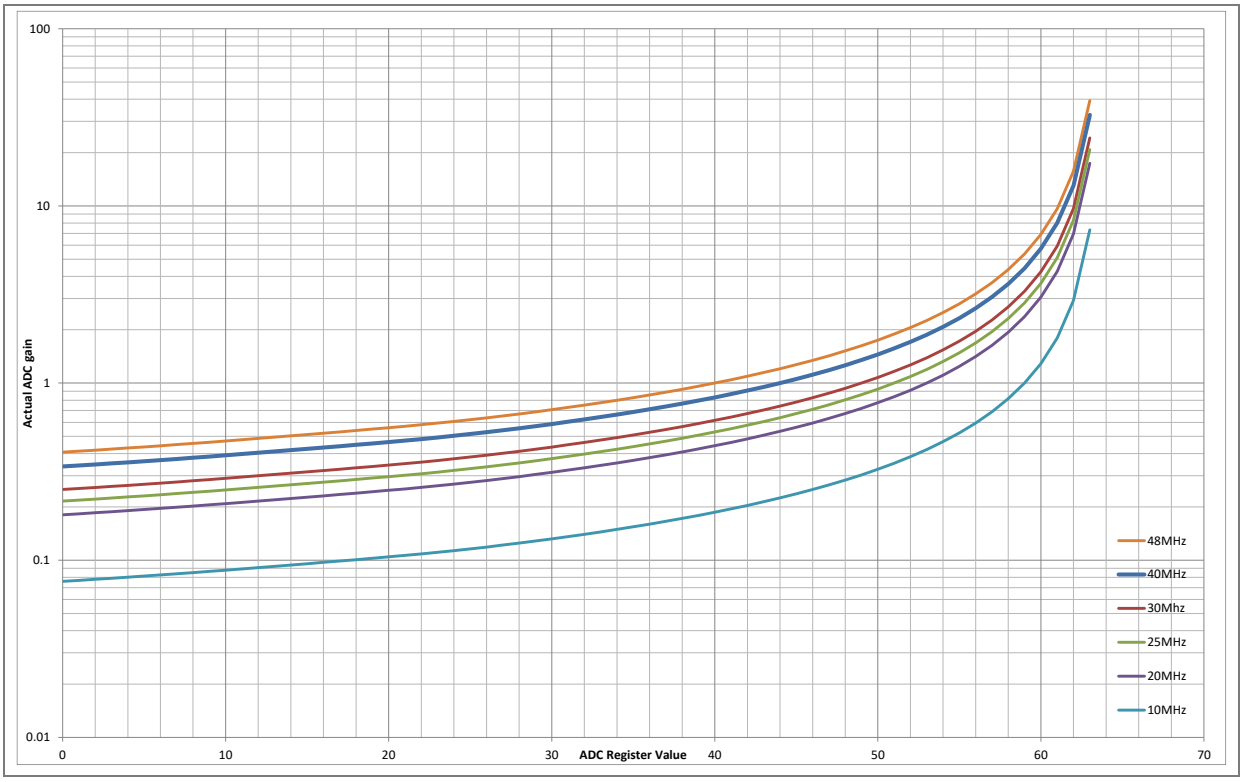
Register name	Register address	Default value	Description of the value
PGA_gain	102[1:0]	0	102[1:0] 0: x1 gain 1: x1.2 gain 2: x1.4 gain 3: x1.6 gain
ADC_gain	103[7:0]	32	Defines the slope of the ADC ramp, a higher value equals more gain.

Table 30: Gain settings for version 3

Register name	Register address	Default value	Description of the value
PGA_gain	102[1:0] 121[0]	0	102[1:0] 0: x1 gain 1: x1.2 gain 2: x1.4 gain 3: x1.6 gain 121[0] 0: Gain is defined in 102[1:0] 1: Gain in 102[1:0] is amplified by 2
ADC_gain	103[7:0]	32	Defines the slope of the ADC ramp, a higher value equals more gain.

The ADC gain is dependent on the master clock. A slower clock signal means a higher ADC_gain register value for an actual ADC gain of 1x. Also at higher register values, the actual ADC gain will increase in bigger steps. So, fine-tuning the ADC gain is easier at lower register values.

Figure 56: Typical graphs of gain setting



7.6.2 Black reference columns

Information:

This chapter is just applicable for Version 3.

When the appropriate SPI register is set, the 16 first columns will be put to an electrical black reference. This electrical black reference can be used to reduce the row noise and/or track black level.

Table 31: Black columns

Register name	Register address	Default value	Description of the value
Black_col_en	121[1]	0	0: Disable 1: Enable

7.6.3 Horizontal line effect during exposure start

Information:

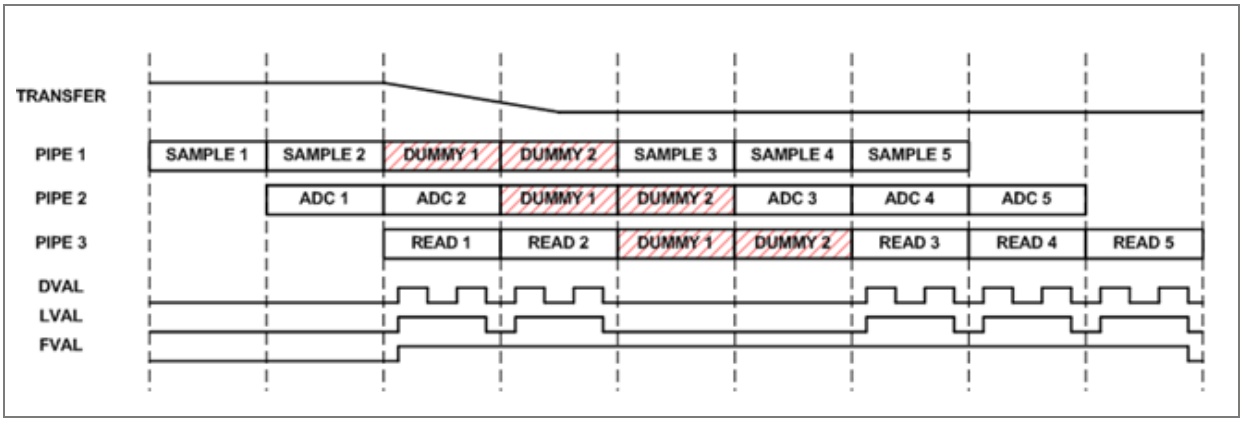
This chapter is just applicable for Version 3.

When the exposure of an image frame is started while a previous image frame is read out this action may become visible in the image frame currently read out. The effect is visible in the line addressed for read-out at the moment the exposure of the next image frame starts. Depending on the moment when the exposure starts within the line read-out time, this will result in a bright or dark offset for the addressed line. This horizontal line artifact is due to the cross-talk of the global transfer gate pulse on the column read-out.

This problem is solved by changing the sequencer timing. At the moment the global transfer is pulsed, a programmable number of dummy rows can be inserted in the read-out. This means that the transfer pulse crosstalk does not influence valid data rows.

The exact internal impact of the new timing depends on the read-out and exposure modes (PLR, internal or external exposure control…). Externally, the only impact is that the DVAL and LVAL outputs are not pulsed for a number of row periods. The external system should always monitor the DVAL, LVAL and FVAL pulses to know when valid pixels, lines and frames become available. Figure 57 shows the timing (in case of 2 dummy rows).

Figure 57: Timing of DVAL, LVAL and FVAL to avoid horizontal line artifact



By default, no dummy rows are inserted in the read-out. The dummy rows are enabled by loading the appropriate values to the register inte_sync and dummy.

Table 32: Dummy rows

Register name	Register address	Default value	Description of the value
Inte_sync	41[2]	0	Must be set to 1 if Dummy is not 0
Dummy	118[7:0]	0	Sets the number of dummy rows

Information:

Note that the register ‘dummy’ sets the number of dummy rows (one row corresponds to one LVAL pulse). In multiplex modes, there are several timing slots within a single row read-out. In case dual exposure is used, the dummy rows are generated for both transfer pulse toggles.

8 Register description

The Table 33 gives an overview of all the sensor registers. The registers with the remark “Do not change” should not be changed unless advised in chapter 7.4.

8.1 Register overview

Table 33: Register overview

Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
0	0									Do not change
1	64	Number_lines [7:0]								
2	4	Number lines [15:8]								
3	0	Start1[7:0]								
4	0	Start1[15:8]								
5	0	Start2[7:0]								
6	0	Start2[15:8]								
7	0	Start3[7:0]								
8	0	Start3[15:8]								
9	0	Start4[7:0]								
10	0	Start4[15:8]								
11	0	Start5[7:0]								
12	0	Start5[15:8]								
13	0	Start6[7:0]								
14	0	Start6[15:8]								
15	0	Start7[7:0]								
16	0	Start7[15:8]								
17	0	Start8[7:0]								
18	0	Start8[15:8]								
19	0	Number_lines1[7:0]								
20	0	Number_lines1[15:8]								
21	0	Number_lines2[7:0]								
22	0	Number_lines2[15:8]								
23	0	Number_lines3[7:0]								
24	0	Number_lines3[15:8]								
25	0	Number_lines4[7:0]								
26	0	Number_lines4[15:8]								

Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
27	0	Number_lines5[7:0]								
28	0	Number_lines5[15:8]								
29	0	Number_lines6[7:0]								
30	0	Number_lines6[15:8]								
31	0	Number_lines7[7:0]								
32	0	Number_lines7[15:8]								
33	0	Number_lines8[7:0]								
34	0	Number_lines8[15:8]								
35	0	Sub_s[7:0]								
36	0	Sub_s[15:8]								
37	0	Sub_a[7:0]								
38	0	Sub_a[15:8]								
39	1								mono	
40	0							Image_flipping[1:0]		
41	0						Inte_sync(1)	Exp_dual	Exp_ext	V3:Set to 4
42	64	Exp_time[7:0]								
43	4	Exp_time[15:8]								
44	0	Exp_time[23:16]								
45	0	Exp_step[7:0]								
46	0	Exp_step[15:8]								
47	0	Exp_step[23:16]								
48	1	Exp_kp1[7:0]								
49	0	Exp_kp1[15:8]								
50	0	Exp_kp1[23:16]								
51	1	Exp_kp2[7:0]								
52	0	Exp_kp2[15:8]								
53	0	Exp_kp2[23:16]								
54	1							Nr_slopes[1:0]		
55	1	Exp_seq[7:0]								
56	V2: 64 V3: 0	Exp_time2[7:0]								
57	V2: 4 V3: 8	Exp_time2[15:8]								
58	0	Exp_time2[23:16]								
59	0	Exp_step2[7:0]								
60	0	Exp_step2[15:8]								
61	0	Exp_step2[23:16]								

Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
62	1									Do not change
63	0									Do not change
64	0									Do not change
65	1									Do not change
66	0									Do not change
67	0									Do not change
68	1									Do not change
69	1	Exp2_seq[7:0]								
70	1	Number_frames [7:0]								
71	0	Number_frames[15:8]								
72	0							Output_mode[1:0]		
73	10	fot_length[7:0]								Can be lowered to 5, see chapter 7.4.1
74	8						i_lvds_rec[3:0](1)			V2: Do not change
75	8									Do not change
76	8									Do not change
77	3							Col_calib(1)	ADC_calib(1)	V2: Do not change V3: Set to 0
78	85	Training_pattern[7:0]								
79	0	Training pattern [11:8]								
80	255	Channel_en[7:0]								
81	255	Channel_en[15:8]								
82	3						Channel_en [18:16]			V2: Set to 7 V3: See chapter 7.5.5 and set to 7
83	8						i_lvds[3:0]			Can be lowered to 4 for meeting EMC standards
84	8						I_col[3:0]			Set to 4
85	8						I_col_prech[3:0]			Set to 1
86	8									Do not change
87	8						I_amp[3:0](1)			V2: Do not change V3: Set to 12
88	96	Vtf_l1[6:0]								Set to 64
89	96	Vlow2[6:0]								

Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
90	96	Vlow3[6:0]								
91	96	Vres_low[6:0]								Set to 64
92	96									Do not change
93	96									Do not change
94	96	V_prech[6:0]								Set to 101
95	96	V_ref[6:0]								Set to 106
96	96									Do not change
97	96									Do not change
98	96	Vramp1[6:0]								See 8.2.1
99	96	Vramp2[6:0]								See 8.2.1
100	195	Offset[7:0]								See 8.2.1
101	63	Offset[13:8]								See 8.2.1
102	0							PGA_gain[1:0]		V3: Set to 1
103	32	ADC_gain[7:0]								See 8.2.1
104	8									Do not change
105	8									Do not change
106	8									Do not change
107	8									Do not change
108	0						T_dig1[3:0]			
109	1						T_dig2[3:0]			
110	0									Do not change
111	1								Bit_ mode	
112	0							ADC_resolution [1:0]		
113	1									V2: Do not change V3: Set to 0
114	0									Do not change
115	0								Config 2	Only V2: Set to 1
115	0									Only V3: Set to 1
116	V2: 32 V3: 217									V2: Do not change V3: See chapter 7.5.3
117	8								Config 1	Only V2: Set to 1
117	8									Only V3: See chapter 7.5.3

Address	Default	Value								Remark
		bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	
118	0	Dummy[7:0]								V2: Do not change V3: Set to 1
119	0									Do not change
120	0									Do not change
121	0							Black_col_en(1)	PGA_gain[0](1)	V2: Do not change
122	0									Do not change
123	V2: 0 V3: 64	V_blacksun[5:0](1)								V2: Do not change V3: Set to 98
124	0									Do not change
125	xx(2)									Do not change
126	0	Temp[7:0]								
127	0	Temp[15:8]								

8.2 Recommended register settings

The following table gives an overview of the registers, which have a required value that is different from their default start-up value. We strongly recommend to load these register settings after start-up and before grabbing an image.

Information:

Depending on the sensor version, there is a slight difference in the register settings. Therefore, the user should follow Table 34 for version 2 and Table 35 for version 3.

Table 34: Recommended registers for version 2

Address	Name	Required value
82[2:0]	Channel_en	7
84[3:0]	I_col	4
85[3:0]	I_col_prech	1
88[6:0]	V_tglow1	64
91[6:0]	Vres_low	64

Address	Name	Required value
94[6:0]	V_precharge	101
95[6:0]	V_ref	106
115[0]	Config2	1
117[0]	Config1	1

Table 35: Recommended registers for version 3

Address	Name	Required value
41[2:0]	Inte_sync Exp_dual Exp_ext	4
77[1:0]	Col_calib ADC_calib	0
84[3:0]	I_col	4
85[3:0]	I_col_prech	1
87[3:0]	I_amp	12
88[6:0]	Vtf_l1	64
91[6:0]	Vres_low	64
94[6:0]	V_prech	101
95[6:0]	V_ref	106
102[1:0]	PGA	1
118[7:0]	Dummy	1
123[5:0]	V_blacksun	98

8.2.1 Adjusting register for optimal performance

Due to processing differences, the response and optical performance may differ slightly from sensor to sensor. To adjust this difference in response, the following registers in should be tuned from sensor to sensor.

Information:

Depending on the sensor version, there is a slight difference in the register settings. Therefore, the user should follow Table 36 for version 2 and Table 37 for version 3.

Table 36: Optical performance registers for version 2

Address	Name	Required value	Valid range
103[7:0]	ADC_GAIN	32	40 - 55
98[6:0]	V_ramp1	96	102 - 115
99[6:0]	V_ramp2	96	102 - 115
100[7:0]	Offset	16323	0 - 16383

Table 37: Optical performance registers for version 3

Address	Name	Required value	Valid range
103[7:0]	ADC_GAIN	See Gain chapter	0 - 63
98[6:0]	V_ramp1	109	102 - 115
99[6:0]	V_ramp2	109	102 - 115
100[7:0] 101[5:0]	Offset	16323	0 - 16383

To optimize the sensor response and minimize noise, the following procedure should be followed for each sensor:

1. Start by programming all registers with the recommended values from the datasheet.
2. Take fully dark images with short exposure and calibrate the offset register so no pixel clips in black (< 0DN).
3. When column non-uniformities are observed in the dark image, a calibration of the V_ramp1 and V_ramp2 registers is necessary. These registers set the starting voltage of the ramp used by the column ramp ADC, so adjusting this value will improve column CDS (correlated double sampling) which will reduce the column FPN. Both values should be adjusted together and should always have the same value.
4. Now take images with light and normal exposure. If the image is not saturated, increase the light or the exposure time until all pixels reach a constant value. If not all pixels saturate at 1023 (meaning that the non-linear part of the pixel voltage is in the ADC input range), increase the ADC gain/range setting until they do. The PGA amplifier can also be used at this stage.
5. The dark offset level may have shifted when doing ADC calibration, so repeat step 2.

6. To compensate gain differences between sensors, choose a fixed light setting or exposure time at which the sensor shows a grey image about 50% of its swing (512 at 10-bit). Now tweak the ADC setting per sensor so that all sensors will have the same average grey value of about 512. This way all sensors will behave about the same to the same amount of light.

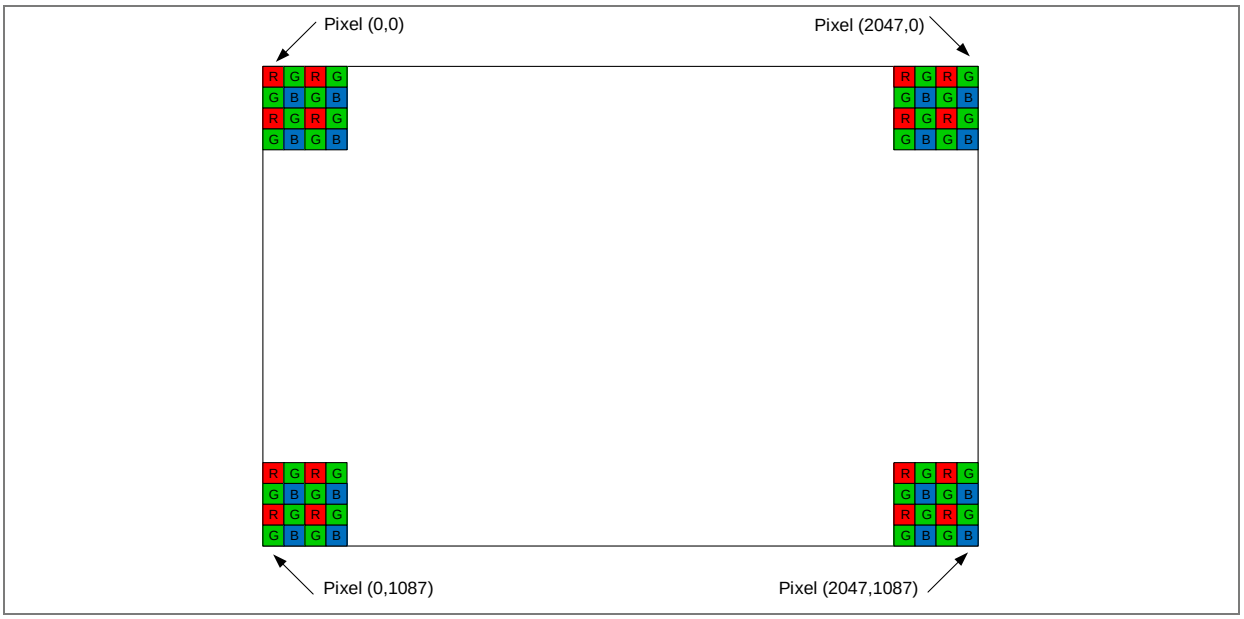
9 Application information

9.1 Color filter

An RGB Bayer pattern is used on the CMV2000 image sensor. The order of the RGB filter can be found in the drawing below. With Y-flipping off (reg40 = 0), pixel (0,0) at the top left is read out first and has a red filter. When Y-flipping is on, pixel (0,1087) is read out first and has a green filter.

For X-flipping the address of the first pixel depends on the output channels used.

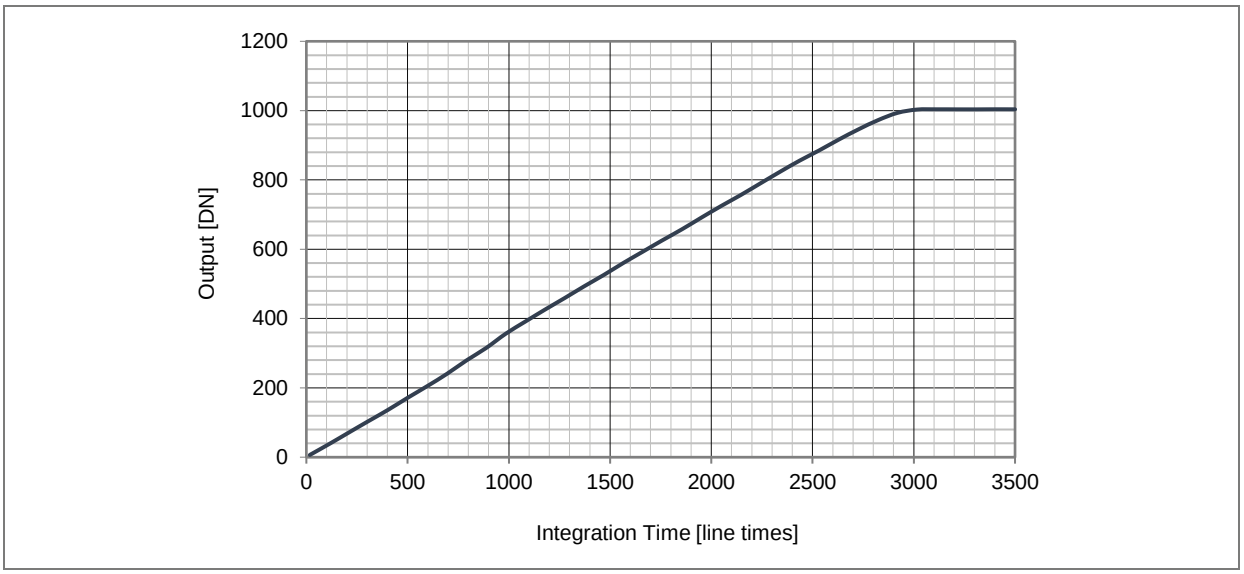
Figure 58: RGB bayer pattern order



9.2 Response curve

Figure 59 shows a typical response curve of integration time (or light input) versus the average output value of the sensor.

Figure 59: Typical response curve

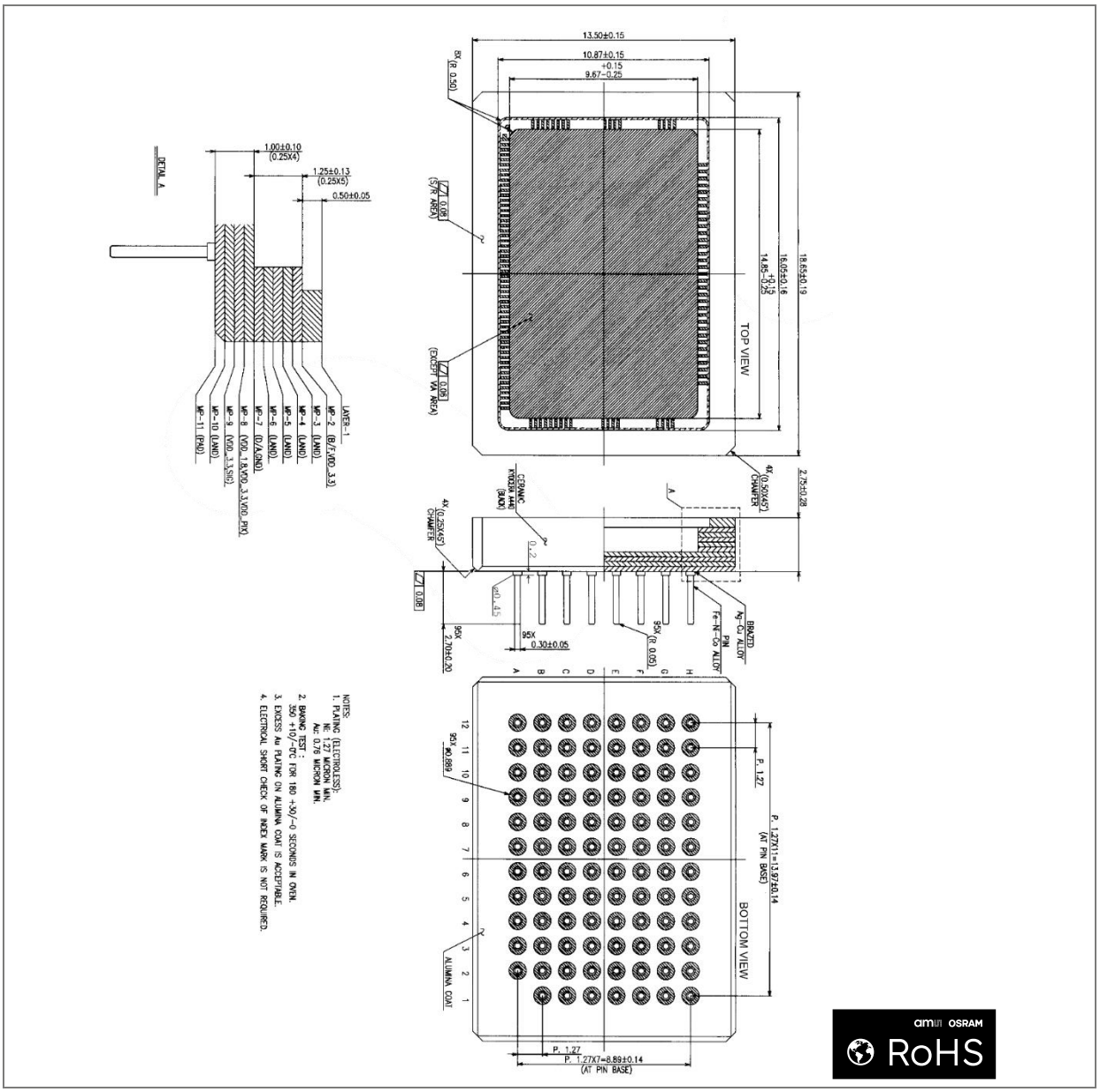


10 Package drawings & markings

10.1 95 pins µPGA and LGA

All dimensions are in millimeter. The LGA package (SMD) is identical to the µPGA but without the through-hole pins.

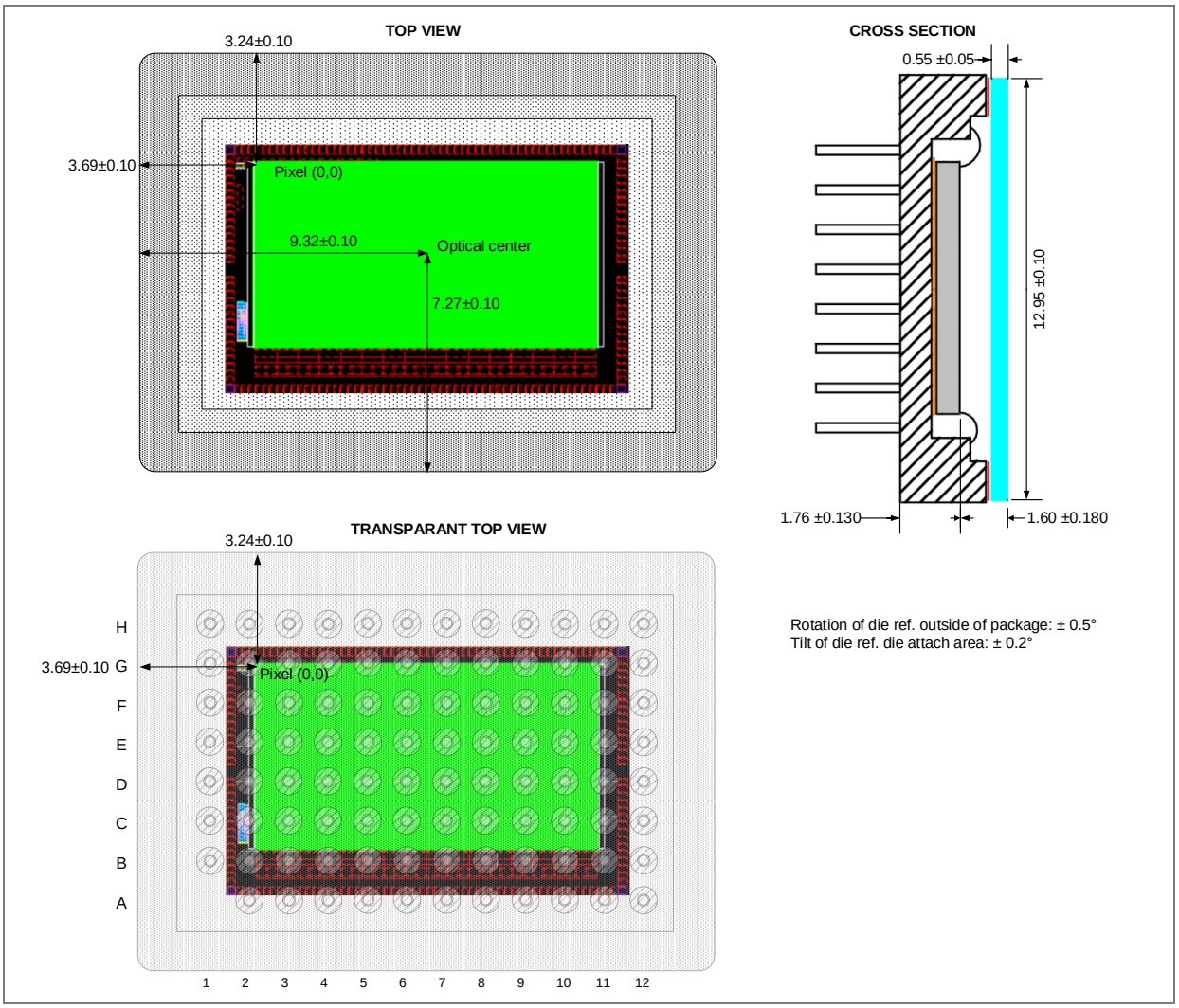
Figure 60: µPGA package drawing



10.1.1 Assembly drawing µPGA

All dimensions are in millimeter.

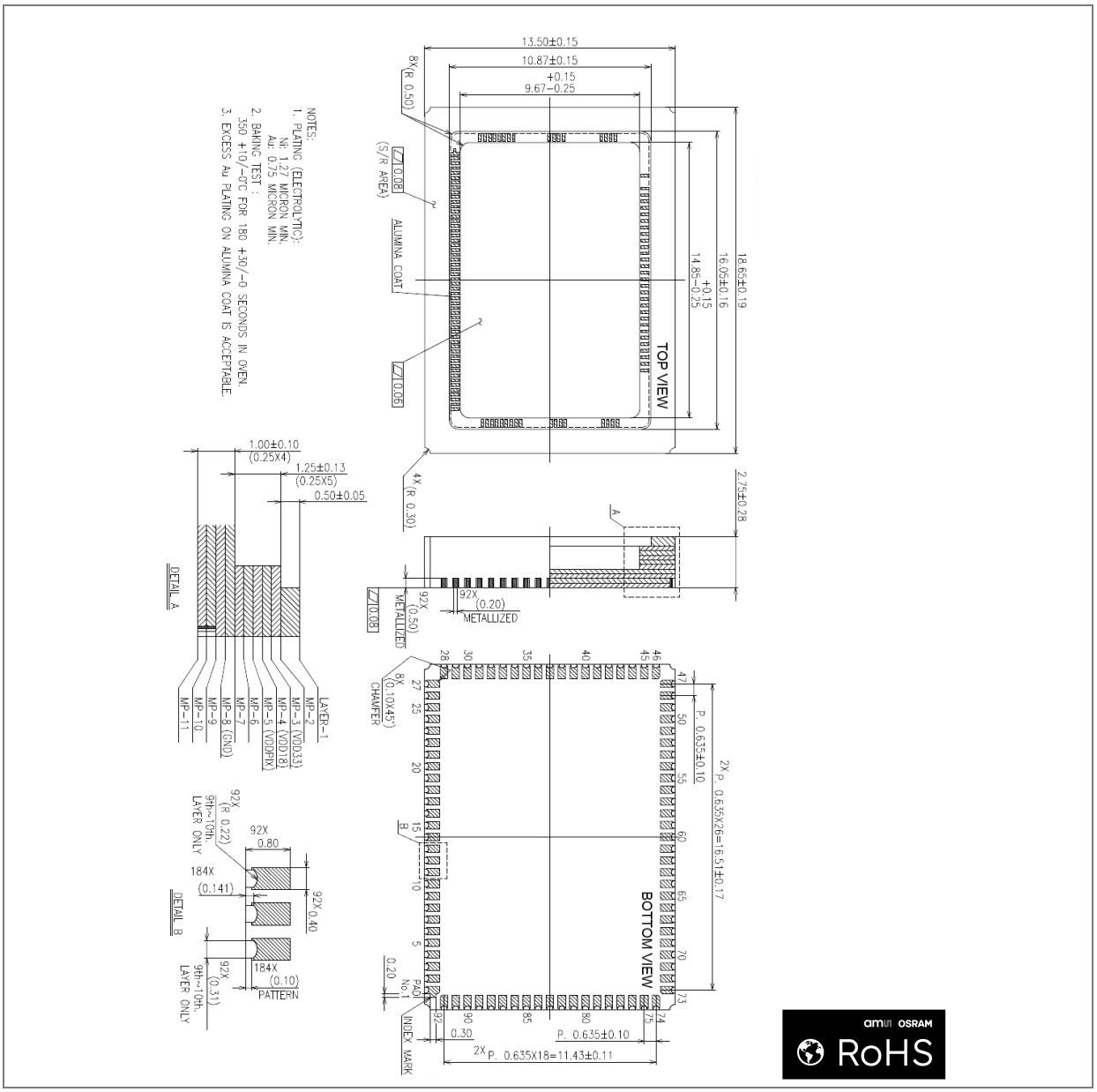
Figure 61: Assembly drawing µPGA



10.2 92 pins LCC

All dimensions are in millimeter.

Figure 62: LCC package drawing



11 Soldering & storage information

CMV2000 is shipped in a moisture barrier package. We recommend to keep the moisture barrier package closed and stored under the conditions shown in Table 5. Only open the moisture barrier package before the usage of the devices.

When reflow soldering, a dry bake needs to be performed upfront! For soldering information, follow Standard J-STD-020. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.

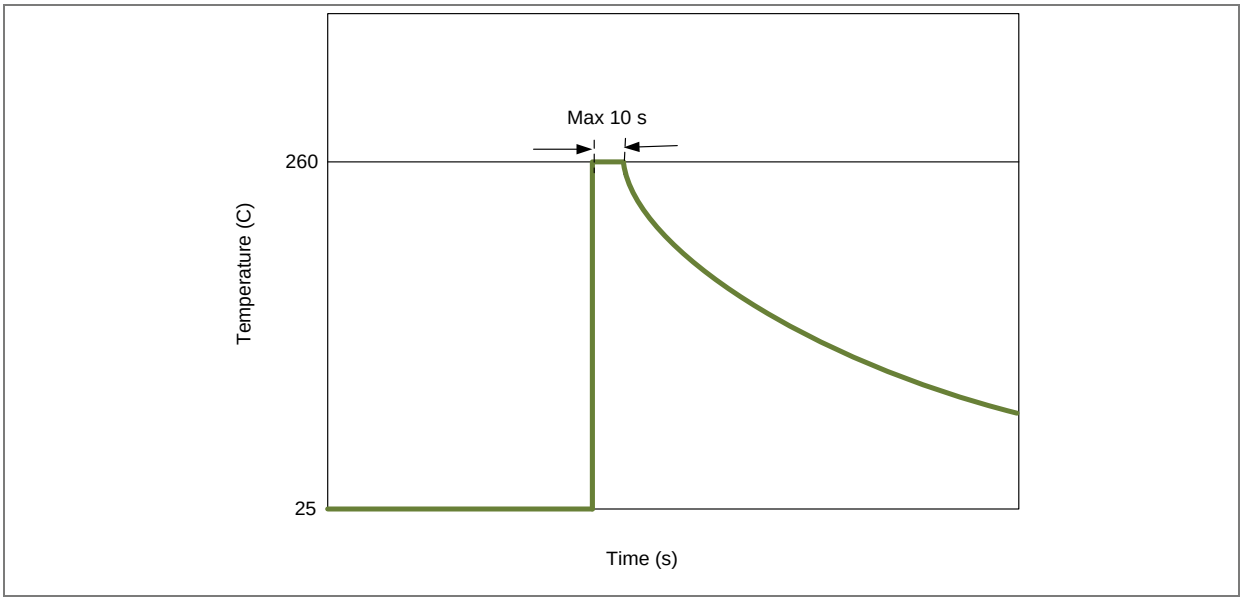
11.1 Manual soldering

Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350 ºC with 270 °C maximum pin temperature, 2 seconds maximum duration per pin. Avoid global heating of the ceramic package during soldering. Failure to do so may alter device performance and reliability.

11.2 Wave soldering

Wave soldering is possible but not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. See Figure 63 for the wave soldering profile.

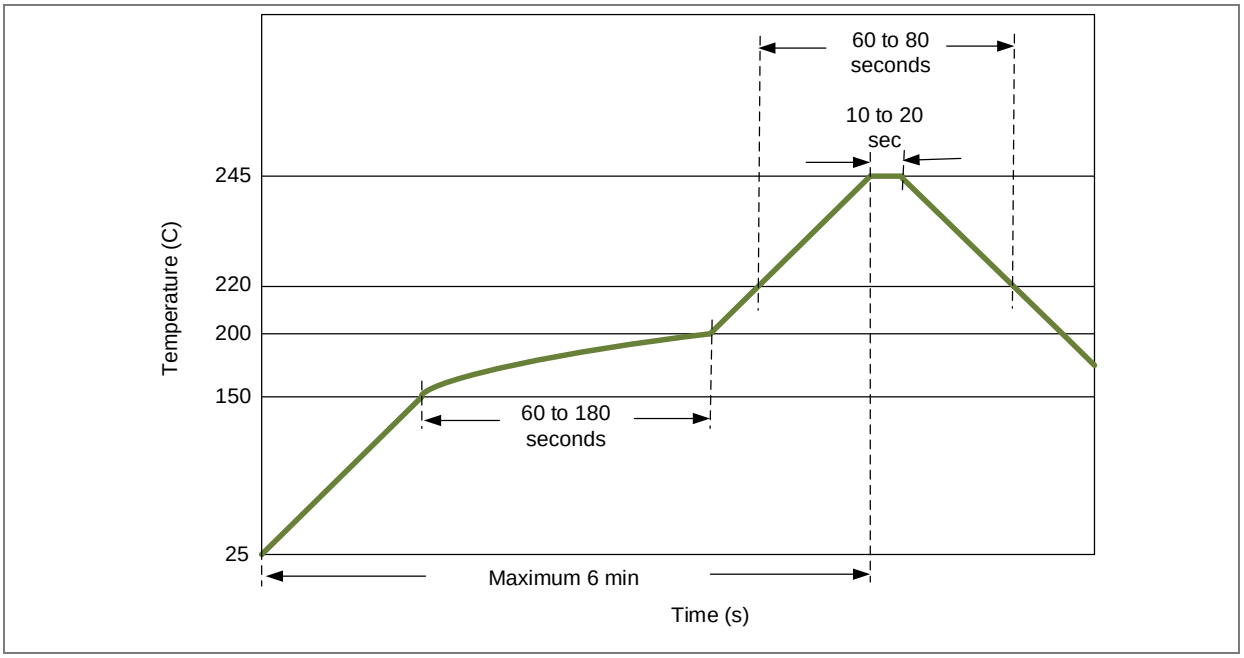
Figure 63: Wave solder profile



11.3 Reflow soldering

Figure 64 shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.

Figure 64: Reflow soldering graph



11.4 Additional recommendation

Image sensors with filter arrays (CFA) and micro-lens are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The best solution will be flow soldering or manual soldering of a socket (through hole) and plug in the sensor at latest stage of the assembly/test process.

12 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous released version to current revision v8-00	Page
Updated information on the description of Figure 15	28
Removed unnecessary paragraph under Figure 15	28

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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