TMF8829

Datasheet

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TMF8829 Time-of-flight sensor

1 General description

The TMF8829 is a direct time-of-flight (dToF) sensor with a resolution of up to 48x32. It has a very wide field of view (FOV) of 80° and achieves a detection range of up to 11 m.

The TMF8829 is a direct time-of-flight (dToF) sensor available in a small footprint modular package with two integrated Vertical Cavity Surface Emitting Lasers (VCSELs). The dToF device is based on SPAD, TDC, and histogram technology and achieves a detection range of up to 11000 mm. Due to its lens on the SPAD, it supports 8x8, 16x16, 32x32 and 48x32 depth pixels and a very wide field of view. A multi-lens-array (MLA) inside the package above the VCSELs widens the FOI (field of illumination). All processing of the raw data is performed on-chip, and the TMF8829 provides distance information along with confidence values, signal amplitude, and ambient light on its interface.

Internally, the TMF8829 uses dToF histograms and peak detection, and therefore, it is highly tolerant to smudges on the cover glass. Additionally, the TMF8829 can handle multiple objects per depth point simultaneously without degrading accuracy. It reports the distance of all depth points with a resolution of 0.25 mm.

The device uses an I3C (I²C compatible) communication interface and a fully featured SPI interface for control and raw data streaming. A VBUS supply pin allows operation of the I²C/I3C or SPI with 1.2V, 1.8V, or 3V I/O supplies.

Raw data streaming, including all algorithm results, allows further processing on the host for “AI-enabled” applications.

The TMF8829 is a fully contained optical module measuring only 5.7 mm x 2.9 mm x 1.5 mm.

1.1 Key benefits & features

The benefits and features of TMF8829, Time-of-flight sensor are listed below:

Table 1: Added value of using TMF8829

Benefits	Features
Matches autofocus region of interest of mobile phone cameras including wide angle camera	80° FOV (diagonal, aspect ratio 4:3); rectangular SPADs
Detect object in a wide distance range	8x8 zone dToF operating mode 5.9 m, 18 % target, 30 Hz, indoor; 8m with 90% target
Distinguish several objects in field of view	16x16 zone dToF operating mode 5 m, 18 % target, 30 Hz, indoor; 5.9 m with 90% target
High resolution for support of hand gestures and face identification support	32x32 zone dToF operating mode 2.3 m, 18 % target, 15 Hz, indoor; 4.7 m with 90 % target 48x32 zone dToF operating mode 1.2 m, 18 % target, 15 Hz, indoor; 2.7 m with 90 % target
Multi-objects detection. Cover glass smudge tolerant	dToF operation with up to 4 objects per depth point.
Off-load host processing power	Full internal processing
AI enabled	Raw data streaming including processed distance data due to fast I3C and SPI interface
Wide range of host processors including newest generation 1v2 I/O supply	1.2V, 1.8V and 3V compliant I/O with dedicated I/O supply pin using I3C (I²C compatible)
Support macro range to telephoto range of mobile phone autofocus (LDAF)	1 cm minimum distance and 0.25 mm resolution
Battery powered applications; power scalable performance	340 mW power consumption at 30 Hz / 8 m / 8x8 / 90% 50 mW at 5 m
Wide range of applications	-40ºC to 85ºC temperature range
Allow integrations in space constrained applications	Module size 5.7 mm x 2.9 mm x 1.5 mm Smallest high resolution dToF sensor

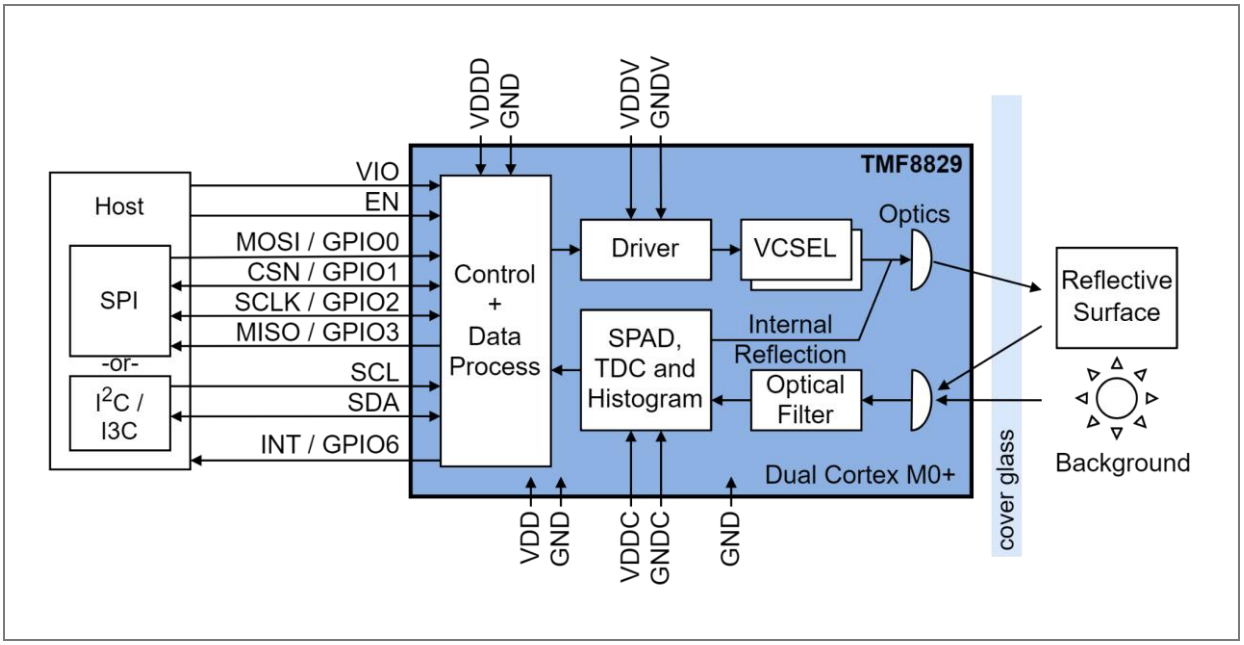
1.2 Applications

- LDAF - Laser detect autofocus
- Bokeh effect for cameras
- SLAM - Simultaneous Localization and Mapping
- Robot automation like obstacle avoidance, cliff detection and room scanning
- People counting
- Advanced gesture detection

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of TMF8829



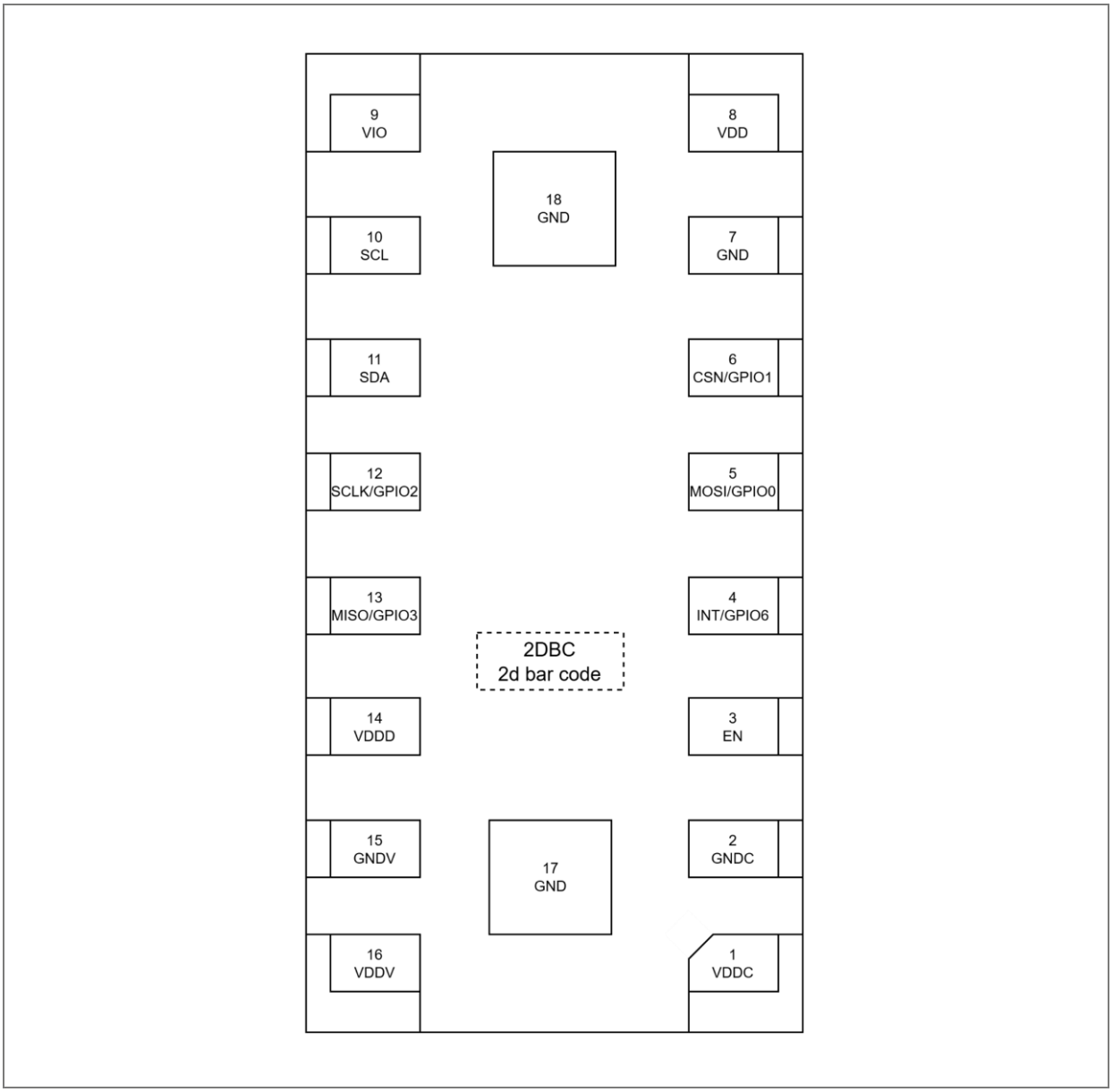
2 Ordering information

Product type	Ordering code	Package	Marking	Delivery form	Delivery quantity
TMF8829-1AM	Q65115A1077	Optical module	8-digit tracecode	Tape & reel 7” reels	500 pcs/reel
TMF8829-1A	Q65113A9854			Tape & reel 11” reels	3500 pcs/reel

3 Pin assignment

3.1 Pin diagram

Figure 2: Pin diagram of TMF8829 top through view (not to scale)



3.2 Pin description

Table 2: Pin description of TMF8829

Pin number	Pin name	Pin type[1]	Description
1	VDDC	PWR	Charge pump supply voltage (3.3 V) – connect all 3.3V VDD pins together; add a capacitor GRM155R70J105KA12 (0402 X7R 1 µF 6.3V) to GND
2	GNDC	GND	Charge pump ground; connect all ground pins together
3	EN	IN	Enable input active high; setting to low forces the device into shutdown and all memory content is lost; connect to VDD respectively VDDD if not used – see section 7.2.1
4	INT/GPIO6	I/O	Interrupt. Open-drain output default Hi-Z; can be used as GPIO pin if interrupt pin functionality is not used; connect to GND if not used
5	MOSI/GPIO0	I/O	SPI MOSI (master out slave in) input pin; default Hi-Z; can be used as GPIO if device is controlled by I3C/I²C; connect to GND if not used; do not leave floating
6	CSN/GPIO1	I/O	SPI CSN input pin; default Hi-Z; can be used as GPIO if device is controlled by I3C/I²C, for I3C/I²C mode, keep high until SPI mode has been disabled; connect to VIO if not used
7	GND	GND	Chip ground; connect all ground pins together
8	VDD	PWR	Chip supply voltage (3.3 V) – connect all 3.3V VDD pins together; add a capacitor GRM155R70J105KA12 (0402 X7R 1 µF 6.3 V) to GND
9	VIO	PWR	Digital pin supply for all digital pins of type IN, I/O and OD/IN; connect to 1.2V or 1.8V or 3.3V, connect GRM033R60J225ME47 (size= 0603M/0201) or similar with typ. 2.2µF, worst case 0.6µF @ 2.6V to GND
10	SCL	IN	I3C/I²C serial clock; can be used as GPIO4 pin if device is controlled by SPI; for SPI mode, keep high until I3C/I²C mode has been disabled; connect to VIO if not used
11	SDA	I/O	I3C/I²C serial data; can be used as GPIO5 pin if device is controlled by SPI; connect to GND if not used
12	SCLK/GPIO2	I/O	SPI SCLK input pin; default Hi-Z; can be used as GPIO if device is controlled by I3C/I²C; connect to GND if not used
13	MISO/GPIO3	I/O	SPI MISO (master in slave out) output pin; default Hi-Z; can be used as GPIO if device is controlled by I3C/I²C; connect to GND if not used
14	VDDD	PWR	Digital supply pin; add a capacitor GRM155R70J105KA12 (0402 X7R 1 µF 6.3 V) to GND
15	GNDV	GND	VCSEL ground; connect all ground pins together
16	VDDV	PWR	VCSEL supply voltage (3.3 V) – connect all 3.3V VDD pins together; add a capacitor GRM155R70J105KA12 (0402 X7R 1 µF 6.3 V) to GND
17	GND	PWR	Chip ground center pads; connect all ground pins together
18	GND	PWR	Chip ground center pads; connect all ground pins together

(1) Explanation of abbreviations:

IN	Digital input pin
I/O	Digital input output pin
GND	Ground supply pin
PWR	Power supply pin

Information:

All digital pins (MOSI/GPIO0, INT/GPIO6, SCL, SDA, CSN/GPIO1, SCLK/GPIO2 and MISO/GPIO3) have only a diode to VIO supply. Therefore, even with VDD = 0 V they do not block the interrupt line, I²C, I3C or SPI bus if VIO is supplied.

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of TMF8829

Symbol	Parameter	Min	Max	Unit	Comment
Electrical parameters					
VDDV, VDDC, VDD	3 V supply voltage	-0.3	3.6(1)	V	Connect pins VDDV, VDDC, VDD on PCB with very short connections
VDDD	1.8 V digital supply	-0.3	Max. 3.6 V	V	
VIO	Digital I/O supply voltage	-0.3	3.6(1)	V	VIO is independent and has no diode to any other supply.
GNDV, GNDC, GND	Ground	0.0	0.0	V	Connect all GND pins on PCB with very short connections
VIOMAX	Digital I/O terminal voltage	-0.3	VIO + 0.3 V max. 3.6 V	V	MOSI/GPIO0, CSN/GPIO1, SCLK/GPIO2, MISO/GPIO3, SCL, SDA and INT/GPIO6 have diodes to VIO but no diode to any other supply
VENMAX	EN pin max voltage	-0.3	3.6	V	Pin EN has no diode to any other supply
I_SCR	Latch up immunity		± 100	mA	JEDEC JESD78E
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM		± 2000	V	JEDEC JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM		± 500	V	JEDEC JS-002-2018
Temperature ranges and storage conditions					
T_{STRG}	Storage temperature range	-40	85	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020(2)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level		3		Represents a maximum floor life time of 168h with T_{AMB} < 30 °C and < 60% r.h.

(1) Limit supply rise to 1 V/µs
(2) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”.

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Device parameters are guaranteed at nominal conditions unless otherwise noted. While the device is operational across the temperature range, functionality will vary with temperature.

Table 4: Electrical characteristics of TMF8829

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comment
V_{VDDV}, V_{VDDC}, V_{VDD}	3.3V supply voltage; current <200mA	Functionality	2.9	3.3	3.5	V	
		Full performance	3.1	3.3	3.5	V	
V_{VIO}	I/O supply voltage	1.2V I/O	1.1	1.2	1.3	V	
		1.8V I/O	1.65	1.8	1.95	V	
		3.3V I/O	2.7	V_{VDD}	3.5	V	
V_{VDDD}	Digital supply voltage: To meet power specifications, use a DCDC converter with 1.8V output voltage; current <100mA		1.65	1.8	3.5	V	
t_{AMB}	Ambient temperature[1]		-40	25	85	°C	
Current consumption							
I_{POWER_DOWN}	Power down current	Pin EN=0; State: Power down; T_{AMB}=23°C		2	10	µA	
$I_{VIO\_VDD\_OFF}$	Leakage current into VIO for VDD=0V			0.1	10	µA	
$I_{STANDBY}$	Standby current	Current consumption for PON=0, wakeup by special I²C command State: Standby; I/O pins not toggling Only register ENABLE (Address 0xF8) accessible by I²C or SPI interface when in this mode.		13		µA	
$I_{STANDBY\_TIMER}$	Standby current with timer running[2]	Current consumption for PON=0, wakeup by timer or special IO State: Standby; I/O pins not toggling.		65		µA	
I_{ACTIVE}	Active current	Current consumption for CPUs running at 158.4 MHz, VCSEL and TDC off State: Active – CPU waiting		4		mA	
$I_{ACTIVE\_RANGING}$	Active current for ranging (VCSEL emitting light)	Current consumption for CPUs running at 158.4 MHz, VCSEL and TDC on State: Active – ranging		117		mA	

[1] Ensure $t_{JUNCTION}$ below 100 °C. To achieve this, set V_{VDDD} to 1.8V, V_{VDD} to 3.3V and/or reduce the duty cycle of the measurement.
[2] GPIOs programmed as output will be tristate during this mode. Use external pullup/pulldowns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comment
Power consumption for running application							
$P_{DIST\_30Hz\_8x8}$	Average power consumption best performance	Default settings with 30 Hz / 8 m / 8x8 zones mode / 90 % target		340		mW	
$P_{DIST\_30Hz\_16x16}$		Default settings with 15 Hz / 5.8 m / 16x16 zones mode / 18 % target		340		mW	
$P_{DIST\_30Hz\_8x8\_LP}$	Average power consumption reduced distance	50k iterations with 30 Hz / 5 m / 8x8 zones mode / 90 % target		50		mW	
I/O levels(1)							
I_{LEAK}	Leakage current to VIO or GND		-5		5	µA	Pins MOSI/GPIO0, CSN/GPIO1, SCLK/GPIO2, MISO/GPIO3, SCL, SDA, INT/GPIO6
V_{IH}	Input voltage high for 1v2 or 1v8 IO supply mode		0.7 * VIO		VIO+0.3 max 3.5	V	
V_{IH_3v3}	Input voltage high for 3v3 IO supply mode		0.8 * VIO		VIO+0.3 max 3.5	V	
V_{IL}	Input voltage low for 1v2 or 1v8 IO supply mode		-0.1 * VIO		0.3 * VIO	V	
V_{IL_3v3}	Input voltage low for 3v3 IO supply mode		-0.1 * VIO		0.2 * VIO	V	
V_{HYS}	Hysteresis		0.1 * VIO			V	
I_{LEAK_EN}	Leakage current to VIO / GND pin EN		-5		5	µA	Pin EN
V_{IH_EN}	Input voltage high pin EN		0.92		Max 3.5	V	
V_{IL_EN}	Input voltage low pin EN		0.0		0.32	V	
V_{HYS_EN}	Hysteresis pin EN		10	75		mV	
V_{OL_1v8}	Output voltage low 1v8 mode @ 3 mA		0		0.27	V	Pins MOSI/GPIO0, CSN/GPIO1, SCLK/GPIO2, MISO/GPIO3, SDA, INT/GPIO6
V_{OH_1v8}	Output voltage high 1v8 mode @ 3 mA		VIO-0.27		VIO	V	
V_{OL_1v2}	Output voltage low 1v2 mode @ 2 mA		0		0.18	V	
V_{OH_1v2}	Output voltage high 1v2 mode @ 2 mA		VIO-0.18		VIO	V	
Bus timing characteristics for I²C communications(1)							
f_{SCL}	SCL clock frequency		0	400	1000	kHz	
t_{BUF}	Bus free time between a STOP and START		0.5			µs	
$t_{HD:STA}$	Hold time (Repeated) start. After this period, the first clock pulse is generated		0.26			µs	
$t_{SU:STA}$	Set-up time for a repeated START condition		0.26			µs	
$t_{SU:STO}$	Set-up time for STOP condition		0.26			µs	
t_{LOW}	LOW period of SCL clock		0.5			µs	
t_{HIGH}	HIGH period of SCL clock		0.26			µs	
$t_{SU:STA}$	Setup time for a repeated START		0.26			µs	
$t_{HD:DAT}$	Data hold time		0			µs	
$t_{SU:DAT}$	Data setup time		50			ns	
t_R	Rise time of both SDA and SCL		20		120(2)	ns	
t_F	Fall time of both SDA and SCL		20		120(2)	ns	
f_{SCLK}	SCL clock frequency		0	400	1000	kHz	
f_{SP}	Pulse width of spikes that must be suppressed by the input filter				50	ns	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comment
Bus timing characteristics for I3C communications in push-pull mode(1)							
f_{SCL}	SCL clock frequency		0	12.5	12.9	MHz	
t_{LOW}	SCL clock low period		24			ns	
t_{DIG_L}	SCL clock low period at the receiver end		32			ns	
t_{HIGH}	SCL clock high period		24			ns	
t_{DIG_H}	SCL clock high period at the receiver end		32			ns	
t_{HIGH_MIXED}	SCL clock high period for mixed bus		24			ns	
$t_{DIG\_H\_MIXED}$	SCL clock high period for mixed bus at the receiver end		32		45	ns	
t_{SCO}	Clock-in to data-out for slave				12	ns	
t_{CF}	SCL clock fall time				$150/f_{SCL}$(3)	ns	
t_{CR}	SCL clock rise time				$150/f_{SCL}$(3)	ns	
t_{HD_PP}	SDA signal data hold time in push-pull mode		0(4)			ns	
t_{SU_PP}	SDA signal data setup time in push-pull mode		3			ns	
t_{CASr}	Clock after repeated START (Sr)		38.4			ns	
t_{CBSr}	Clock before repeated START (Sr)		19.2			ns	
Bus timing characteristics for I3C communications in open drain mode(1)							
t_{LOW_OD}	SCL clock low period		200			ns	
$t_{DIG\_OD\_L}$	SCL clock low period at the receiver end		t_{LOW_ODmin} + t_{fDA_ODmin}			ns	
t_{HIGH}	SCL clock high period		24		41	ns	
t_{DIG_H}	SCL clock high period at the receiver end		32		t_{HIGH} + t_{CF}	ns	
t_{fDA_OD}	SDA signal fall time		t_{CF}		12	ns	
t_{SU_OD}	SDA signal data setup time in open drain mode		3			ns	
t_{CAS}	Clock after start (S) condition		38.4 nano		50 milli(5)	s	
t_{CBP}	Clock before stop (P) condition		19.2			ns	
t_{AVAL}	Bus available condition		1			µs	
t_{IDLE}	Bus idle condition		200			µs	
SPI interface(1)							
f_{SPI}	SPI clock frequency				20	MHz	
t_{SPI_H}	SPI clock high time		20			ns	
t_{SPI_L}	SPI clock low time		20			ns	
Timings							
frame_rate_8x8	Maximum frame rate in 8x8 mode		60			Hz	8x8 zones mode
frame_rate_16x16	Maximum frame rate in 16x16 mode		30			Hz	16x16 zones mode
f_{clk}	RC oscillator, all internal timings are derived from this clock			4.95		MHz	
f_{CPUs}	Operating frequency of CPUs			fclk * 32 (158.4)		MHz	
t_{POR}	Power on time				2	ms	
t_{PON0}	Time to enter standby				100	µs	
t_{PON1}	Time to leave standby				100	µs	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comment
$t_{OFF\_TO\_MEASUREMENT}$	Time from power off to first measurement result				190	ms	
$t_{STBY\_TO\_MEASUREMENT}$	Time from standby to first measurement result				60	ms	
Optical parameters							
FOV_{DIAG}	Field of view diagonal			80		°	Diagonal full angle view
FOV_X	Field of view in x-direction			67.9		°	
FOV_Y	Field of view in y-direction			52.8		°	
Optical stack requirements							
$AIRGAP_{THICKNESS}$	Air gap		0.1	0.25	0.5	mm	
$GLASS_{THICKNESS}$	Glass thickness		0.5	0.65	1.0	mm	
$OPT\_STACK_{THICKNESS}$	Air gap + glass thickness				1.3	mm	
$GLASS_{TRANSPARENCY}$	Glass transparency @ 940nm			85		%	
RUBBER_BOOT	Rubber boot			Yes			
$XTALK_{SYSTEM}$	System crosstalk	Measured in final application		See ams OSRAM optical design guide			

(1) Over temperature and supply.
(2) The device Bus Timing Characteristics for I²C communications are designed to support Fast-mode Plus. Most of the timing parameters are downward compatible with Standard-mode and Fast-mode, except the t_F and t_R, where higher rise/fall time of 300 ns are acceptable for fast-mode (400 kHz).
(3) t_{CF} and t_{CR} are capped at 60ns.
(4) According to MIP I3C Specification V1-0, the Master Device Data Hold Time needs to keep at least 3ns.
(5) The device does not support ENTAS0-ENTAS3 CCCs. The t_{CAS} maximum is 50 ms fixed.

5.1 Algorithm performance parameters

Table 5: Algorithm performance parameters

Parameter	Condition		Min	Nom	Max	Units
Timings						
Default data rate	8x8 or 16x16 default mode, 600k iterations			33		ms
Object detection algorithm parameters						
Reflectivity of object at 940 nm	Perpendicular to TMF8829		5		90	%
Maximum distance[3] detection, 1.5 m x 1.5 m object Object perpendicular to measured zone		350 lux fluorescent light on object, 90% white card, center pixel, 8x8 long range mode, 2000k iterations		11000		mm
	8x8 mode, 33 ms, 600k iterations	350 lux fluorescent light on object, 90% white card, center pixel, 8x8 long range mode, 300k iterations		8000		mm
		350 lux fluorescent light on object, 18% grey card, center pixel		5900		mm
		350 lux fluorescent light on object, 90% white card, corner pixel		6000		mm
		350 lux fluorescent light on object, 18% grey card, corner pixel		3400		mm
		5 k lux sunlight[1] on object, 18% grey card, center pixel		1370		mm
		50 k lux sunlight[2] on object, 18% grey card, center pixel		590		mm
	16x16 mode, 33 ms, 600k iterations	350 lux fluorescent light on object, 90% white card, center pixel		5900		mm
		350 lux fluorescent light on object, 18% grey card, center pixel		5800		mm
		350 lux fluorescent light on object, 90% white card, corner pixel		5700		mm
		350 lux fluorescent light on object, 18% grey card, corner pixel		3000		mm
		5 k lux sunlight[1] on object, 18% grey card, center pixel		1030		mm
	32x32 mode, 66 ms, 1200k iterations	350 lux fluorescent light on object, 90% white card, center pixel		5000		mm
		350 lux fluorescent light on object, 18% grey card, center pixel		2300		mm
		350 lux fluorescent light on object, 90% white card, corner pixel		3000		mm
		350 lux fluorescent light on object, 18% grey card, corner pixel		1500		mm
	48x32 mode, 66 ms, 1200k iterations	350 lux fluorescent light on object, 90% white card, center pixel		2700		mm
		350 lux fluorescent light on object, 18% grey card, center pixel		1200		mm
		350 lux fluorescent light on object, 90% white card, corner pixel		1900		mm
		350 lux fluorescent light on object, 18% grey card, corner pixel		800		mm

Parameter	Condition	Min	Nom	Max	Units
Minimum distance detection, 18 % grey card, 20 cm x 26 cm			10		mm
Accuracy	Object distance ≥ 300 mm		±3		%
	20 mm ≤ object distance < 300 mm Mode: *_HIGH_ACCURACY modes or any of the dual modes see section 7.3		±10		mm
	10 mm ≤ object distance < 20 mm Mode: *_HIGH_ACCURACY modes or any of the dual modes see section 7.3		+15 -15		mm
Precision	350 lux fluorescent light on object		2 mm + 0.5% of distance		For ±2 sigma (95%)

(1) 5 k lux sunlight is represented by 830 Lux halogen light: Light on object only.
(2) 50 k lux sunlight is represented by 8300 Lux halogen light: Light on object only.
(3) Due to SPAD screamers, a small number of pixels can have a degraded performance in detection distance due to higher noise. This is only applicable for low ambient light conditions.

6 Typical operating characteristics

Figure 3: Linear scan 10 mm – 1000 mm, high accuracy 16x16 mode, pixel [3,3], 600k iterations, black: 1800k iterations, 350 lux fluorescent lighting

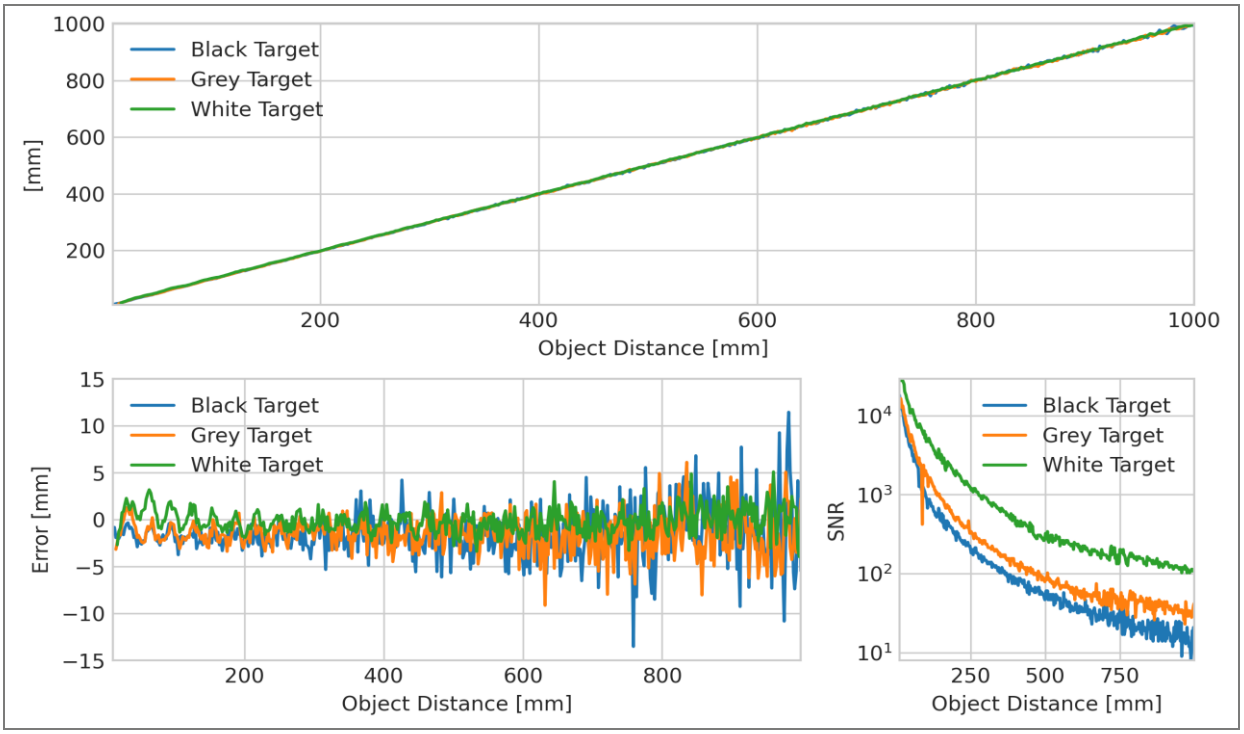


Figure 4: Distance vs. temperature
no ambient light, fixed target distance 280 mm

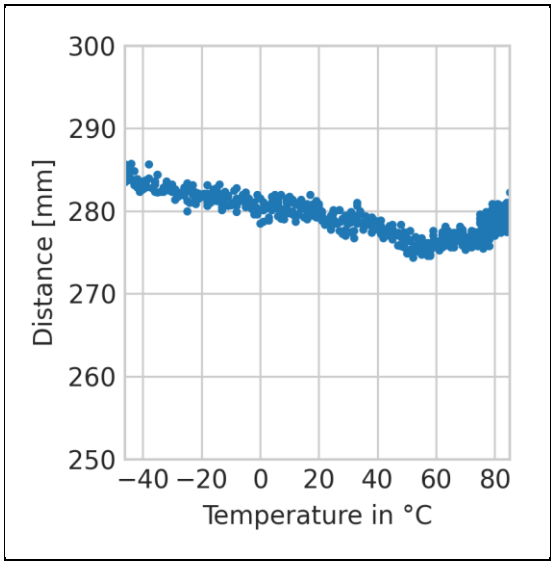


Figure 5: Confidence (SNR) vs. temperature
no ambient light, fixed target distance

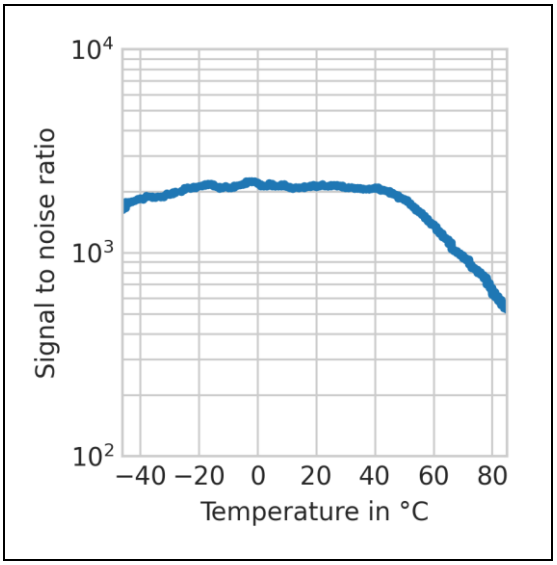


Figure 6: Linear scan, high accuracy 16x16 mode, pixel [8,8], 600k iterations, black:1800k, 350 lux FL light

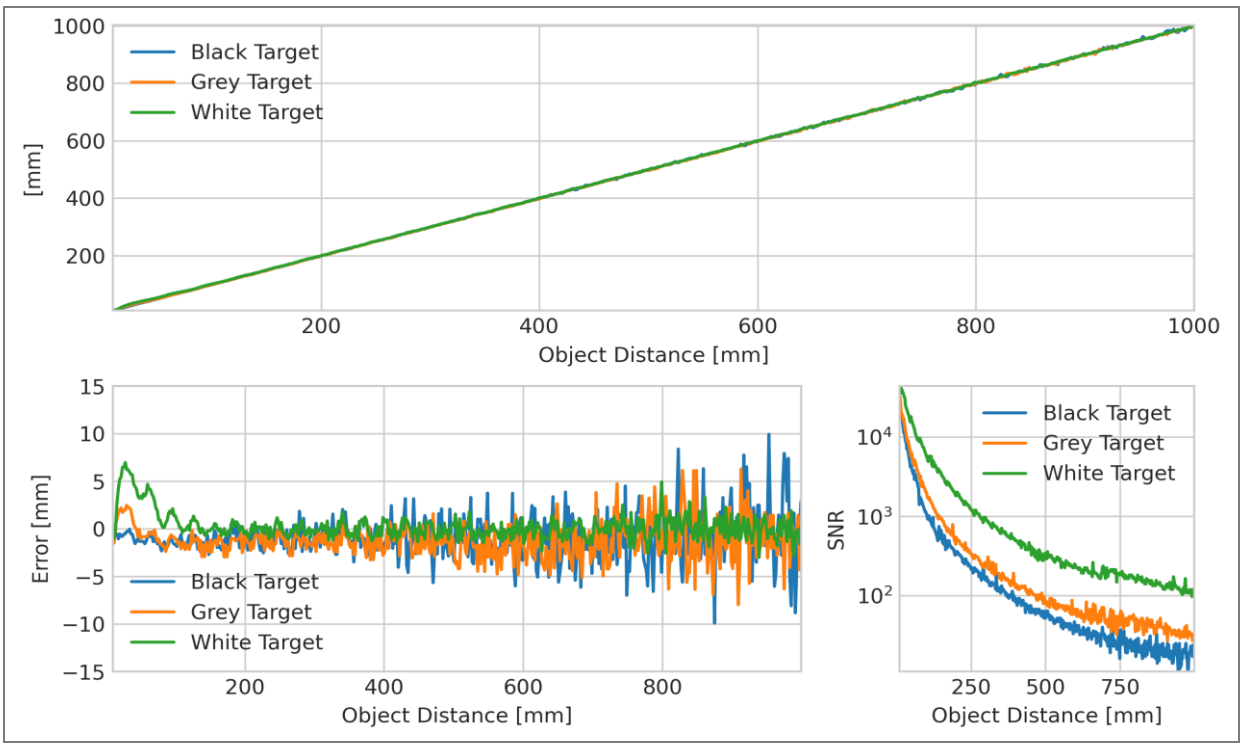


Figure 7: Linear scan, 10 mm – 5000 mm, 16x16 dual mode, 4000k/600k iterations, 350 lux FL lighting

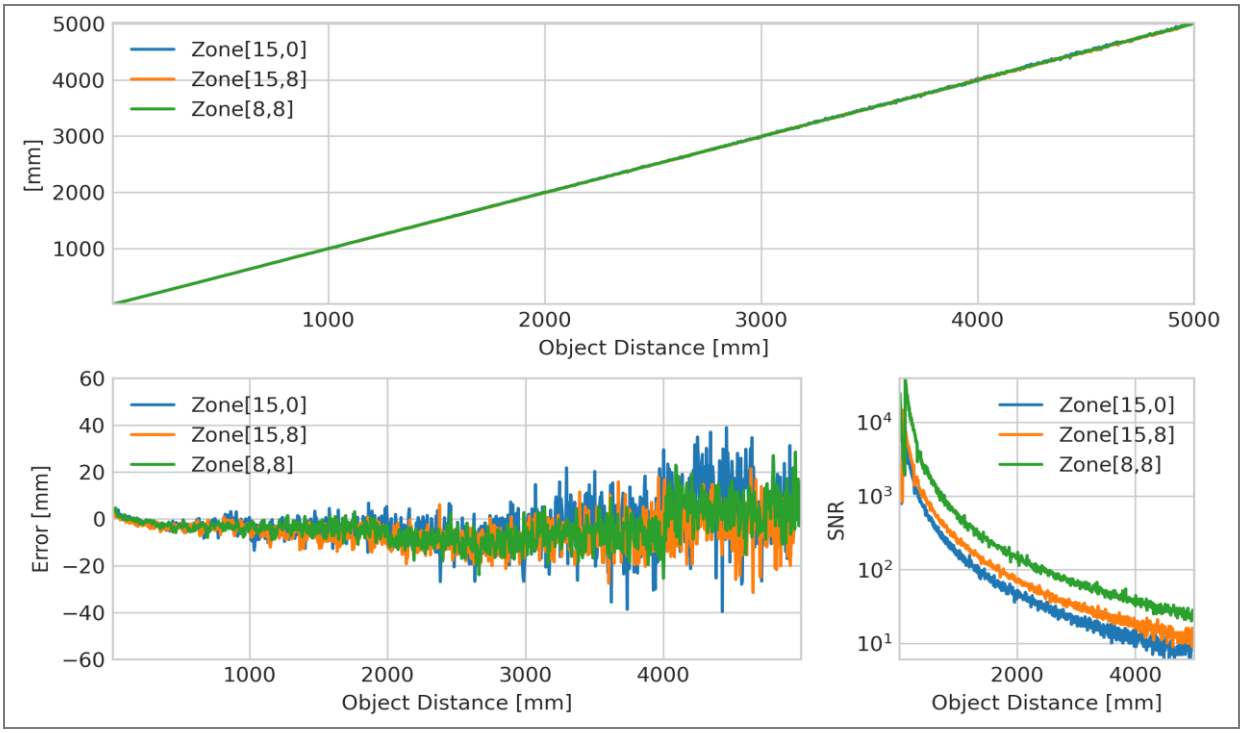


Figure 8: Grey target at 100 mm, distance of all pixels in 16x16 high accuracy mode - flatness of ams OSRAM factory calibration

98	99	98	98	98	99	98	96	99	99	98	98	99	99	99	100
97	98	98	98	99	100	98	98	99	97	98	97	99	98	98	101
98	97	98	98	97	98	99	98	99	99	98	99	98	98	99	99
100	99	100	99	98	100	99	100	100	99	100	99	99	100	98	99
100	100	98	99	98	99	100	98	100	100	98	98	99	99	99	99
100	99	99	100	98	97	99	97	98	99	100	97	98	98	100	98
99	99	100	100	100	99	100	97	99	98	100	98	99	100	99	98
99	99	98	100	97	99	98	97	98	100	97	98	98	99	99	99
100	99	100	100	97	98	98	99	99	99	97	99	98	99	99	100
98	99	100	98	100	100	99	100	98	99	99	100	99	98	100	99
98	98	100	99	101	99	99	98	98	100	99	98	99	99	98	101
100	100	99	99	99	100	99	99	99	100	99	99	99	99	100	99
99	99	98	99	100	99	99	99	99	100	100	99	100	100	99	100
99	100	98	99	100	99	99	99	100	100	99	99	98	99	100	100
101	98	98	98	98	98	98	98	100	101	99	100	99	100	98	98
100	99	100	100	100	100	98	99	100	100	100	98	99	100	99	100

7 Functional description

7.1 Functional working principle

The TMF8829 is a direct time-of-flight sensor that measures the time between sending a light pulse and receiving it. The TMF8829 internally generates histograms versus time for each measurement, which enables the device to measure ultra-short times and achieve a resolution of 0.25 mm, as 0.25 mm corresponds to only 1.7 ps.

An internal reference SPAD (single photon avalanche diode) with an associated TDC and histogram is used to determine the exact start time of each pulse. The reference SPAD is processed during both calibration and operation of the device and calibration is already performed at ams OSRAM. The calibration information is stored within each TMF8829, simplifying the use of the device. All processing is performed internally by the device.

The measurement SPADs are used to capture the measurement histograms; using the different measurement channels, the target distance is calculated.

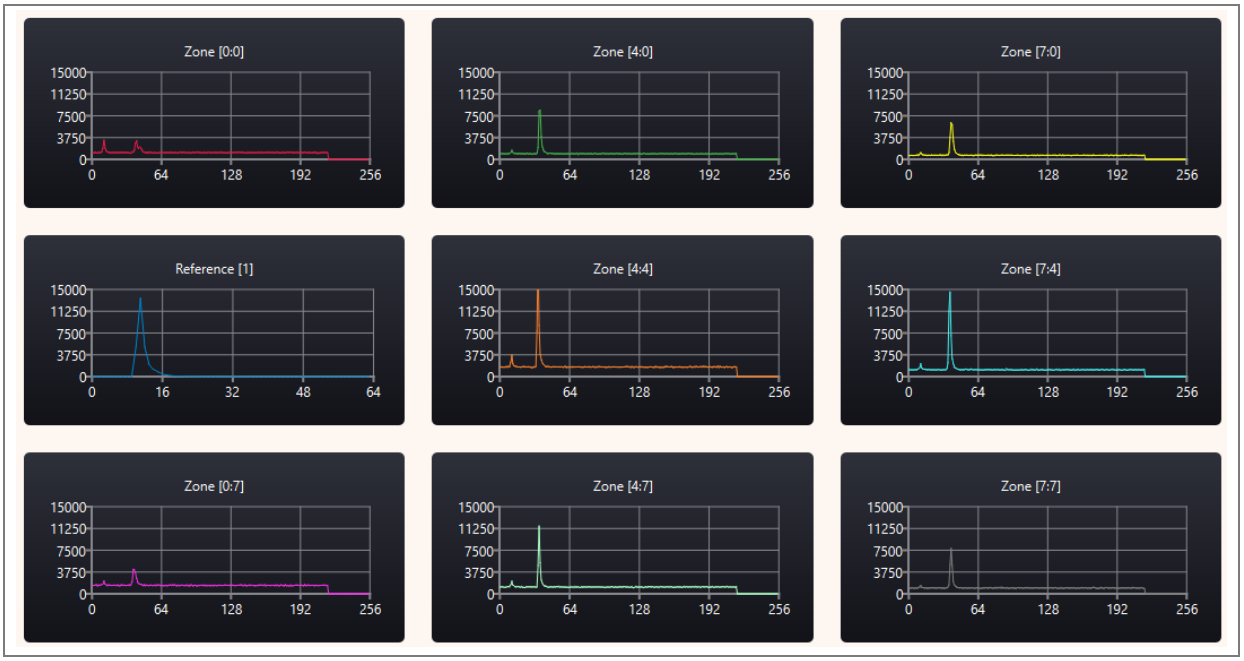
The histograms are generated by using a pulse train of VCSEL pulses defined by the iteration setting. These pulses are spread using an MLA (micro lens array) to illuminate the FOI (field of illumination). An object reflects these rays back to the TMF8829 receiver optics lens and onto the SPAD array. A TDC (time to digital converter) measures now the time from emission of these pulses to their arrival and accumulates the hits into bins inside a histogram.

All histograms can be processed inside the TMF8829 and/or readout through the I²C/I3C or SPI interface. It is recommended to readout the histograms only in I3C or SPI mode as I²C would limit the data rate.

Figure 9 shows a histogram obtained from TMF8829 in 8x8 high accuracy mode. The x-axis is scaled in bins, where the nominal bin size is 200 ps per bin and each TDC has 256 bins in this example[3]. The y-axis is scaled in counts represented by 24-bit values. The blue histogram on the left in the center shows the reference histogram and its peak marks the reference or zero distance – please note that this histogram shows only 64 bins. The other histograms are measured from different zones. A target at 70 cm is used to generate the peak around bin 30.

[3] Number of bins in a histogram and bin size are mode specific.

Figure 9: Histogram



The target detection algorithm running inside the TMF8829 uses the target peaks together with the reference channel to calculate zero distance using the dual core internal processor (2 x ARM M0+ ®). The algorithm calculates from bins to time, and converts to distance using speed of light.

7.2 Startup and operation of TMF8829

A typical startup sequence to run a continuous measurement is shown below.

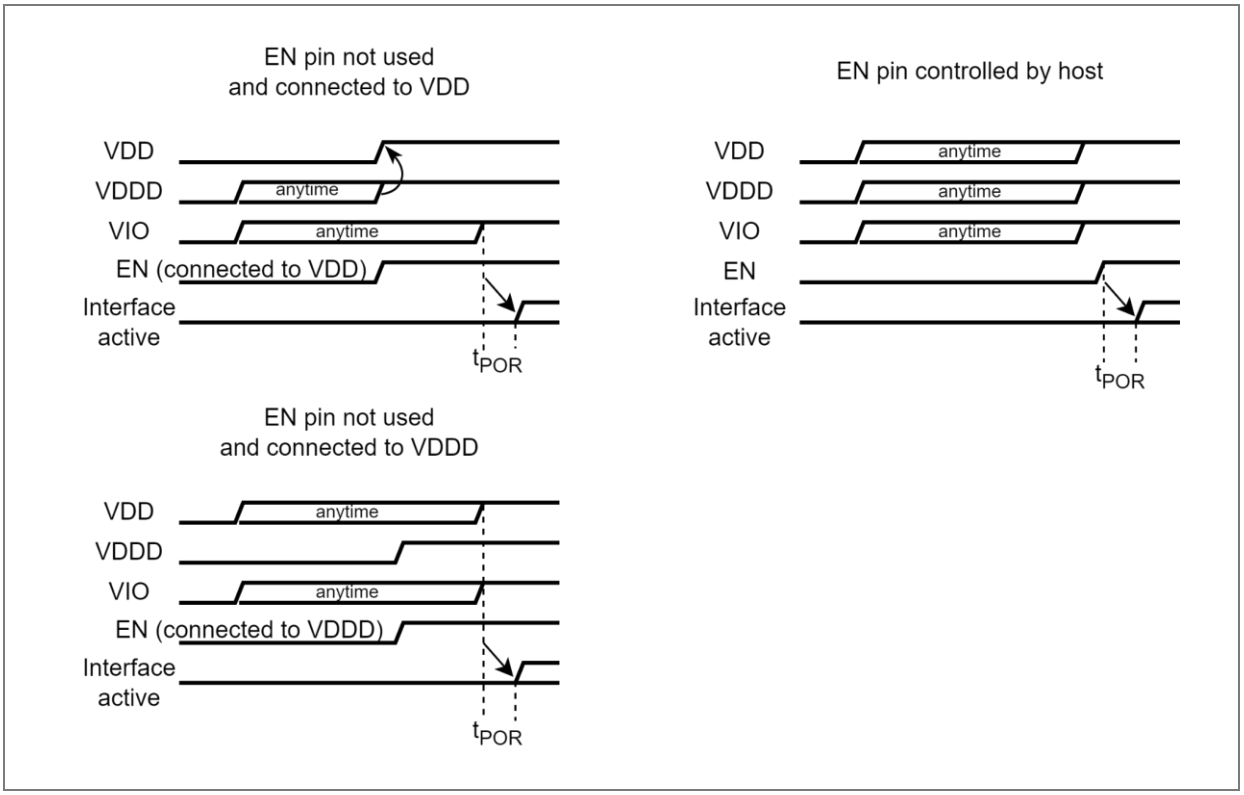
7.2.1 Hardware power sequencing

Ramp up supplies VDD, VDDD[4] and VIO:

Ensure VDDD starts before or with VDD. If not, connect EN to VDDD instead of VDD, unless the EN pin is controlled by the host. If EN is controlled by the cost, keep it at 0 and VDDD can start anytime.

If pin EN is controlled by the host[5], set EN = 1 after all supplies are all ramped up.

Figure 10: VDD, VDDD and VIO power sequencing



[4] The simplest configuration is to connect VDD = VDDD = EN to a 3.3V supply and have VIO connect to the I/O voltage.
[5] If EN is not used, connect it to VDD respectively VDDD, see above Figure 10.

7.2.2 Software sequence and power modes

See document “TMF8829 Host Driver Communication” for a detailed description of the individual item.

7.2.2.1 Booting and firmware download

1. Power on device by setting *pon=1*, *powerup_select*=0 and waiting for *cpu_ready*=1.
2. Select interface SPI and I²C/I3C – see section 7.9.
3. Download firmware (BL_CMD_W_FIFO_BOTH)
4. Boot loader command to start application (BL_CMD_START_RAM_APP)

The TMF8829 is now in active mode and consumes power as defined by I_{ACTIVE}.

7.2.2.2 Operation cycle

1. Use pre-configuration commands to select mode from section 7.3.
2. Change any other parameters as needed by the application (example *iterations* or *period*).
3. Execute command CMD_WRITE_PAGE_AND_MEASURE by writing 20 (decimal) to register *cmd_stat* and wait for *cmd_stat* = STAT_OK to start the actual measurement.
4. Repeat
   a. Wait for interrupt or poll INT_STATUS
   b. Clear interrupt by writing to register INT_STATUS
   c. Readout FIFO – always start reading from register FIFOSTATUS onwards. For interpretation of the results, see “TMF8829 Host Driver Communication”; there are examples in this guide for typical use cases.
5. Execute command CMD_STOP by writing 255 (decimal) to register *cmd_stat* and wait for *cmd_stat* = STAT_OK.
6. Enter standby mode by setting *poff=1* and wait for *cpu_ready*=0.

The TMF8829 is now in standby mode and consumes minimum power $I_{STANDBY}$.

7. To wakeup the TMF8829 from standby mode to enter active mode, set *pon=1*, *powerup_select*=2 and wait for *cpu_ready*=1 – then continue directly from item (1) of this list as no firmware download is needed.

7.3 Distance and operating modes

The TMF8829 has several pre-configured operating modes that optimize device performance. It is strongly recommended to use these modes rather than setting individual registers. Guaranteed performance is achieved only by using these pre-sets.

To load these presents, follow this sequence:

- *cmd_stat* = CMD_LOAD_CFG_8X8 (respectively selected mode) and wait for *cmd_stat* = STAT_OK

Table 6: TMF8829 pre-configured operating modes

Command to load used for register *cmd_stat*	Recommended for	Maximum range	Programs following registers
CMD_LOAD_CFG_8X8	Default 8x8 mode	5.7 m	*fp_mode* = FP_8x8A, *pulse_width* = 1300 ps, current = 93, *vcsel_period* = 249, *histogram_bins* = 218, *bin_shift* = *ref_bin_shift* = 2, *select* = 1, *peak_detect_start* = 40
CMD_LOAD_CFG_8X8_ LONG_RANGE	Mode with longest range	11 m	*fp_mode* = FP_8x8A, *pulse_width* = 1300 ps, current = 51, *vcsel_period* = 449, *histogram_bins* = 418, *bin_shift* = *ref_bin_shift* = 2, *select* = 1, *peak_detect_start* = 40
CMD_LOAD_CFG_8X8_ HIGH_ACCURACY	Emphasizes accuracy in short range	5.7 m	*fp_mode* = FP_8x8A, *pulse_width* = 330 ps, current = 23, *vcsel_period* = 249, *histogram_bins* = 218, *bin_shift* = *ref_bin_shift* = 0, *select* = 2, *peak_detect_start* = 25
CMD_LOAD_CFG_16X16	Default 16x16 mode	5.7 m	*fp_mode* = FP_16x16, *pulse_width* = 1300 ps, current = 93, *vcsel_period* = 249, *histogram_bins* = 218, *bin_shift* = *ref_bin_shift* = 2, *select* = 1, *peak_detect_start* = 40
CMD_LOAD_CFG_16X16_ HIGH_ACCURACY	Emphasizes accuracy in short range	1.4 m	*fp_mode* = FP_16x16, *pulse_width* = 330 ps, current = 23, *vcsel_period* = 249, *histogram_bins* = 64, *bin_shift* = *ref_bin_shift* = 0, *select* = 2, *peak_detect_start* = 25
CMD_LOAD_CFG_32X32	Default 32x32 mode	5.7 m	*fp_mode* = FP_32x32, *pulse_width* = 1300 ps, current = 93, *vcsel_period* = 249, *histogram_bins* = 218, *bin_shift* = *ref_bin_shift* = 2, *select* = 1, *peak_detect_start* = 40
CMD_LOAD_CFG_32X32_ HIGH_ACCURACY	Emphasizes accuracy in short range	1.4 m	*fp_mode* = FP_32x32, *pulse_width* = 330 ps, current = 23, *vcsel_period* = 249, *histogram_bins* = 64, *bin_shift* = *ref_bin_shift* = 0, *select* = 2, *peak_detect_start* = 25
CMD_LOAD_CFG_48X32	Default 48x32 mode	5.7 m	*fp_mode* = FP_48x32, *pulse_width* = 1300 ps, current = 93, *vcsel_period* = 249, *histogram_bins* = 218, *bin_shift* = *ref_bin_shift* = 2, *select* = 1, *peak_detect_start* = 40
CMD_LOAD_CFG_48X32_ HIGH_ACCURACY	Emphasizes accuracy in short range	1.4 m	*fp_mode* = FP_48x32, *pulse_width* = 330 ps, current = 23, *vcsel_period* = 249, *histogram_bins* = 64, *bin_shift* = *ref_bin_shift* = 0, *select* = 2, *peak_detect_start* = 25

7.3.1 Dual mode

If enabled by register *dual_mode*=1 respectively *dual_mode*=2 for CMD_LOAD_CFG_8X8_LONG_RANGE, this mode continuously alternates between the default mode (e.g. 8x8 mode - CMD_LOAD_CFG_8X8) and the associated high accuracy mode (for default 8x8 mode this is high accuracy 8x8 mode - CMD_LOAD_CFG_8X8_HIGH_ACCURACY). The distance detection algorithm is executed, and both results are combined and reported to the host as one combined measurement result.

In this mode, the number of iterations for default mode is set by register *iterations* and for the high performance mode, *high_accuracy_iterations*. The configuration always uses the setting defined by TMF8829 pre-configured operating modes according to Table 6.

This operating mode enables the TMF8829 to cover its full range with one setting, from 10 mm up to 11000 mm. To enable this mode, use one default mode (e.g. CMD_LOAD_CFG_8X8) and set register *dual_mode*=1 respectively 2.

The following modes are combined for dual mode:

Table 7: Modes combined in dual mode

dual_mode **setting**	**Main mode used – use this for programming** **Iteration setting used: *iterations***	**High accuracy mode used** **Iterations setting used: *high_accuracy_iterations***
0	Mode defined as shown in section 7.3; no dual mode	Not used
1	CMD_LOAD_CFG_8X8	CMD_LOAD_CFG_8X8_HIGH_ACCURACY
2	CMD_LOAD_CFG_8X8_LONG_RANGE	CMD_LOAD_CFG_8X8_HIGH_ACCURACY
1	CMD_LOAD_CFG_16X16	CMD_LOAD_CFG_16X16_HIGH_ACCURACY
1	CMD_LOAD_CFG_32X32	CMD_LOAD_CFG_32X32_HIGH_ACCURACY
1	CMD_LOAD_CFG_48X32	CMD_LOAD_CFG_48X32_HIGH_ACCURACY

7.3.2 Motion detection

To reduce the number of interrupts sent to the host, the TMF8829 can do motion detection. To program this motion detection, use following registers:

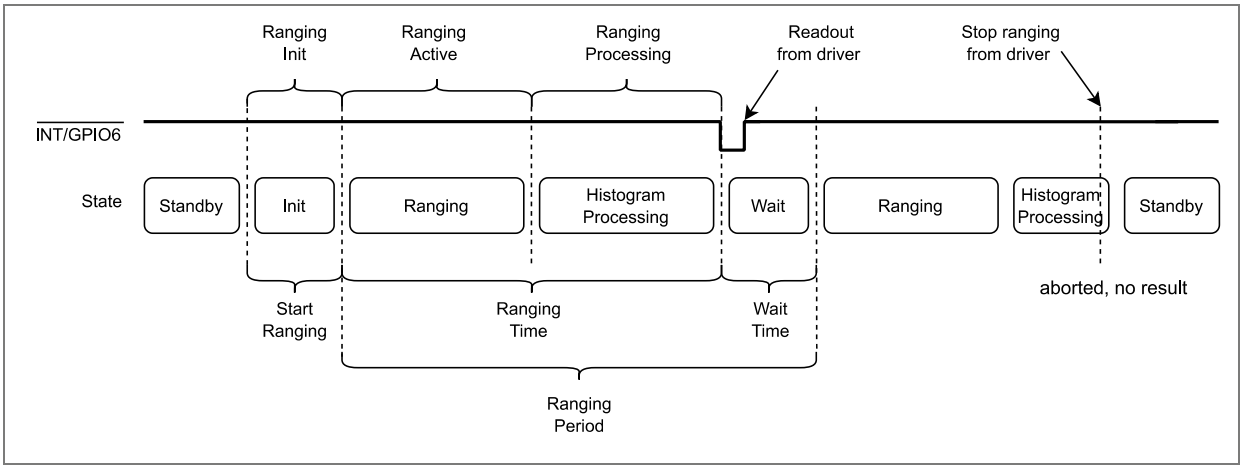
Table 8: Motion detection registers

Register	Purpose
int1	Result interrupt to signal motion detection
int1_enab	Enable assertion on INT on detected motion
post_processing	Enable for motion detection (set to MOTION or MOTION_ALWAYS_RESULTS) For persistence mode, set to PERSISTENCE
int_persistence	Set to 1 or higher
motion_distance	Distance in UQ2 [0.25 mm], which is considered as motion
detect_snr, release_snr	Detect and release SNR motion threshold
motion_adjacent	Number of adjacent pixels with motion to be considered as motion detected
int_zone_mask	Interrupt masked on zone A 1 means this zone can trigger an interrupt, lsb is zone 0
int_threshold_low	Interrupt threshold for distance – only zones >= *int_threshold_low* will trigger an interrupt
int_threshold_high	Interrupt threshold for distance – only zones <= *int_threshold_high* will trigger an interrupt
mp_top_x, mp_top_y, mp_bottom_x, mp_bottom_y	Restrict the area in which objects are recorded to the macro-pixels defined by rectangular mp_top_x/mp_top_y to mp_bottom_x/mp_bottom_y (full FOV has 16x16 macro-pixels) Set register *spad_cropping*=1 to disable SPADs which are outside the cropped area.

7.4 Ranging acquisition timing

The typical ranging acquisition follows this timing diagram:

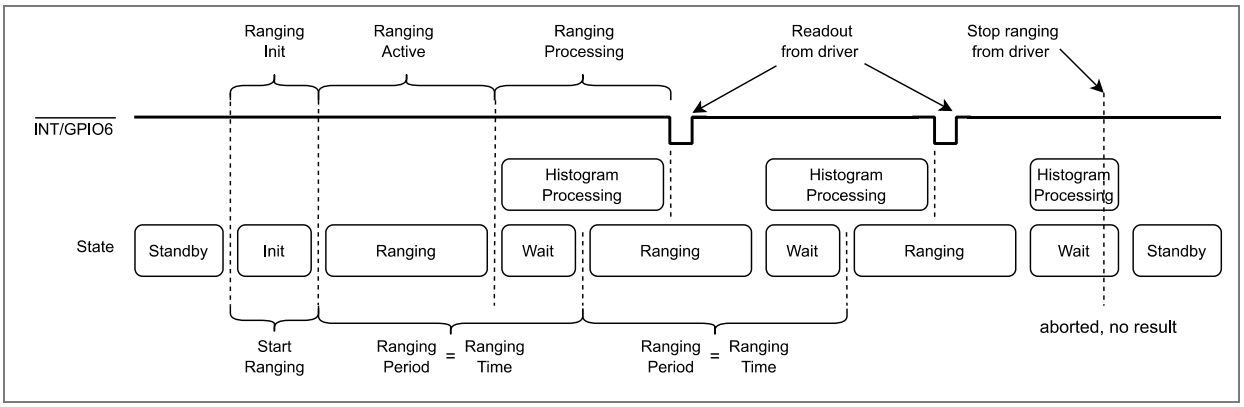
Figure 11: Timing diagram for ranging period > ranging active + histogram processing



Ranging period is defined by register *period* and the wait time is adjusted accordingly. Ranging active is defined by the number of iterations (register *iterations*) configured and the VCSEL clock frequency (register *vcsel_period*).

If the ranging period is chosen shorter than the combined time of ranging active and histogram processing, the TMF8829 automatically runs histogram processing in parallel to ranging active:

Figure 12: Timing diagram for ranging period < ranging active + histogram processing



If the ranging time gets longer than *period*, wait time is omitted. In this case, the ranging period is equal to ranging active and *period* is ignored.

7.5 Algorithm performance

The following section only applies for in-application automatic oscillator clock skew correction using one of the reference drivers.

The TMF8829 is embedded in the application using a 0.17 mm airgap and 0.5 mm thick glass. A rubber boot or additional mask on the opaque ink is implemented according to TMF8829 optical design guide (ODG).

7.5.1 Customer factory calibration

The TMF8829 are already factory calibrated in ams OSRAM production site and there is **no customer factory calibration required**. The calibration is performed for 8x8 and 16x16 modes described in section 7.3. For 16x16 mode, 6 SPADs are used per zone and for 8x8 4*6 SPADs are used – this implies *spad_select* = 63.

For 48x32 and 32x32, where only one or two SPADs are used per zone, the same calibration from 16x16 mode with 6 SPADs is re-used, therefore expect slightly more offset errors in these modes.

For an application, which needs even higher accuracy in 48x32 or 32x32 modes, an additional customer device individual calibration is recommended. An example is to measure a grey card at an exact known distance (e.g. 20 cm) and store the measured offsets on the host. Subtract these offsets from the measurements upon operation.

7.5.2 Algorithm timings and performance parameters

The TMF8829 can adjust the number of iterations and detection threshold using registers *iterations* and *confidence_threshold* which can have a minimum value of 4. If you are concerned about false positive detection, increase *confidence_threshold* to 6.

The different timings are shown in section 5.1 on page 16 and described in section 7.4.

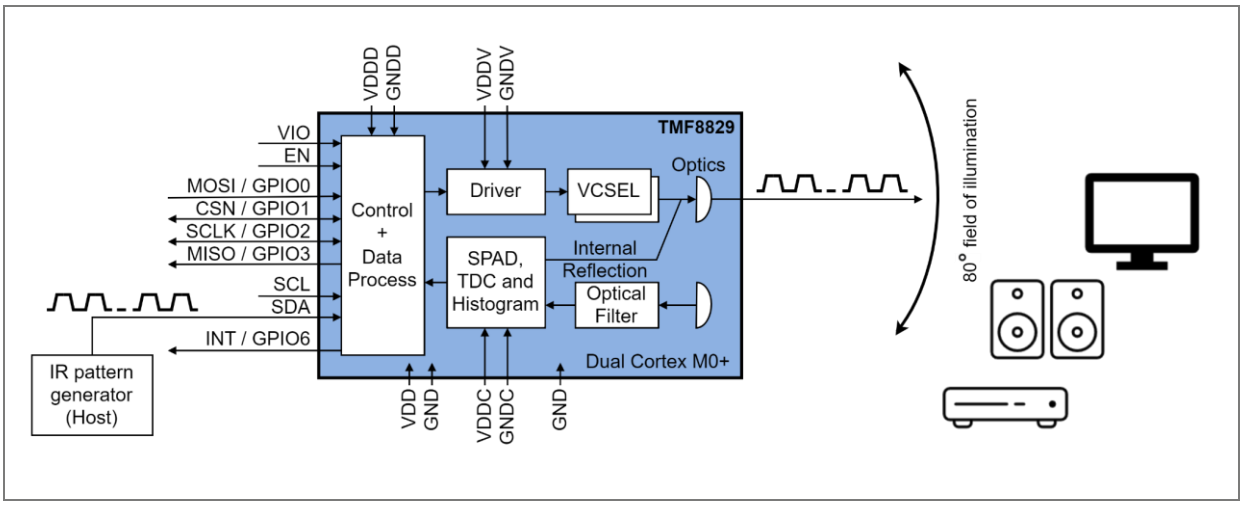
The algorithm reports distance information of up to four objects in 0.25 mm steps. Using the timings described above, the performance as shown in section 5.1 on page 16 is achieved.

7.6 IR remote operation

The two TMF8829 VCSELs can operate simultaneously controlled by any of the GPIO pins. This allows implementing an IR remote emission pattern and controlling any devices like a TV set, radio or air condition device.

An example, where SDA is used as control input, is shown in Figure 13:

Figure 13: IR remote functionality



To enable this mode, initialize the device by booting and downloading firmware according to section 7.2.2.1 to enter active mode[6], and then run following commands – in this example SDA is used as input which assumes that the TMF8829 is controlled by SPI:

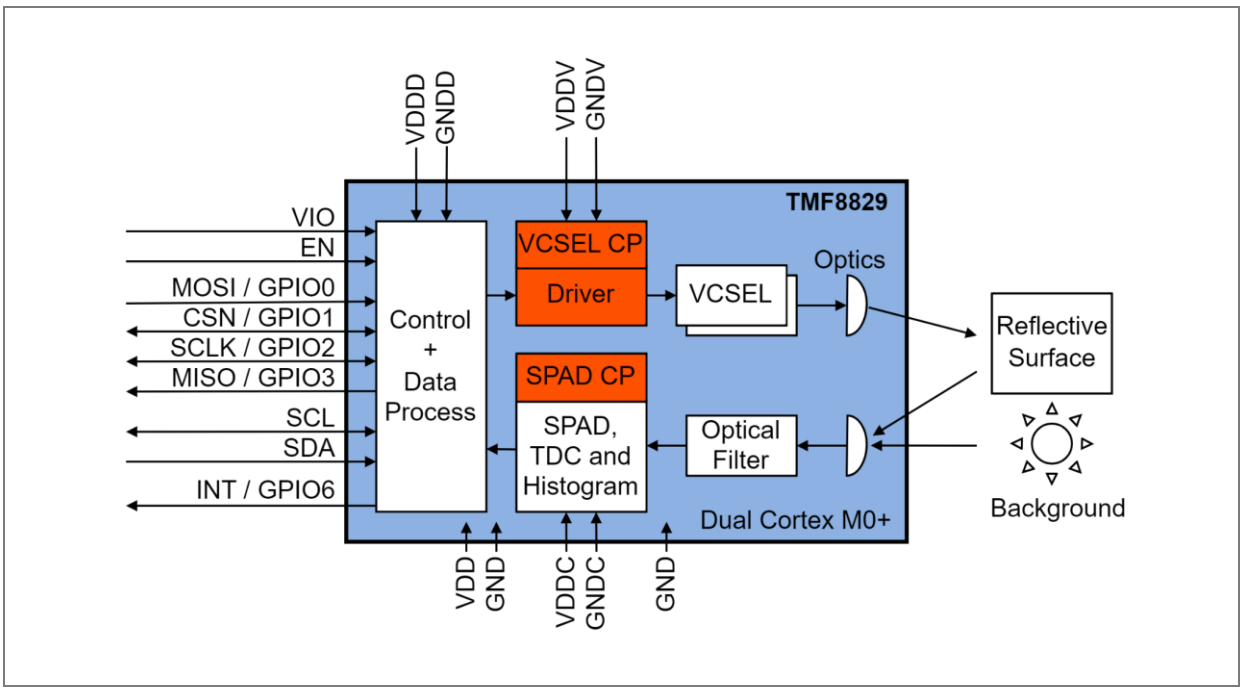
- Load configuration page: *cmd_stat* = CMD_LOAD_CONFIG_PAGE and wait for *cmd_stat* = STAT_OK
- Set *gpio5_func* = 0 and register TMF8829_CFG_GPIO_5, *gpio5* = 1 (IR mode)
- Write configuration page: *cmd_stat* = CMD_WRITE_PAGE and wait for *cmd_stat* = STAT_OK

To stop IR mode, use the same sequence, but set *gpio5* = 0 (tristate).

[6] If a measurement is running, stop this measurement first (CMD_STOP) before continuing.

7.7 EMC performance enhancements

Figure 14: Blocks with EMC performance enhancements highlighted



The TMF8829 internally uses charge pumps (VCSEL CP and SPAD CP) for power management. These blocks are switching capacitors at high frequency to obtain higher voltages and therefore emit EMC noise. To attenuate this effect, the TMF8829 allows to spread this EMC emission much more smoothly over a wider frequency range.

7.7.1 VCSEL and SPAD charge pump spread spectrum

The recommended settings for the two charge pumps are shown in Table 9:

Table 9: Spread spectrum configurations

Spread spectrum configured by	Affected block	Notes
Register TMF8829_HV_CP: *spr_spec_amp*: Set to 15 *spr_spec_cfg*: Set to 1	SPAD charge pump	No side effects other than reducing EMC noise
Register TMF8829_VCDRV_CP: *vc_spr_spec_amp*: Set to 15 *vc_spr_spec_cfg*: Set to 1	VCSEL charge pump	No side effects other than reducing EMC noise

7.7.2 Dithering to reject aliased objects and improve EMC

The VCSEL driver setting allows EMC reduction but also reduces the effect of aliased objects from long distance.

The TMF8829 support dithering of the VCSEL clock to avoid aliasing of objects at large distance to much closer objects. The aliasing happens exactly at the multiple of the VCSEL clock frequency. For the *vcsel_period* default setting of 19.72 MHz VCSEL clock, an object at 7.6m is aliased to 0m.

To avoid this aliasing, the registers *dither_increment* and *dither_rounds* can be used.

Table 10: Spread spectrum configurations

Dithering configured by	Affected block	Notes
Register TMF8829_CFG_DITHER Valid range: Set both registers to 0 for no dithering (default) *dither_rounds*: Set to 7 *dither_increment*: Set to 7	VCSEL driver	Reduce EMC noise and attenuate aliased objects but reduce VCSEL clock frequency and increase ranging active time.

The average *vcsel_period* is increased to:

Equation 1:

$$vcsel\_period + \frac{dither\_rounds * dither\_increment}{2}$$

Example:

dither_rounds = *dither_increments* = 7

vcsel_period = 249

The VCSEL frequency is reduced from 19.72 MHz without dithering to 17.95 MHz with dithering and ranging active time is increased by ~9% if the same iteration setting is used.

7.8 Typical optical characteristics

7.8.1 VCSEL

Internal protection ensures that even with a single point of failure the TMF8829 will stay Class 1 Laser Eye Safe.

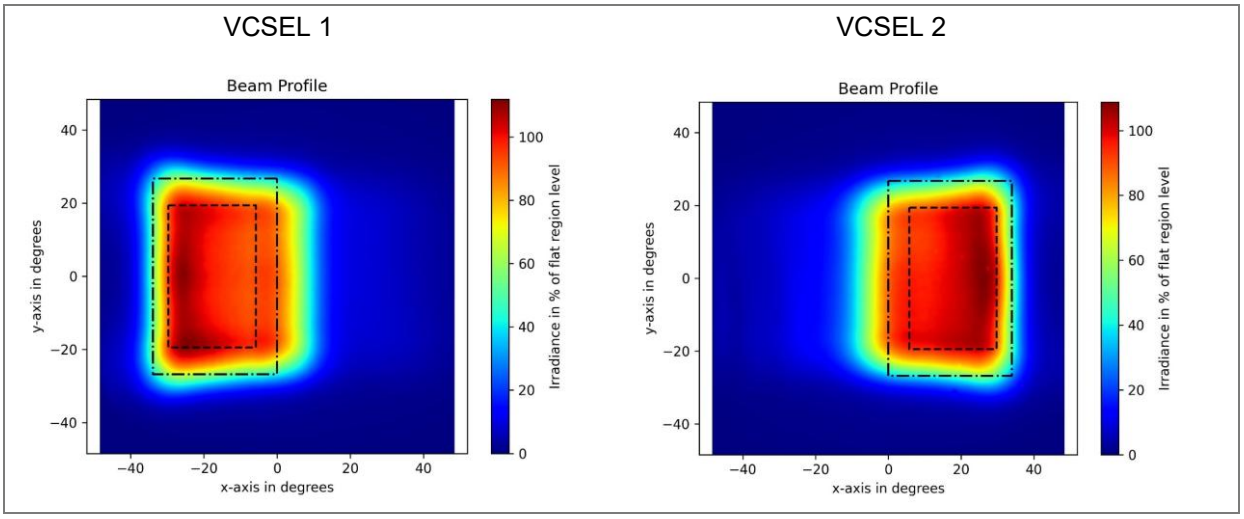
- Laser Safety — Class 1
- Peak emission wavelength — 940 nm
- VCSEL Pulse Rep Rate — 50.7 ns ~ 19.72 MHz
  Exception: CMD_LOAD_CFG_8X8_LONG_RANGE
  91.44 ns ~ 10.94 MHz

If dithering is enabled, the VCSEL frequency is reduced – see section 7.7.2.

7.8.2 Field of illumination (FOI)

The TMF8829 use two internal VCSELs and sequential illumination with the FOI shown in Figure 15. Only in IR-remote operating mode, see section 7.6, both VCSEL operate simultaneously.

Figure 15: VCSEL FOI



The typical combined FOI is:

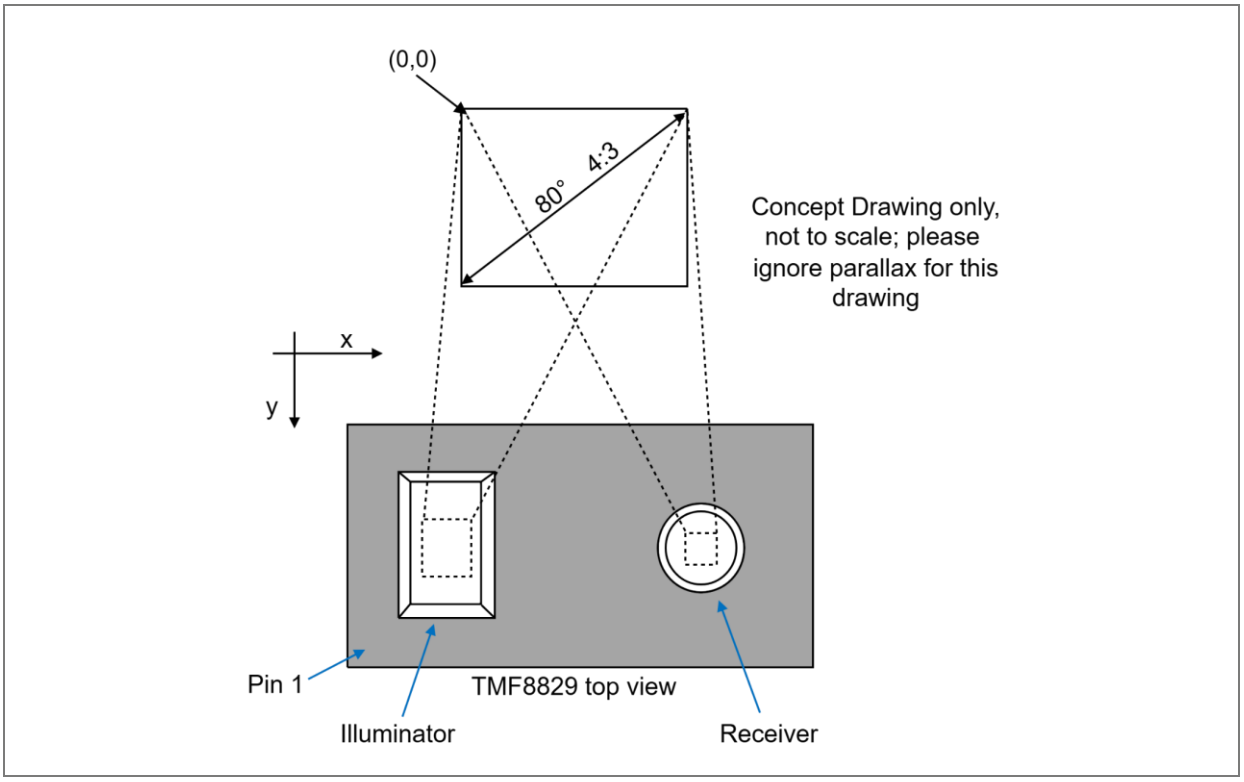
- FWHM, x-direction: 67.8 degrees
- FWHM, y-direction[7]: 53.5 degrees

7.8.3 Field of view (FOV)

The field of view of the receiver matches very closely the FOI and is defined by FOV_X and FOV_Y.

[7] Measured through the center of each VCSELs FOI.

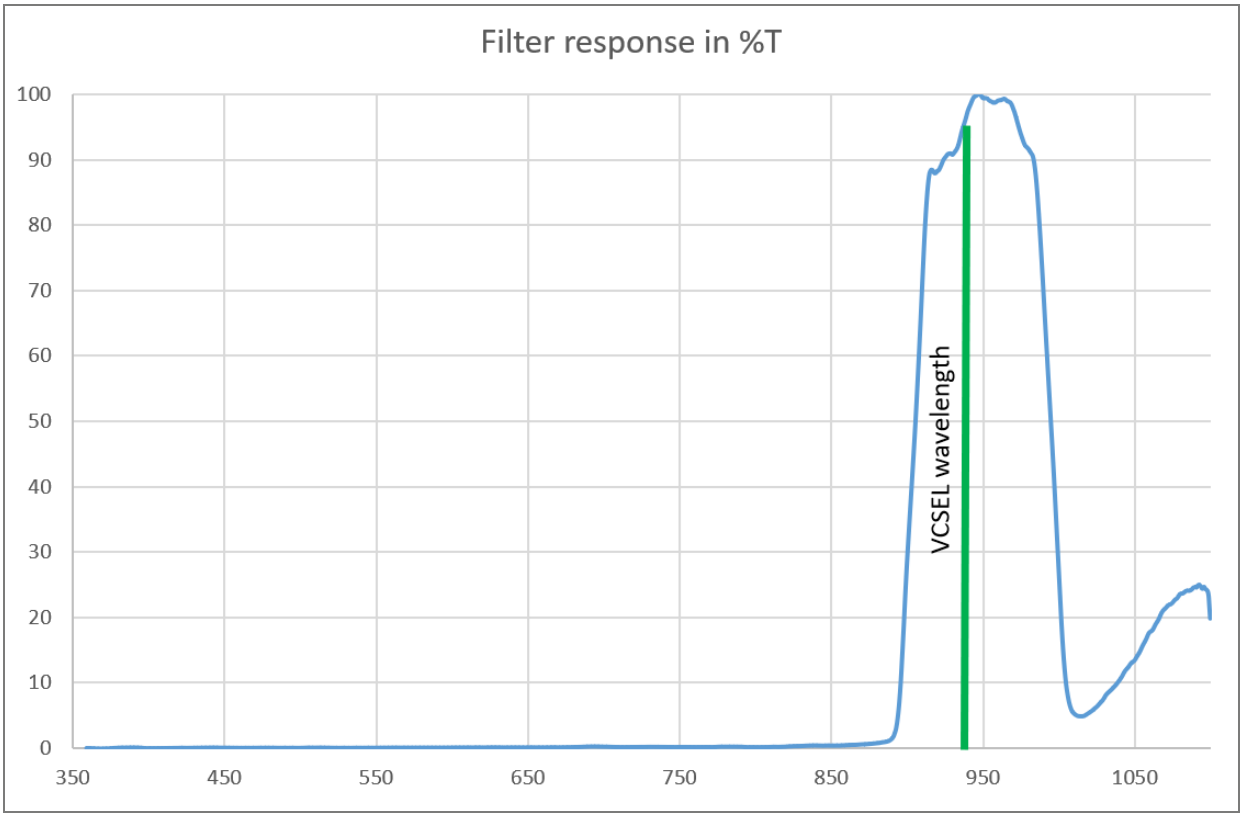
Figure 16: Device orientation – pixel (0,0) is upper left corner



7.8.4 Optical filter characteristics

The TMF8829 has a customized interference filter integrated in the module. The filter response (filter only) is shown in this graph:

Figure 17: Filter response without SPADs



Information:

Since SPADs have largely reduced sensitivity above 1000nm, higher transmissivity of the optical filter there is acceptable and has minimal impact on application performance.

7.9 Interface mode selection

After startup (see section 7.2.2.1), the system is in active mode, the oscillator is started, the PLL is started and the CPU starts execution of the internal firmware at 158.4 MHz.

Both interfaces, SPI and I²C/I3C are enabled and wait for the first transaction at either interface. The first command (bootloader command BL_CMD_SPI_OFF or BL_CMD_I2C_OFF) shall define the interface, which enables only the chosen interface.

Information:

The TMF8829 will not enter standby mode before an interface is chosen. To enter standby mode, set then *pon*=0.

7.10 I²C/I3C interface

The device provides I3C serial communication interface with clock speed up to 12.5 MHz, which improves the features of the I²C interface and preserves backward compatibility of Legacy I²C messaging. Read and Write transactions comply with the MIPI I3C specification v1.0 set by MIPI Alliance. For a complete description of the I3C protocol, please review the MIPI I3C specification.

The device does not have to know whether it is on a Legacy I²C Bus or an I3C Bus. The device has a Legacy I²C Static Address and participates in using that Address up until (and if) it is assigned a Dynamic Address by using either the SETDASA CCC command or the ENTDAA CCC command. Once assigned to a Dynamic Address, the device operates as an I3C Slave, and that Dynamic Address shall be used in all subsequent transactions on the I3C Bus until and unless the Master changes the Dynamic Address. The way for the Master to change the Device's Dynamic Address is by using either the RSTDA CCC command or the SETNEWDA CCC command. Before being assigned a Dynamic Address, the device operates as an I²C device with added features of acknowledging the I3C Broadcast Address (7'h7E) after START condition and processing the CCCs ENTDAA and SETDASA as appropriate.

When on an I3C bus, the device is initialized as I3C slave. After the Dynamic Address Assignment, SDR Mode is selected for private messaging. SDR Mode is also used to enter other Modes, sub-Modes, and states and for built-in features such as Common Commands Codes (CCCs), In-Band Interrupts (IBI), and transition from I²C to I3C by assignment of a Dynamic Address. The device can coexist on the same I3C Bus with many I3C devices and I²C slave devices. For the procedures and conditions that I3C shares with I²C, it closely follows the definition in the I²C specification.

When on an I²C bus, the device automatically detects and operates as Legacy I²C slave, supporting Standard-mode, Fast-mode and Fast-mode Plus (1 MHz). The protocol complies with the I²C specification set by Philips (now NXP). For a complete description of the I²C specification, please review UM10204, I²C bus specification and user manual.

The timing parameters are specified by design and characterization and are not production tested unless otherwise noted. All parameters are measured with V_{DD} = 3.3 V and T_A = 25°C unless otherwise noted.

Figure 18: Bus timing diagram for I²C communications of TMF8829

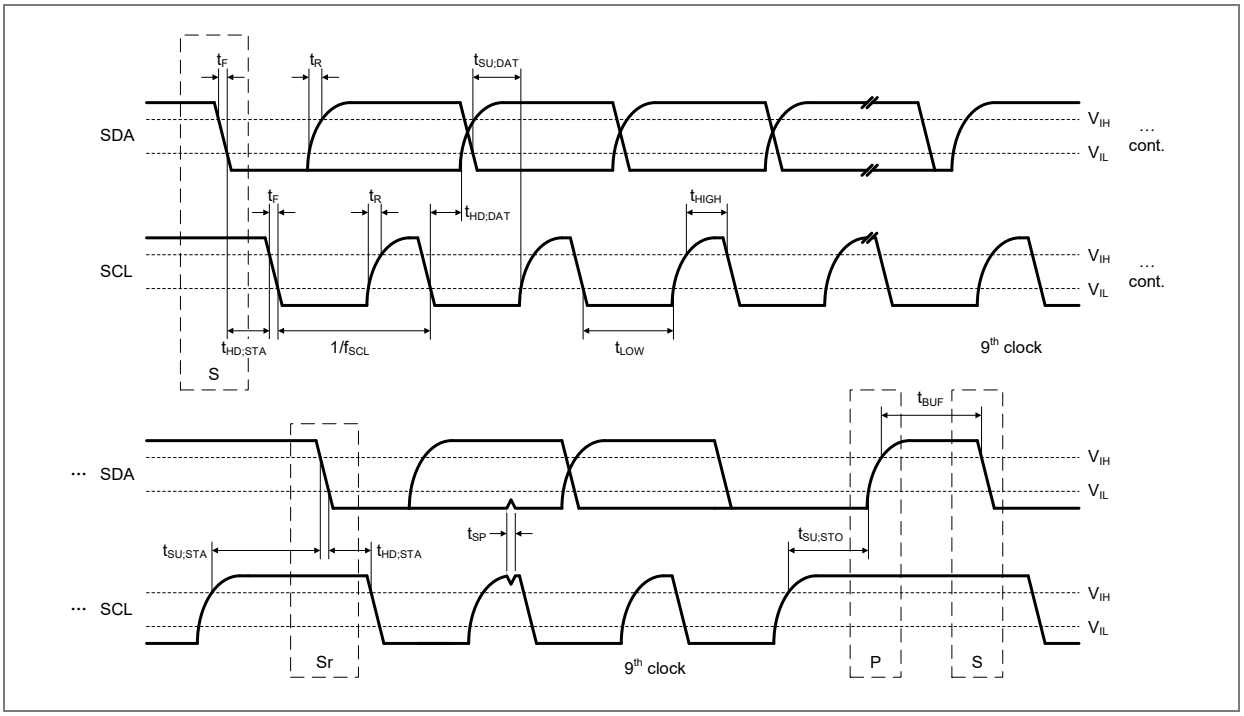
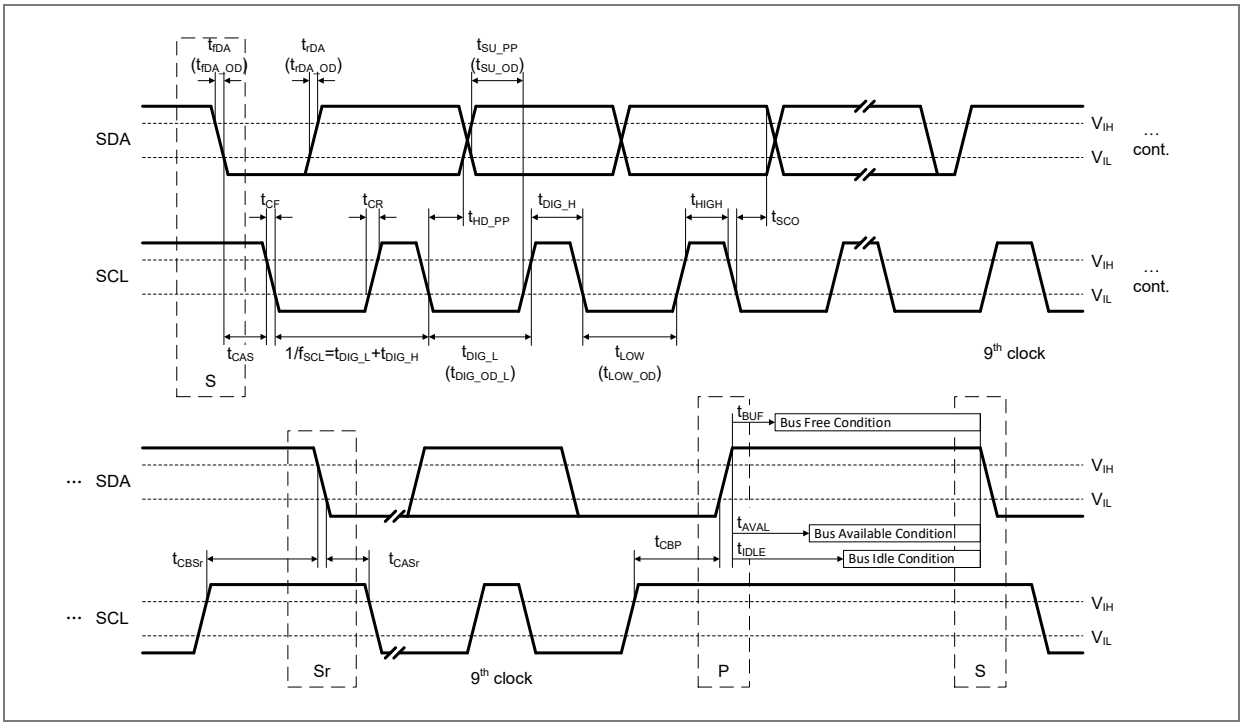


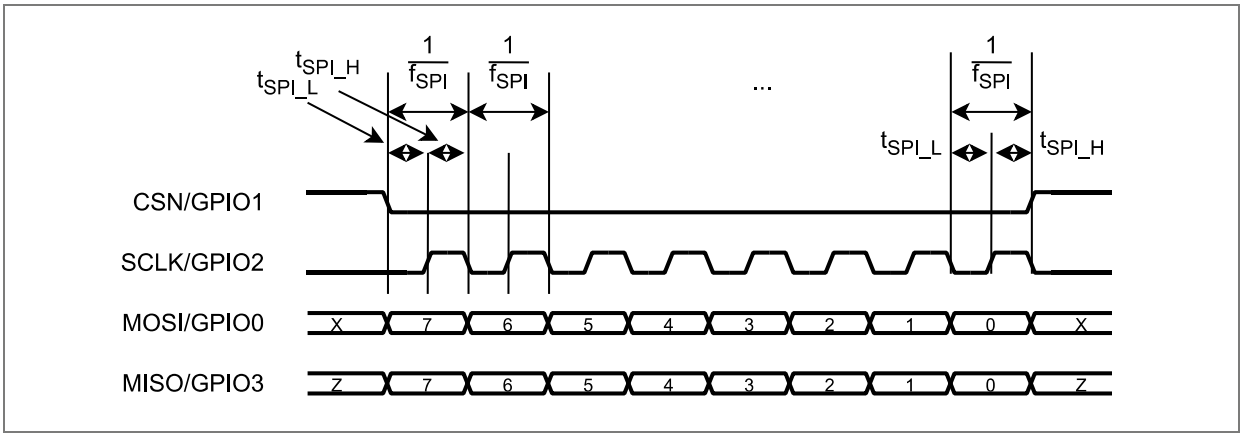
Figure 19: Bus timing diagram for I3C communications of TMF8829



7.11 SPI interface

The TMF8829 is using SPI mode 0, which is defined by CPOL (clock polarity) = 0 and CPHA (clock phase) = 0, see Serial Peripheral Interface. The following waveform shows a general SPI transaction including timings using the mode – 8 bits data read/write are used for explanation only:

Figure 20: SPI interface communication and timings



Data is shifted out on the falling edge of SCLK/GPIO2 and when CSN/GPIO1 is asserted.

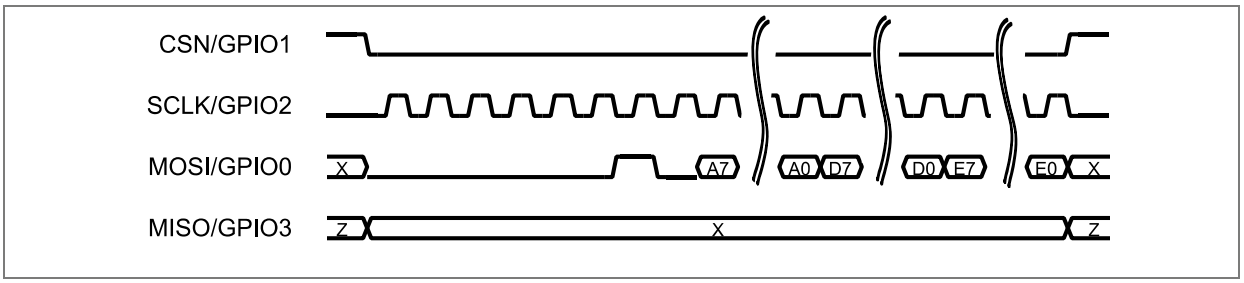
Data is sampled on the rising edge of SCLK/GPIO2.

7.11.1 SPI write transaction

A write consists of at least three bytes on the bus, the first one being the command code (“write”=0x02), second one being the 8-bit register address (equivalent to the I²C/I3C address), followed by at least one data byte. Like with I²C/I3C, the addresses are automatically incremented for each further byte that is transmitted, except for address 0xff which is the FIFO address. Accesses to address 0xff go into the FIFO, the actual RAM address at which the FIFO gets stored depends on the FIFO configuration and FIFO pointer.

Example: Writing to two bytes (values D and E) to two consecutive registers A and A+1. The write command code is 0x02:

Figure 21: SPI write

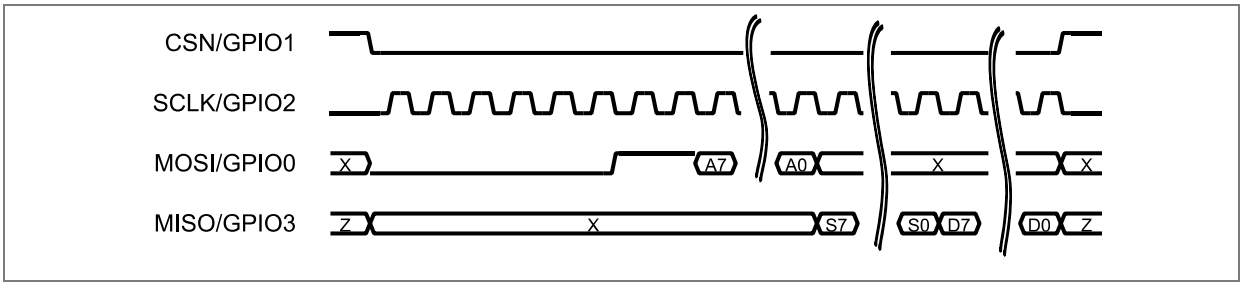


7.11.2 SPI read transaction

A SPI read consists of at least four bytes on the bus, the first one being the command code (“read”=0x03), second address, followed by a dummy byte, followed by the data bytes. The data bytes are presented by the device on the MISO output pin.

Example: Reading to one byte (value D) from register A. The read command code is 0x03. Value S is the status/dummy byte and can be ignored.

Figure 22: SPI read



8 Register description

8.1 Registers independent on *cid_rid*

8.1.1 TMF8829_APP_ID register (Address 0x00)

Table 11: TMF8829_APP_ID register

Addr: 0x00		TMF8829_APP_ID		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*appid*	0	RO	Currently running application: 0x01 RAM patch 0x80 bootloader

8.1.2 TMF8829_MAJOR register (Address 0x01)

Table 12: TMF8829_MAJOR register

Addr: 0x01		TMF8829_MAJOR		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*major*	0	RO	Application major revision

8.1.3 TMF8829_MINOR register (Address 0x02)

Table 13: TMF8829_MINOR register

Addr: 0x02		TMF8829_MINOR		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*minor*	0	RO	Application minor revision

8.1.4 TMF8829_CMD_STAT register (Address 0x08)

Table 14: TMF8829_CMD_STAT register

Addr: 0x08		TMF8829_CMD_STAT		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*cmd_stat*	0	RW	**Write**: Host writes to this register a command. Commands have the value range 0x10..0xFF and are described in Table 15. **Read**: TMF8829 writes to this register to confirm a command. This is the STATUS of the device as described in Table 16.

Following tables show the possible commands and status of TMF8829:

Table 15: Commands for TMF8829 – write to register 0x08 / cmd_stat

Code (decimal)	Symbol	Function
16	CMD_MEASURE	Measure: Start a cyclic measurement according to the configuration
17	CMD_CLEAR_STATUS	Clear Status: Clear all status registers (note that a new measurement clears them too)
20	CMD_WRITE_PAGE_AND_MEASURE	Write configuration page (whatever page has been loaded to registers 0x20 and following will be written to the device) and start a measurement, if no error occurred
21	CMD_WRITE_PAGE	Write a configuration page (whatever page has been loaded to registers 0x20 and following will be written to the device)
22	CMD_LOAD_CONFIG_PAGE	Load configuration page
30	CMD_OSC_TUNE_UP	Increase on-chip oscillator frequency, not monotonically increasing
31	CMD_OSC_TUNE_DOWN	Decrease on-chip oscillator frequency, not monotonically decreasing
64	CMD_LOAD_CFG_8X8	Preconfigure for 8x8 default mode and load configuration page
65	CMD_LOAD_CFG_8X8_LONG_RANGE	Preconfigure for 8x8 12m mode and load configuration page
66	CMD_LOAD_CFG_8X8_HIGH_ACCURACY	Preconfigure for 8x8 (short range mode) higher resolution = Better visibility at short range and load configuration page
67	CMD_LOAD_CFG_16X16	Preconfigure for 16x16 default mode and load configuration page
68	CMD_LOAD_CFG_16X16_HIGH_ACCURACY	Preconfigure for 16x16 short range mode and load configuration page
69	CMD_LOAD_CFG_32X32	Preconfigure for 32x32 default mode and load configuration page
70	CMD_LOAD_CFG_32X32_HIGH_ACCURACY	Preconfigure for 32x32 short range mode and load configuration page
71	CMD_LOAD_CFG_48X32	Preconfigure for 48x32 default mode and load configuration page
72	CMD_LOAD_CFG_48X32_HIGH_ACCURACY	Preconfigure for 48x32 short range mode and load configuration page
255	CMD_STOP	Stop: Abort any ongoing measurement
All other not specified values shall not to be used and the behavior if one of them is set, is undefined.		

Table 16: Status of TMF8829 - read from register 0x08 / cmd_stat

Code (decimal)	Symbol	Function
0	STAT_OK	OK, command accepted and successfully executed
1	STAT_ACCEPTED	Command accepted and being executed, send a STOP command to halt continues execution
2	STAT_ERR_CONFIG	ERROR configuration not accepted, reconfiguration needed
3	STAT_ERR_APPLICATION	ERROR application encountered a severe error and stopped
4	STAT_ERR_CONFIG_RESULT_SIZE	ERROR configuration will generate result frames that are too big to be transferred
5	STAT_ERR_CONFIG_VCSEL	ERROR configuration of VCSEL (only one of the two can be on at one point in time)
6	STAT_ERR_WAKEUP_TIMED	ERROR wakeup timed, severe internal error, device should be power cycled
7	STAT_ERR_RESET_UNEXPECTED	ERROR unexpected reset, severe internal error, device should be power cycled
8	STAT_ERR_UNKNOWN_CMD	ERROR unknown command
9	STAT_ERR_UNKNOWN_CID	ERROR tried to write a config page with unknown CID
10, 11, 12, 13	STAT_ERR_STOP	ERROR stop not accepted, device should be power cycled
14	STAT_ERR_OSC_TUNE	ERROR could not increase or decrease the oscillator frequency

8.1.5 TMF8829_PREV_CMD register (Address 0x09)

Table 17: TMF8829_PREV_CMD register

Addr: 0x09		TMF8829_PREV_CMD		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*prev_cmd*	0	RO	The previously executed command by TMF8829

8.1.6 TMF8829_GPIO_VALUE register (Address 0x10)

Table 18: TMF8829_GPIO_VALUE register

Addr: 0x10		TMF8829_GPIO_VALUE		
Field	**Name**	**Rst**	**Type**	**Description**
6	*gpio_value_6*	0	RO	Read back the value of INT/GPIO6 as seen by the device
5	*gpio_value_5*	0	RO	Read back the value of SDA as seen by the device
4	*gpio_value_4*	0	RO	Read back the value of SCL as seen by the device
3	*gpio_value_3*	0	RO	Read back the value of MISO/GPIO3 as seen by the device
2	*gpio_value_2*	0	RO	Read back the value of SCLK/GPIO2 as seen by the device
1	*gpio_value_1*	0	RO	Read back the value of CSN/GPIO1 as seen by the device
0	*gpio_value_0*	0	RO	Read back the value of MOSI/GPIO0 as seen by the device

8.1.7 TMF8829_LIVE_BEAT_0 register (Address 0x1A)

Table 19: TMF8829_LIVE_BEAT_0 register

Addr: 0x1A		TMF8829_LIVE_BEAT_0		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*live_beat_0*	0	RO	Free running counter that counts every time the application wakes up from sleep for CPU 0

8.1.8 TMF8829_LIVE_BEAT_1 register (Address 0x1B)

Table 20: TMF8829_LIVE_BEAT_1 register

Addr: 0x1B		TMF8829_LIVE_BEAT_1		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*live_beat_1*	0	RO	Free running counter that counts every time the application wakes up from sleep for CPU 1

8.1.9 TMF8829_SERIAL_NUMBER_0 register (Address 0x1C)

Table 21: TMF8829_SERIAL_NUMBER_0 register

Addr: 0x1C		TMF8829_SERIAL_NUMBER_0		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*serial_number[7:0]*	0	RO	Unique serial number

8.1.10 TMF8829_SERIAL_NUMBER_1 register (Address 0x1D)

Table 22: TMF8829_SERIAL_NUMBER_1 register

Addr: 0x1D		TMF8829_SERIAL_NUMBER_1		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*serial_number[15:8]*	0	RO	Unique serial number

8.1.11 TMF8829_SERIAL_NUMBER_2 register (Address 0x1E)

Table 23: TMF8829_SERIAL_NUMBER_2 register

Addr: 0x1E		TMF8829_SERIAL_NUMBER_2		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*serial_number[23:16]*	0	RO	Unique serial number

8.1.12 TMF8829_SERIAL_NUMBER_3 register (Address 0x1F)

Table 24: TMF8829_SERIAL_NUMBER_3 register

Addr: 0x1F		TMF8829_SERIAL_NUMBER_3		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*serial_number[31:24]*	0	RO	Unique serial number

8.1.13 TMF8829_CID_RID register (Address 0x20)

Table 25: TMF8829_CID_RID register

Addr: 0x20		TMF8829_CID_RID			
Field	**Name**	**Rst**	**Type**	**Description**	
7:0	*cid_rid*	0	RO	Unique ID identifying the following pages/frames.	
				Code	**Symbol** / **Function**
				22	CID_CONFIG — Config page is loaded
				48	RID_REF_SPAD_FRAME — Reference SPAD frame ID
				64	CID_CFG_8X8 — Preconfigure for 8x8 default mode page
				65	CID_CFG_8X8_LONG_RANGE — Preconfigure for 8x8 12m mode page
				66	CID_CFG_8X8_HIGH_ACCURACY — Preconfigure for 8x8 (short range mode) higher resolution page
				67	CID_CFG_16X16 — Preconfigure for 16x16 default mode page
				68	CID_CFG_16X16_HIGH_ACCURACY — Preconfigure for 16x16 short range mode page
				69	CID_CFG_32X32 — Preconfigure for 32x32 default mode page
				70	CID_CFG_32X32_HIGH_ACCURACY — Preconfigure for 32x32 short range mode page
				71	CID_CFG_48X32 — Preconfigure for 48x32 default mode page
				72	CID_CFG_48X32_HIGH_ACCURACY — Preconfigure for 48x32 short range mode page

8.1.14 TMF8829_PAYLOAD register (Address 0x21)

Table 26: TMF8829_PAYLOAD register

Addr: 0x21		TMF8829_PAYLOAD		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*payload*	0	RO	Number of bytes in page (without this 2-byte header)

8.1.15 I2C_DEVADDR register (Address 0xE0)

Table 27: I2C_DEVADDR register

Addr: 0xE0		I2C_DEVADDR		
Field	**Name**	**Rst**	**Type**	**Bit description**
7:1	*i2c_devaddr*	0x41	RO	This defines the I²C device address of the I²C interface. Use config register *i2c_slave_address* for changes.
0	*reserved*	0x0	RO	Reserved.

8.1.16 INT_STATUS register (Address 0xE1)

Table 28: INT_STATUS register

Addr: 0xE1		INT_STATUS		
Field	**Name**	**Rst**	**Type**	**Description**
3	*int3*	0	R_PUSH1	Histogram interrupt for histogram readout. **int3 status**. If bit is asserted, and *int3_enab* is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear *int3* register.
2	*int2*	0	R_PUSH1	Proximity detection interrupt, see register *prox_distance*. **int2 status**. If bit is asserted, and *int2_enab* is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear *int2* register.
1	*int1*	0	R_PUSH1	Result interrupt to signal motion detection (*post_processing = 1 or 2*) **int1 status**. If bit is asserted, and *int1_enab* is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear *int1* register.
0	*int0*	0	R_PUSH1	Result interrupt to signal measurement results (*post_processing*=0). **int0 status**. If bit is asserted, and *int0_enab* is asserted as well, then the INT pin will be pulled low. Writing a '1' here will clear *int0* register.

8.1.17 INT_ENAB register (Address 0xE2)

Table 29: INT_ENAB register

Addr: 0xE2		INT_ENAB		
Field	**Name**	**Rst**	**Type**	**Description**
3	*int3_enab*	0	RW	0 = Disabled, 1 = Enabled -> INT output is active if *int3* flag is "1".
2	*int2_enab*	0	RW	0 = Disabled, 1 = Enabled -> INT output is active if *int2* flag is "1".
1	*int1_enab*	0	RW	0 = Disabled, 1 = Enabled -> INT output is active if *int1* flag is "1".
0	*int0_enab*	0	RW	0 = Disabled, 1 = Enabled -> INT output is active if *int0* flag is "1".

Note: This register has only influence on the digital pin INT. It does not prevent assertion of the interrupt in register INT_STATUS.

8.1.18 ID register (Address 0xE3)

Table 30: ID register

Addr: 0xE3		ID		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*id*	9eh	RO	Chip ID, reads 0x9e to identify TMF8829.

8.1.19 REVID register (Address 0xE4)

Table 31: REVID register

Addr: 0xE4		REVID		
Field	**Name**	**Rst**	**Type**	**Description**
2:0	*rev_id*	1	RO	Chip revision ID

8.1.20 INTERFACE register (Address 0xE9)

Table 32: INTERFACE register

Addr: 0xE9		INTERFACE – see section 7.9		
Field	**Name**	**Rst**	**Type**	**Description**
7	*Reserved*	0	RO	Reserved, set to 0
6	*i2c_interface_enable*	1	R_PUSH	I²C interface is active on the SCL/SDA pins
5	*spi_interface_enable*	1	R_PUSH	SPI interface is active on the SPI pins
4:0	*Reserved*	0x00	RO	Reserved, set to 0

8.1.21 GPIO01CFG register (Address 0xF1)

Table 33: GPIO01CFG register

Addr: 0xF1		GPIO01CFG		
Field	**Name**	**Rst**	**Type**	**Description**
7:4	*gpio1_func*	1	RW	CSN/GPIO1 function **Value** **Description** 0 GPIO1 functionality 1 SPI CSN (chips select input) 2-15 Don't use any other values
3:0	*gpio0_func*	1	RW	MOSI/GPIO0 function **Value** **Description** 0 GPIO0 functionality 1 SPI MOSI (serial data input) 2-15 Don't use any other values

8.1.22 GPIO23CFG register (Address 0xF2)

Table 34: GPIO23CFG register

Addr: 0xF2		GPIO23CFG			
Field	**Name**	**Rst**	**Type**	**Description**	
7:4	*gpio3_func*	1	RW	MISO/GPIO3 function	
				Value	**Description**
				0	GPIO3 functionality
				1	SPI MISO (serial data output)
				2-15	Don't use any other values
3:0	*gpio2_func*	1	RW	SCLK/GPIO2 function	
				Value	**Description**
				0	GPIO2 functionality
				1	SPI SCLK (serial clock input)
				2-15	Don't use any other values

8.1.23 GPIO45CFG register (Address 0xF3)

Table 35: GPIO45CFG register

Addr: 0xF3		GPIO45CFG			
Field	**Name**	**Rst**	**Type**	**Description**	
7:4	*gpio5_func*	1	RW	SDA function	
				Value	**Description**
				0	GPIO5 functionality
				1	I²C/I3C SDA (serial data input/output)
				2-15	Don't use any other values
3:0	*gpio4_func*	1	RW	SCL function	
				Value	**Description**
				0	GPIO4 functionality
				1	I²C/I3C SCL (serial clock input)
				2-15	Don't use any other values

8.1.24 GPIO6CFG register (Address 0xF4)

Table 36: GPIO6CFG register

Addr: 0xF4		GPIO6CFG			
Field	**Name**	**Rst**	**Type**	**Description**	
7:4	*Reserved*	0	RO	Reserved, set to 0	
3:0	*gpio6_func*	1	RW	INT/GPIO6 function	
				Value	**Description**
				0	GPIO6
				1	INT (low active interrupt, default)
				2-15	Don't use any other values

8.1.25 RESET register (Address 0xF7)

Table 37: RESET register

Addr: 0xF7	RESET			
Field	**Name**	**Rst**	**Type**	**Description**
7	*hard_reset*	0	PUSH1	Equivalent to a power on reset – triggers a cold start
6	*soft_reset*	0	PUSH1	Reset CPUs and internal registers; interface selection is not affected
5:0	*Reserved*	0xx	RO	Reserved, set to 0

8.1.26 ENABLE register (Address 0xF8)

Table 38: ENABLE register

Addr: 0xF8		ENABLE		
Field	**Name**	**Rst**	**Type**	**Description**
7	*cpu_ready*	0	RO	TMF8829 is ready to handle commands - if this bit is zero, then the device will not respond to requests. Bit gets set only explicitly by software, therefore a functional and running firmware is necessary for this bit to work
6:4	*powerup_select*	0x00	RW	Select what to do at powerup (*pon*=1) 0 … Boot loader 1 … Force boot loader 2 … RAM 3 … Reserved, don't use
3	*poff*	0	PUSH1	1=Ask TMF8829 to go to standby mode, register cannot be read back
2	*pon*	0x1	R_PUSH1	If this bit reads back 1, then the system is in Active mode, otherwise Standby or Timed Standby. Activating the device from power-down is implemented in hardware. Whenever this register is '0' and a '1' is being written, the power is being activated and TMF8829 is being booted. Note that if this bit reads 1, but the standby_mode bit reads 1, then the system is in transition to Active mode.
1	*timed_standby_mode*	0x0	RO	This bit reads back 0 in normal operation mode, and 1 in Timed Standby mode.
0	*standby_mode*	0x0	RO	This bit reads back 0 in normal operation mode, and 1 in Standby mode (non-timed).

8.1.27 FIFOSTATUS register (Address 0xFA)

Table 39: FIFOSTATUS register

Addr: 0xFA		FIFOSTATUS		
Field	**Name**	**Rst**	**Type**	**Description**
5	*rxfifo_overrun*	0	SS_WC	Host was writing into full FIFO. Write 1 to clear.
4	*txfifo_underrun*	0	SS_WC	Host was reading from empty FIFO. Write 1 to clear.
3	*rxfifo_full*	0	RO	In RXFIFO mode: Indicates the host cannot write. There's no space left for the host. Disregard in TXFIFO mode.
2	*txfifo_empty*	0	RO	In TXFIFO mode: Indicates the host cannot read. There's no data available for the host. Disregard in RXFIFO mode.
1	*fifo_dma_busy*	0	RO	Transaction ongoing still In TXFIFO mode: Indicates more data from CPU will be pushed into FIFO. In RXFIFO mode: Indicates more data from host expected to be pushed into FIFO. **Note:** For the host to write to the FIFO this flag shall be 1. Otherwise, any writes from the host to the FIFO are ignored and produce a *rxfifo_overrun* flag.
0	*fifo_direction*	0	RO	FIFO mode setup by TMF8829: 0 … Configured as TXFIFO (TMF8829 to host) 1 … Configured as RXFIFO (host to TMF8829)

8.1.28 SYSTICK_0 register (Address 0xFB)

Table 40: SYSTICK_0 register

Addr: 0xFB		SYSTICK_0		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*hif_systick[7:0]*	0	RO	32-bit systick running from 125kHz clock.

8.1.29 SYSTICK_1 register (Address 0xFC)

Table 41: SYSTICK_1 register

Addr: 0xFC		SYSTICK_1		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*hif_systick[15:8]*	0	RO	32-bit systick running from 125kHz clock.

8.1.30 SYSTICK_2 register (Address 0xFD)

Table 42: SYSTICK_2 register

Addr: 0xFD		SYSTICK_2		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*hif_systick[23:16]*	0	RO	32-bit systick running from 125kHz clock.

8.1.31 SYSTICK_3 register (Address 0xFE)

Table 43: SYSTICK_3 register

Addr: 0xFE		SYSTICK_3		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*hif_systick[31:24]*	0	RO	32-bit systick running from 125kHz clock.

8.1.32 FIFO register (Address 0xFF)

Table 44: FIFO register

Addr: 0xFF		FIFO		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*fifo_data*	0x00	PUSHPOP	FIFO access (R/W)

8.2 cid_rid = 22 or 64…72 / CID_CONFIG registers

To modify any of the registers in this chapter, first load the config page:

See *cmd_stat* codes CMD_LOAD_CONFIG_PAGE, CMD_LOAD_CFG_8X8 … CMD_LOAD_CFG_48X32_HIGH_ACCURACY

Then modify the register and write back the configuration:

See *cmd_stat* codes CMD_WRITE_PAGE or CMD_WRITE_PAGE_AND_MEASURE.

8.2.1 TMF8829_CFG_PERIOD_MS_LSB (Address 0x22)

Table 45: TMF8829_CFG_PERIOD_MS_LSB register

Addr: 0x22		TMF8829_CFG_PERIOD_MS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*period[7:0]*	33	RW	Measurement period in milli-seconds

8.2.2 TMF8829_CFG_PERIOD_MS_MSB (Address 0x23)

Table 46: TMF8829_CFG_PERIOD_MS_MSB register

Addr: 0x23		TMF8829_CFG_PERIOD_MS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*period[15:8]*	0	RW	Measurement period in milli-seconds

8.2.3 TMF8829_CFG_KILO_ITERATIONS_LSB (Address 0x24)

Table 47: TMF8829_CFG_KILO_ITERATIONS_LSB register

Addr: 0x24		TMF8829_CFG_KILO_ITERATIONS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*iterations[7:0]*	74	RW	Measurement kilo iterations LSB. **Calculation:** Iterations = 1024 * (*iterations[15:8]** 256 + *iterations[7:0]*) Default 586*1024 = 600k iterations

8.2.4 TMF8829_CFG_KILO_ITERATIONS_MSB (Address 0x25)

Table 48: TMF8829_CFG_KILO_ITERATIONS_MSB register

Addr: 0x25		TMF8829_CFG_KILO_ITERATIONS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*iterations[15:8]*	2	RW	Measurement kilo iterations MSB. **Calculation:** Iterations = 1024 * (*iterations[15:8]** 256 + *iterations[7:0]*)

8.2.5 TMF8829_CFG_FP_MODE (Address 0x26)

Table 49: TMF8829_CFG_FP_MODE register

Addr: 0x26		TMF8829_CFG_FP_MODE				
Field	**Name**	**Rst**	**Type**	**Description**		
7:0	*fp_mode*	2	RW	Focal plane mode – Resolution of TMF8829		
				Code	**Symbol**	**Function**
				0	FP_8x8A	8x8 mode, 1x time-multiplexed, 4x (3x2) SPADs are used for one depth pixel
				1	FP_8x8B	8x8 mode, combined 4 macro-pixels before TDC – Do not use
				2	FP_16x16	16x16 mode, 1x time-multiplexed, 3x2 SPADs are used for one depth pixel
				3	FP_32x32	32x32 mode, 8x time-multiplexed and 2x1 SPADs are used for one depth pixel
				4	FP_32x32s	32x32 mode, 8x time-multiplexed and one (single) SPAD is used for one depth pixel
				5	FP_48x32	48x32 mode, 12x time-multiplexed and one (single) SPAD is used for one depth pixel

Information:

TMF8829 has a total of 16x16 macro-pixels and each macro-pixel has 3x2 SPADs (Total: 48x32=1536 measurement SPADs).

8.2.6 TMF8829_CFG_SPAD_SELECT (Address 0x27)

Table 50: TMF8829_CFG_SPAD_SELECT register

Addr: 0x27		TMF8829_CFG_SPAD_SELECT		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*spad_select*	63	RW	SPAD mask per macro-pixel Bit0 = Top left, bit1 = top mid, ..., is the same for all macro-pixels. Only used for 8x8 and 16x16 modes.

8.2.7 TMF8829_CFG_REF_SPAD_SELECT (Address 0x28)

Table 51: TMF8829_CFG_REF_SPAD_SELECT register

Addr: 0x28		TMF8829_CFG_REF_SPAD_SELECT		
Field	**Name**	**Rst**	**Type**	**Description**
5:0	*ref_spad_select*	2	RO	Keep at default value, do not change.

8.2.8 TMF8829_CFG_SPAD_DEADTIME (Address 0x29)

Table 52: TMF8829_CFG_SPAD_DEADTIME register

Addr: 0x29		TMF8829_CFG_SPAD_DEADTIME		
Field	**Name**	**Rst**	**Type**	**Description**
5:0	*dead_time*	60	RW	SPAD dead time setting, where, 0=291ns, 1=237ns, 2=198ns, 3=171ns, 4=150ns, 5=134ns, 7=110ns, 10=87ns, 15=65ns, 20=51ns, 25=43ns, 30=37ns, 40=25ns, 45=18ns, 50=15ns, **60=11ns** (default), 63=10ns

8.2.9 TMF8829_CFG_RESULT_FORMAT (Address 0x2A)

Table 53: TMF8829_CFG_RESULT_FORMAT register

Addr: 0x2A		TMF8829_CFG_RESULT_FORMAT (Configure reported results for each depth pixel)		
Field	**Name**	**Rst**	**Type**	**Description**
7	*full_noise*	0	RW	If set the noise_strength is reporting the sum and is no longer divided by number of bins
6	*sub_result*	0	RO	Only read, is used to encode the sub-result frame in the results; on writing use '0' to write
5	*xtalk*	0	RW	If set, 2 bytes x-talk (crosstalk) shall be encoded with each depth pixel. X-talk is the sum of the crosstalk peak and its two adjacent neighbor bins. Values 0…32767 are encoded as is (factor 1) and bit 15 reset, values 32768 or higher are encoded divided by 256 and bit 15 set.
4	*noise_strength*	0	RW	If set, 2 bytes noise strength (=baseline of the histogram) shall be encoded with each depth pixel (sum of the full histogram excluding peaks divided by the number of bins) Values 0…32767 are encoded as is (factor 1) and bit 15 reset, values 32768 or higher are encoded divided by 256 and bit 15 set.
3	*signal_strength*	0	RW	If set, 2 bytes signal strength shall be encoded with each depth pixel; signal strength is the peak height above the baseline where the peak plus its two adjacent neighbor bins are added. Values 0…32767 are encoded as is (factor 1) and bit 15 reset, values 32768 or higher are encoded divided by 256 and bit 15 set.
2:0	*nr_peaks*	1	RW	If non-zero, then this is the number of peaks per depth pixel with each result, max is 4 peaks **Note:** It depends on the height and length of the peaks in the histogram. If more than one results per pixel is reported.

8.2.10 TMF8829_CFG_DUMP_HISTOGRAMS (Address 0x2B)

Table 54: TMF8829_CFG_DUMP_HISTOGRAMS register

Addr: 0x2B		TMF8829_CFG_DUMP_HISTOGRAMS		
Field	**Name**	**Rst**	**Type**	**Description**
0	*histograms*	0	RW	If set then raw histograms are provided in blocking mode. I.e., the host *has* to read them, otherwise the device will not continue to measure.

8.2.11 TMF8829_CFG_POWER_MODES (Address 0x2E)

Table 55: TMF8829_CFG_POWER_MODES register

Addr: 0x2E		TMF8829_CFG_POWER_MODES		
Field	**Name**	**Rst**	**Type**	**Description**
3	*spad_cropping*	0	RW	If this bit is set auto-deselection SPAD of a disabled MP is done before each measurement. Only set this if cropping is used as this function consumes runtime, but saves power.
2	*lp_osc_device_sleep*	1	RW	If this bit is set the low power oscillator is used when going to standby-timed. This bit only influences the standby-timed mode.
1	*device_sleep*	0	RW	If this bit is set the device goes to standby timed (see parameter $I_{STANDBY\_TIMER}$) during periodic measurements when all work is done (i.e. the distances have been calculated, published and read by the host).
0	*cpu_sleep*	1	RW	If this bit is set the CPUs go to sleep mode (WFE – wait for event) when no work is pending.

8.2.12 TMF8829_CFG_VCSEL_ON (Address 0x30)

Table 56: TMF8829_CFG_VCSEL_ON register

Addr: 0x30		TMF8829_CFG_VCSEL_ON			
Field	**Name**	**Rst**	**Type**	**Description**	
3:2	*t1_vcsel*	1	RW	VCSEL used for timeslot t1	
				Code	**Function**
				0	Use no VCSEL
				1	Use VCSEL0
				2	Use VCSEL1
1:0	*t0_vcsel*	2	RW	VCSEL used for timeslot t0 with same coding like t1_vcsel above	

8.2.13 TMF8829_CFG_DITHER (Address 0x31)

Table 57: TMF8829_CFG_DITHER register

Addr: 0x31		TMF8829_CFG_DITHER (See section 7.7.1, Table 9: Spread spectrum configurations)		
Field	**Name**	**Rst**	**Type**	**Description**
6:4	*dither_rounds*	0	RW	Spread spectrum: Dither rounds, number of VCSEL periods to apply increment
2:0	*dither_increment*	0	RW	Spread spectrum: Add this many unit delays every VCSEL period

8.2.14 TMF8829_CFG_VCDRV (Address 0x32)

Table 58: TMF8829_CFG_VCDRV register

Addr: 0x32		TMF8829_CFG_VCDRV		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*pulse_width*	3	RW	VCSEL driver pulse width 0=330ps 1=660ps 2=1000ps 3=1300ps

8.2.15 TMF8829_CFG_VCDRV_2 (Address 0x33)

Table 59: TMF8829_CFG_VCDRV_2 register

Addr: 0x33		TMF8829_CFG_VCDRV_2		
Field	**Name**	**Rst**	**Type**	**Description**
6:0	*current*	93	RW	VCSEL driver current Use only the settings provided by the operation modes with *cmd_stat* and defined according to Table 6.

8.2.16 TMF8829_CFG_VCDRV_3 (Address 0x34)

Table 60: TMF8829_CFG_VCDRV_3 register

Addr: 0x34		TMF8829_CFG_VCDRV_3		
Field	**Name**	**Rst**	**Type**	**Description**
5	*ext_inv_output*	0	RW	Invert external VCSEL driver signal
4	*ext_en_output*	0	RW	Set to 1 to enable external VCSEL driver signal
3:0	*hi_len*	0	RW	Length of vcdrv high-pulse (hi_len+1)*6.25ns; set to 0 if no external VCSEL driver is used (*ext_en_output*=0)

8.2.17 TMF8829_VCSEL_PERIOD_200PS_LSB (Address 0x36)

Table 61: TMF8829_VCSEL_PERIOD_200PS_LSB register

Addr: 0x36		TMF8829_VCSEL_PERIOD_200PS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*vcsel_period[7:0]*	249	RW	VCSEL period setting LSB in 203.65 ps steps Shall not be a multiple of 31 and 249 is fastest setting. Example with default 249: 249*203.65 ps = 50.7 ns ~ 19.72 MHz -> (249-31)*203.65 ps = 44.4 ns can be recorded

8.2.18 TMF8829_VCSEL_PERIOD_200PS_MSB (Address 0x37)

Table 62: TMF8829_VCSEL_PERIOD_200PS_MSB register

Addr: 0x37		TMF8829_VCSEL_PERIOD_200PS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*vcsel_period[9:8]*	0	RW	VCSEL period setting in 203.65 ps units MSB See *vcsel_period[7:0] above.*

8.2.19 TMF8829_VCDRV_OFFSET_200PS_LSB (Address 0x38)

Table 63: TMF8829_VCDRV_OFFSET_200PS_LSB register

Addr: 0x38		TMF8829_VCDRV_OFFSET_200PS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*vcdrv_offset[7:0]*	0	RW	VCSEL driver time offset LSB in 203.65 ps steps Only set *vcdrv_offset* > 0 or *tdc_offset* > 0 not both

8.2.20 TMF8829_VCDRV_OFFSET_200PS_MSB (Address 0x39)

Table 64: TMF8829_VCDRV_OFFSET_200PS_MSB register

Addr: 0x39		TMF8829_VCDRV_OFFSET_200PS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*vcdrv_offset[9:8]*	0	RW	VCSEL driver time offset MSB in 203.65 ps steps Only set *vcdrv_offset* > 0 or *tdc_offset* > 0 not both

8.2.21 TMF8829_VCDRV_CP (Address 0x3A)

Table 65: TMF8829_VCDRV_CP register

Addr: 0x3A		TMF8829_VCDRV_CP		
Field	**Name**	**Rst**	**Type**	**Description**
6:6	*vc_spr_spec_single_edge*	0	RW	If set randomize VCSEL driver charge pump clock; keep at 0
5:4	*vc_spr_spec_cfg*	0	RW	Select mode for spread spectrum – see section 7.7.1
3:0	*vc_spr_spec_amp*	0	RW	Amplitude for spread spectrum: 0 = Disable, 1..15 = Amount of jitter

8.2.22 TMF8829_HISTOGRAM_BINS_LSB (Address 0x40)

Table 66: TMF8829_HISTOGRAM_BINS_LSB register

Addr: 0x40		TMF8829_HISTOGRAM_BINS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*histogram_bins[7:0]*	218	RW	Number of bins in histogram bins where maximum is vcsel_period - 31 Note that this number is divided by (1<<TMF8829_BIN_SHIFT); for 16x16 mode or higher only 64 bins max after bin shift, in 8x8 mode maximum 256 bins after bin-shift In 8x8 always 256 bins are transferred, in all other modes 64 bins are transferred. Examples: bin-shift=2, 256 histogram_bins -> 256/(1<<2) = 64 bins, which is possible in all modes bin-shift=0, 256 histogram_bins ==> 256/(1<<0)=256 bins, only possible for 8x8 mode

8.2.23 TMF8829_HISTOGRAM_BINS_MSB (Address 0x41)

Table 67: TMF8829_HISTOGRAM_BINS_MSB register

Addr: 0x41		TMF8829_HISTOGRAM_BINS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*histogram_bins[9:8]*	0	RW	MSB of histogram bins – see description above

8.2.24 TMF8829_BIN_SHIFT (Address 0x42)

Table 68: TMF8829_BIN_SHIFT register

Addr: 0x42		TMF8829_BIN_SHIFT					
Field	**Name**	**Rst**	**Type**	**Description**			
1:0	*bin_shift*	2	RW	Time duration of one bin in the histogram where			
				Code	**Time per bin**	**Distance per bin**	**VCSEL *pulse_width* recommendation**
				0	200 ps	3 cm	330 ps (*pulse_width* = 0)
				1	400 ps	6 cm	660 ps (*pulse_width* = 1)
				2	800 ps	12 cm	1300 ps (*pulse_width* = 3)
				3	1600 ps	24 cm	1300 ps not recommended as VCSEL pulse is shorter than one bin

8.2.25 TMF8829_REF_BIN_SHIFT (Address 0x43)

Table 69: TMF8829_REF_BIN_SHIFT register

Addr: 0x43		TMF8829_REF_BIN_SHIFT		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*ref_bin_shift*	2	RW	Same as *bin_shift* but for the reference histogram Time duration of one bin in the reference histogram.

8.2.26 TMF8829_TDC_OFFSET_200PS_LSB (Address 0x44)

Table 70: TMF8829_TDC_OFFSET_200PS_LSB register

Addr: 0x44		TMF8829_TDC_OFFSET_200PS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*tdc_offset[7:0]*	14	RW	TDC time offset in 203.65 ps steps; LSB value Only set *vcdrv_offset* > 0 or *tdc_offset* > 0 not both

8.2.27 TMF8829_TDC_OFFSET_200PS_MSB (Address 0x45)

Table 71: TMF8829_TDC_OFFSET_200PS_MSB register

Addr: 0x45		TMF8829_TDC_OFFSET_200PS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*tdc_offset[9:8]*	0	RW	TDC time offset in 203.65 ps steps; LSB value Only set *vcdrv_offset* > 0 or *tdc_offset* > 0 not both

8.2.28 TMF8829_TDC_PRE_PERIODS_LSB (Address 0x46)

Table 72: TMF8829_TDC_PRE_PERIODS_LSB register

Addr: 0x46		TMF8829_TDC_PRE_PERIODS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*settling[7:0]*	80	RW	TDC settling time LSB value in *vcsel_period* units; for default *vcsel_period* value of 50.7 ns and *settling* = 80, this is ~ 4.1 µs Keep this setting at the default value.

8.2.29 TMF8829_TDC_PRE_PERIODS_MSB (Address 0x47)

Table 73: TMF8829_TDC_PRE_PERIODS_MSB register

Addr: 0x47		TMF8829_TDC_PRE_PERIODS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*settling[9:8]*	80	RW	TDC settling time MSB value, see above

8.2.30 TMF8829_HV_CP (Address 0x48)

Table 74: TMF8829_HV_CP register

Addr: 0x48		TMF8829_HV_CP – see section 7.7.1		
Field	**Name**	**Rst**	**Type**	**Description**
6	*spr_spec_single_edge*	0	RW	If set randomize HV CP clock with each pos-edge; keep at 0
5:4	*spr_spec_cfg*	0	RW	Select mode for spread spectrum – see section 7.7.1
3:0	*spr_spec_amp*	0	RW	Amplitude for spread spectrum: 0 = Disable 1..15 = Amount of jitter

8.2.31 TMF8829_CFG_HA_KILO_ITERATIONS_LSB (Address 0x4A)

Table 75: TMF8829_CFG_HA_KILO_ITERATIONS_LSB register

Addr: 0x4A		TMF8829_CFG_HA_KILO_ITERATIONS_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*high_accuracy_iterations[7:0]*	100	RW	Measurement kilo iterations LSB for dual mode – see section 7.3.1 – only used if *dual_mode*=1 or 2 **Calculation:** Iterations = 1024 * (*high_accuracy_iterations [15:8]** 256 + *high_accuracy_iterations [7:0]*) Default 100*1024 = 102k iterations

8.2.32 TMF8829_CFG_HA_KILO_ITERATIONS_MSB (Address 0x4B)

Table 76: TMF8829_CFG_HA_KILO_ITERATIONS_MSB register

Addr: 0x4B		TMF8829_CFG_HA_KILO_ITERATIONS_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*high_accuracy_iterations [15:8]*	0	RW	Measurement kilo iterations LSB for dual mode – see section 7.3.1 – only used if *dual_mode*=1 or 2 **Calculation:** Iterations = 1024 * (*high_accuracy_iterations [15:8]** 256 + *high_accuracy_iterations [7:0]*) Default 100*1024 = 102k iterations

8.2.33 TMF8829_CFG_ENABLE_DUAL_MODE (Address 0x4C)

Table 77: TMF8829_CFG_ENABLE_DUAL_MODE register

Addr: 0x4C		TMF8829_CFG_ENABLE_DUAL_MODE		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*dual_mode*	0	RW	If set use dual-mode, if cleared no dual-mode – details are described in section 7.3.1 0 = No dual mode 1 = Dual-mode is high-accuracy and regular-range-mode (up to ~6m) 2 = Dual-mode is high-accuracy and 8x8 long range mode (up to 11m)

8.2.34 TMF8829_CFG_HV_CP_OVERLOAD_DETECT (Address 0x4D)

Table 78: TMF8829_CFG_HV_CP_OVERLOAD_DETECT register

Addr: 0x4D		TMF8829_CFG_HV_CP_OVERLOAD_DETECT		
Field	**Name**	**Rst**	**Type**	**Description**
0	*hv_cp_overload_detect*	0	RW	Set to discard results for *bin_shift* = 2 when a high-voltage charge-pump overload was detected, clear to always use results even when overload was detected

8.2.35 TMF8829_CFG_ALG_PEAK_BINS (Address 0x50)

Table 79: TMF8829_CFG_ALG_PEAK_BINS register

Addr: 0x50		TMF8829_CFG_ALG_PEAK_BINS		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*peak_bins*	2	RW	Number of bins to use for peak detection and peak strength calculation 0=1 bin, 1=2 bins, 2=3 bins, 3=4 bins

8.2.36 TMF8829_CFG_ALG_REF_PEAK_BINS (Address 0x51)

Table 80: TMF8829_CFG_ALG_REF_PEAK_BINS register

Addr: 0x51		TMF8829_CFG_ALG_REF_PEAK_BINS		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*ref_peak_bins*	2	RW	Number of bins to use for reference peak detection 0=1 bin, 1=2 bins, 2=3 bins, 3=4 bins

8.2.37 TMF8829_CFG_ALG_DISTANCE (Address 0x52)

Table 81: TMF8829_CFG_ALG_DISTANCE register

Addr: 0x52		TMF8829_CFG_ALG_DISTANCE		
Field	**Name**	**Rst**	**Type**	**Description**
1:0	*select*	1	RW	Automatically selected when mode is selected – see section 7.3 Distance is reported in 0.25 mm steps 1 = Distance algorithm for default modes (max distance ~6m or 11m) 2 = Distance algorithm for high performance modes (max distance 1.4m)

8.2.38 TMF8829_CFG_ALG_CONFIDENCE_THRESHOLD (Address 0x53)

Table 82: TMF8829_CFG_ALG_CONFIDENCE_THRESHOLD register

Addr: 0x53		TMF8829_CFG_ALG_CONFIDENCE_THRESHOLD		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*confidence_threshold*	6	RW	Only objects which have a confidence level (this is signal to noise ratio) equal or higher than this will be reported

8.2.39 TMF8829_CFG_ALG_HW_PEAK_START (Address 0x57)

Table 83: TMF8829_CFG_ALG_HW_PEAK_START register

Addr: 0x57		TMF8829_CFG_ALG_HW_PEAK_START		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*peak_detect_start*	25	RO	Nominal start bin (for bin-shift 0) for hardware assisted peak detect

8.2.40 TMF8829_CFG_ALG_CALIBRATION (Address 0x5F)

Table 84: TMF8829_CFG_ALG_CALIBRATION register

Addr: 0x5F		TMF8829_CFG_ALG_CALIBRATION		
Field	**Name**	**Rst**	**Type**	**Description**
0	*add_100_mm_offset*	0	RW	If set an offset of 100 mm will be added to each pixel distance – therefore the algorithm can report negative distances as well especially if additional host side calibration is used.

8.2.41 TMF8829_CFG_INT_ZONE_MASK_0 (Address 0x60) – TMF8829_CFG_INT_ZONE_MASK_7 (Address 0x67)

Table 85: TMF8829_CFG_INT_ZONE_MASK_0 (Address 0x60) – TMF8829_CFG_INT_ZONE_MASK_7 (Address 0x67) registers

Addr: 0x60 – 0x67		TMF8829_CFG_INT_ZONE_MASK_0 – TMF8829_CFG_INT_ZONE_MASK_7		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*int_zone_mask[7:0]* … *int_zone_mask[63:56]]*	255	RW	Interrupt masked on zone A 1 means this zone can trigger an interrupt, lsb is zone 0

64-bit register to mask the zones which can raise an interrupt, applies for 8x8 mode directly.
For 16x16 mode, combine 2x2 pixels together to use only an 8x8 zone mask.
For 32x32 mode, combine 4x4 pixels together to use only an 8x8 zone mask.
For 48x32 mode, these registers have no effect.

8.2.42 TMF8829_CFG_INT_THRESHOLD_LOW_LSB (Address 0x68)

Table 86: TMF8829_CFG_INT_THRESHOLD_LOW_LSB register

Addr: 0x68		TMF8829_CFG_INT_THRESHOLD_LOW_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*int_threshold_low[7:0]*	0	RW	Interrupt threshold for distance LSB – only zones >= *int_threshold_low* will trigger an interrupt

8.2.43 TMF8829_CFG_INT_THRESHOLD_LOW_MSB (Address 0x69)

Table 87: TMF8829_CFG_INT_THRESHOLD_LOW_MSB register

Addr: 0x69		TMF8829_CFG_INT_THRESHOLD_LOW_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*int_threshold_low[15:8]*	0	RW	Interrupt threshold for distance MSB – only zones >= *int_threshold_low* will trigger an interrupt

8.2.44 TMF8829_CFG_INT_THRESHOLD_HIGH_LSB (Address 0x6A)

Table 88: TMF8829_CFG_INT_THRESHOLD_HIGH_LSB register

Addr: 0x6A		TMF8829_CFG_INT_THRESHOLD_HIGH_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*int_threshold_high[7:0]*	255	RW	Interrupt threshold for distance LSB – only zones <= *int_threshold_high* will trigger an interrupt

8.2.45 TMF8829_CFG_INT_THRESHOLD_HIGH_MSB (Address 0x6B)

Table 89: TMF8829_CFG_INT_THRESHOLD_HIGH_MSB register

Addr: 0x6B		TMF8829_CFG_INT_THRESHOLD_HIGH_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*int_threshold_high[15:8]*	255	RW	Interrupt threshold for distance MSB – only zones <= *int_threshold_high* will trigger an interrupt

8.2.46 TMF8829_CFG_INT_PERSISTENCE (Address 0x6C)

Table 90: TMF8829_CFG_INT_PERSISTENCE register

Addr: 0x6C		TMF8829_CFG_INT_PERSISTENCE		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*int_persistence*	0	RW	0 means each measurement that finds a target inside the threshold range will trigger an interrupt 1 means there have to be two consecutive measurements that find a target inside the threshold range will trigger an interrupt 2 …three consecutive measurements … and so on.

8.2.47 TMF8829_CFG_POST_PROCESSING (Address 0x6D)

Table 91: TMF8829_CFG_POST_PROCESSING register

Addr: 0x6D		TMF8829_CFG_POST_PROCESSING				
Field	**Name**	**Rst**	**Type**	**Description**		
7:0	*post_processing*	0	RW	Select post processing algorithm		
				Code	**Symbol**	**Function**
				0	PERSISTENCE	Persistence algorithm enabled, persistence interrupt is *int1*
				1	MOTION	Motion detection, set *int_persistence* >=1 as well; motion interrupt is *int1*
				2	MOTION_ALWAYS_RESULTS	Same as MOTION but result frames are always published but *int1* only asserted upon motion detection

8.2.48 TMF8829_CFG_PROX_DISTANCE (Address 0x6E)

Table 92: TMF8829_CFG_PROX_DISTANCE register

Addr: 0x6E		TMF8829_CFG_PROX_DISTANCE		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*prox_distance*	0	RW	Proximity distance in mm. Any object detected closer than *prox_distance* in [mm] will raise a proximity interrupt *int2*. If proximity distance is set to the default 0 or *int_persistence*=0, function is disabled.

8.2.49 TMF8829_CFG_CROP_TOP_X (Address 0x70)

Table 93: TMF8829_CFG_CROP_TOP_X register

Addr: 0x70		TMF8829_CFG_CROP_TOP_X		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*mp_top_x*	0	RW	Restrict the area in which objects are recorded to the macro-pixels defined by rectangular mp_top_x/mp_top_y to mp_bottom_x/mp_bottom_y (full FOV has 16x16 macro-pixels) Set register *spad_cropping*=1 to disable SPADs which are outside the cropped area.

8.2.50 TMF8829_CFG_CROP_TOP_Y (Address 0x71)

Table 94: TMF8829_CFG_CROP_TOP_Y register

Addr: 0x71		TMF8829_CFG_CROP_TOP_Y		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*mp_top_y*	0	RW	Restrict the area in which objects are recorded to the macro-pixels defined by rectangular mp_top_x/mp_top_y to mp_bottom_x/mp_bottom_y (full FOV has 16x16 macro-pixels) Set register *spad_cropping*=1 to disable SPADs which are outside the cropped area.

8.2.51 TMF8829_CFG_CROP_BOTTOM_X (Address 0x72)

Table 95: TMF8829_CFG_CROP_TOP_X register

Addr: 0x72		TMF8829_CFG_CROP_BOTTOM_X		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*mp_bottom_x*	0	RW	Restrict the area in which objects are recorded to the macro-pixels defined by rectangular mp_top_x/mp_top_y to mp_bottom_x/mp_bottom_y (full FOV has 16x16 macro-pixels) Set register *spad_cropping*=1 to disable SPADs which are outside the cropped area.

8.2.52 TMF8829_CFG_CROP_BOTTOM_Y (Address 0x73)

Table 96: TMF8829_CFG_CROP_BOTTOM_Y register

Addr: 0x73		TMF8829_CFG_CROP_BOTTOM_Y		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*mp_bottom_y*	0	RW	Restrict the area in which objects are recorded to the macro-pixels defined by rectangular mp_top_x/mp_top_y to mp_bottom_x/mp_bottom_y (full FOV has 16x16 macro-pixels) Set register *spad_cropping*=1 to disable SPADs which are outside the cropped area.

8.2.53 TMF8829_CFG_INFO_FOV_CORR (Address 0x78)

Table 97: TMF8829_CFG_INFO_FOV_CORR register

Addr: 0x78		TMF8829_CFG_INFO_FOV_CORR		
Field	**Name**	**Rst**	**Type**	**Description**
3:0	*fov_correction*	0	RW	Field of view sub-pixel correction value: Can be used for the host to further fine-tune perpendicular field of view.

8.2.54 TMF8829_CFG_GPIO_0 (Address 0x80)

Table 98: TMF8829_CFG_GPIO_0 register

Addr: 0x80				TMF8829_CFG_GPIO_0		
Field	**Name**	**Rst**	**Type**	**Description**		
2:0	*gpio0*	0	RW	MOSI/GPIO0 output control - setting will be ignored if this pin is used as SPI MOSI interface pin unless *gpio0_func*=0		
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (i.e. if high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.55 TMF8829_CFG_GPIO_1 (Address 0x81)

Table 99: TMF8829_CFG_GPIO_1 register

Addr: 0x81 **TMF8829_CFG_GPIO_1**

Field	Name	Rst	Type	Description		
2:0	*gpio1*	0	RW	CSN/GPIO1 output control - setting will be ignored if this pin is used as SPI CSN interface pin unless *gpio1_func*=0		
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (i.e. If high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.56 TMF8829_CFG_GPIO_2 (Address 0x82)

Table 100: TMF8829_CFG_GPIO_2 register

Addr: 0x82		TMF8829_CFG_GPIO_2				
Field	**Name**	**Rst**	**Type**	**Description**		
2:0	*gpio2*	0	RW	SCLK/GPIO2 output control - setting will be ignored if this pin is used as SPI SCLK interface pin unless *gpio2_func*=0		
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in Tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (I.e. If high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.57 TMF8829_CFG_GPIO_3 (Address 0x83)

Table 101: TMF8829_CFG_GPIO_3 register

Addr: 0x83		TMF8829_CFG_GPIO_3				
Field	**Name**	**Rst**	**Type**	**Description**		
2:0	*gpio3*	0	RW	MISO/GPIO3 output control - setting will be ignored if this pin is used as SPI MISO interface pin unless *gpio3_func*=0		
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (i.e. If high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.58 TMF8829_CFG_GPIO_4 (Address 0x84)

Table 102: TMF8829_CFG_GPIO_4 register

Addr: 0x84	TMF8829_CFG_GPIO_4					
Field	**Name**	**Rst**	**Type**	**Description**		
2:0	*gpio4*	0	RW	SCL (respectively GPIO4) output control - setting will be ignored if this pin is used as I²C/I3C SCL interface pin unless *gpio4_func*=0		
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (i.e. If high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.59 TMF8829_CFG_GPIO_5 (Address 0x85)

Table 103: TMF8829_CFG_GPIO_5 register

Addr: 0x85 **TMF8829_CFG_GPIO_5**

Field	Name	Rst	Type	Description		
2:0	*gpio5*	0	RW	SDA (respectively GPIO5) output control - setting will be ignored if this pin is used as I²C/I3C SDA interface pin unless *gpio5_func*=0		
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (i.e. If high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.60 TMF8829_CFG_GPIO_6 (Address 0x86)

Table 104: TMF8829_CFG_GPIO_6 register

Addr: 0x86	TMF8829_CFG_GPIO_6				
Field	**Name**	**Rst**	**Type**	**Description**	
2:0	*gpio6*	0	RW	INT/GPIO6 output control - setting will be ignored if this pin is used as INT interface pin unless *gpio6_func*=0	
				Code	**Symbol**	**Function**
				0	TRISTATE	Pin is in tristate
				1	INPUT_IR	Input and VCSEL emission follows logical level (i.e. If high, VCSEL is on, else off)
				2	INPUT_ACTIVE_HIGH	Input allow VCSEL operation active high
				3	INPUT_ACTIVE_LOW	Input allow VCSEL operation active low
				4	OUTPUT_LOW_VCSEL_PULSING	VCSEL signaling output active low
				5	OUTPUT_HIGH_VCSEL_PULSING	VCSEL signaling output active high
				6	OUTPUT_HIGH	Output logic high
				7	OUTPUT_LOW	Output logic low

8.2.61 TMF8829_CFG_GPIO (Address 0x87)

Table 105: TMF8829_CFG_GPIO register

Addr: 0x87	TMF8829_CFG_GPIO					
Field	**Name**	**Rst**	**Type**	**Description**		
1:0	*pre_delay*	0	RW	Output of VCSEL pulsing will be asserted with *pre_delay* time before the VCSEL starts emitting - OUTPUT_LOW_VCSEL_PULSING or OUTPUT_HIGH_VCSEL_PULSING – applies for any of the above GPIOs 0-6 using this setting.		
				Code	**Symbol**	**Function**
				0	NO_PREDELAY	No delay
				1	d_100_US_PREDELAY	100 µs pre-delay
				2	d_200_US_PREDELAY	200 µs pre-delay

8.2.62 TMF8829_CFG_I2C_ADDRESS (Address 0x90)

Table 106: TMF8829_CFG_I2C_ADDRESS

Addr: 0x90		TMF8829_CFG_I2C_ADDRESS		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*i2c_slave_address*	130	RW	The unshifted I²C slave address for I²C communication – The LSB is automatically set by direction of communication.

8.2.63 TMF8829_CFG_MOTION_DETECT_DISTANCE_LSB (Address 0xB0)

Table 107: TMF8829_CFG_MOTION_DETECT_DISTANCE_LSB register

Addr: 0xB0		TMF8829_CFG_MOTION_DETECT_DISTANCE_LSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*motion_distance[7:0]*	208	RW	LSB of Distance in UQ2 [0.25 mm], which is considered as motion if motion detection is enabled (*post_processing*=1). Default is 50cm = 500mm *4 = 2000, (7*256 + 208)=2000

8.2.64 TMF8829_CFG_MOTION_DETECT_DISTANCE_MSB (Address 0xB1)

Table 108: TMF8829_CFG_MOTION_DETECT_DISTANCE_MSB register

Addr: 0xB1		TMF8829_CFG_MOTION_DETECT_DISTANCE_MSB		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*motion_distance[15:8]*	7	RW	MSB of Distance in UQ2 [0.25 mm], which is considered as motion if motion detection is enabled (*post_processing*=1). Default is 50cm = 500mm *4 = 2000, (7*256 + 208)=2000

8.2.65 TMF8829_CFG_MOTION_DETECT_SNR (Address 0xB2)

Table 109: TMF8829_CFG_MOTION_DETECT_SNR register

Addr: 0xB2		TMF8829_CFG_MOTION_DETECT_SNR		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*detect_snr*	10	RW	Detect SNR motion threshold. Set *detect_snr* > *release_snr* to avoid oscillating pixels for motion detection toggling between detect / no detect.

8.2.66 TMF8829_CFG_MOTION_RELEASE_SNR (Address 0xB3)

Table 110: TMF8829_CFG_MOTION_RELEASE_SNR register

Addr: 0xB3		TMF8829_CFG_MOTION_RELEASE_SNR		
Field	**Name**	**Rst**	**Type**	**Description**
7:0	*release_snr*	6	RW	Release SNR motion threshold. Set *detect_snr* > *release_snr* to avoid oscillating pixels for motion detection toggling between detect / no detect.

8.2.67 TMF8829_CFG_MOTION_ADJACENT_PIXEL (Address 0xB4)

Table 111: TMF8829_CFG_MOTION_ADJACENT_PIXEL register

Addr: 0xB4		TMF8829_CFG_MOTION_ADJACENT_PIXEL		
Field	**Name**	**Rst**	**Type**	**Description**
3:0	*motion_adjacent*	8	RW	Number of adjacent pixels with motion to be considered as motion detected. Maximum value is 15 (to limit stack usage)

8.3 Bootloader registers *appid* = 0x80

See document “TMF8829 Host Driver Communication” for a detailed description.

In bootloader mode, registers 0x00 (TMF8829_APP_ID), 0x01 (TMF8829_MAJOR), and all hardware registers from 0xE0 (I2C_DEVADDR) onward are accessible. Registers 0x08 to 0x0F perform different functions as detailed in the table below.

Table 112: Bootloader registers

Address	Register name	Value/Range	Meaning
0x08	CMD_STAT	See next table	Setup FIFO upload
0x09	PAYLOAD	0 or 6	Size of command payload
0x0A	ADDRESS0	0..0xff	Address LSB
0x0B	ADDRESS1	0..0xff	
0x0C	ADDRESS2	0..0xff	
0x0D	ADDRESS3	0..0xff	Address MSB
0x0E	WORD_SIZE0	0..0xff	Word size LSB
0x0F	WORD_SIZE1	0..0xff	Word size MSB

The Register 0x08 (CMD_STAT) supports following commands in bootloader mode:

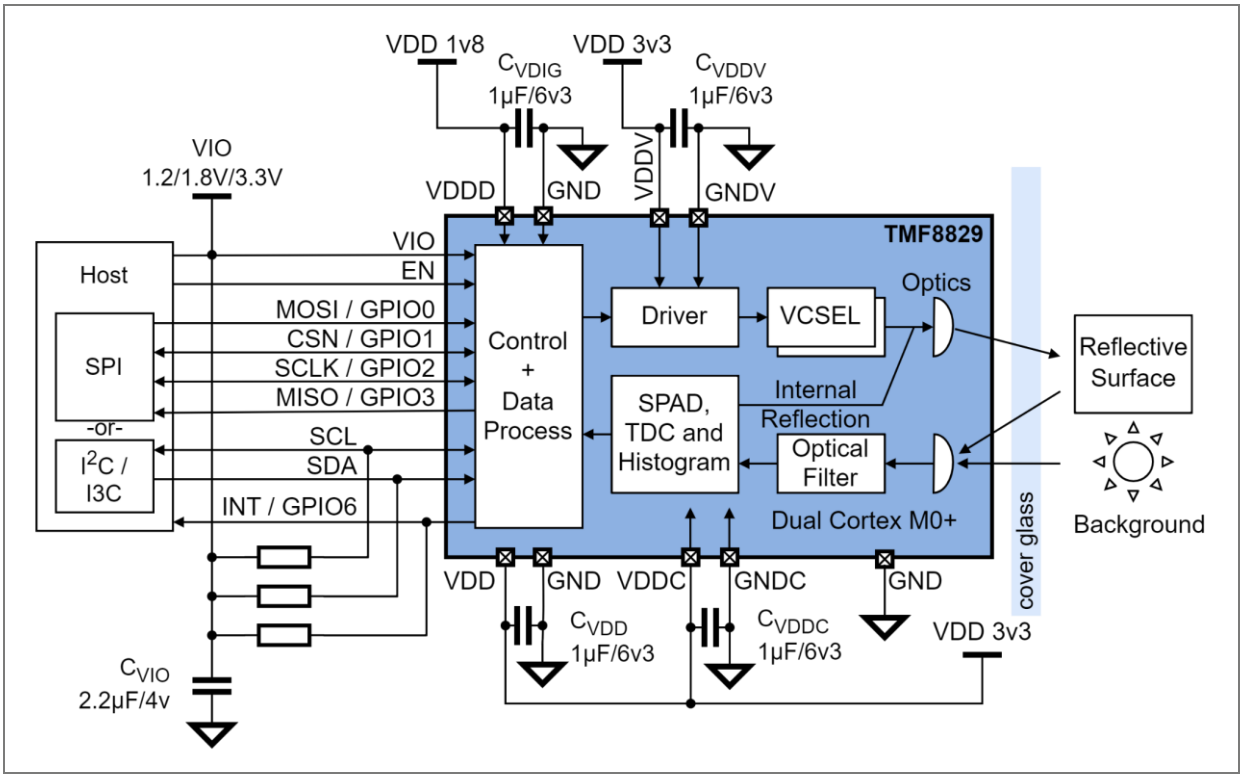
Table 113: Boot-monitor commands

Code (decimal)	Symbol	Function
22	BL_CMD_START_RAM_APP	Start the RAM application
32	BL_CMD_SPI_OFF	Disable SPI interface
34	BL_CMD_I2C_OFF	Disable I²C/I3C interface
69	BL_CMD_W_FIFO_BOTH	Setup size for FIFO writes to both CPU RAM’s in parallel
All other not specified values shall not to be used and the behavior if one of them is set, is undefined.		

9 Application information

9.1 Schematic

Figure 23: Application circuit diagram



The TMF8829 is using following supplies for operation:

- VDD 3v3 – Main supply voltage for the internal analog blocks and VCSEL driver.
- VDD 1v8 – Digital supply. It is recommended to use a DCDC converter to power this supply. If a DCDC converter is not available, this supply can be connected to VDD 3v3 as well, but this will increase system power consumption.
- VIO – 1.2, 1.8 or 3.3V – I/O supply voltage, the I/O pads I²C/I3C (SCL, SDA), the SPI interface (MOSI/GPIO0, CSN/GPIO1, SCLK/GPIO2, MISO/GPIO3), all GPIO pins, interrupt pin (INT/GPIO6) and enable pin (EN).
  VIO shall be present if any of these pins are powered. VIO does not draw current if the other supplies are disabled (VDD 3v3 and VDD 1v8 = 0V), see $I_{VIO\_VDD\_OFF}$.

Table 114: External components

Symbol	Order code	Value	Manufacturer	Size
C_{VDDV}, C_{VDDC}, C_{VDDC}, C_{VDDD}	GRM155R70J105KA12	1 µF, 6.3V, X7R Worst case >= 0.5µF @ 2.6V >= 6.3V voltage rating	Murata	0402 (1005M)
C_{VIO}	GRM033R60J225ME47	2.2 µF, 4V, X5R Worst case >= 0.6µF @ 2.6V >= 4V voltage rating	Murata	0201 (0603M)

9.1.1 Operating several TMF8829 devices on a single I²C/I3C bus

9.1.1.1 I3C

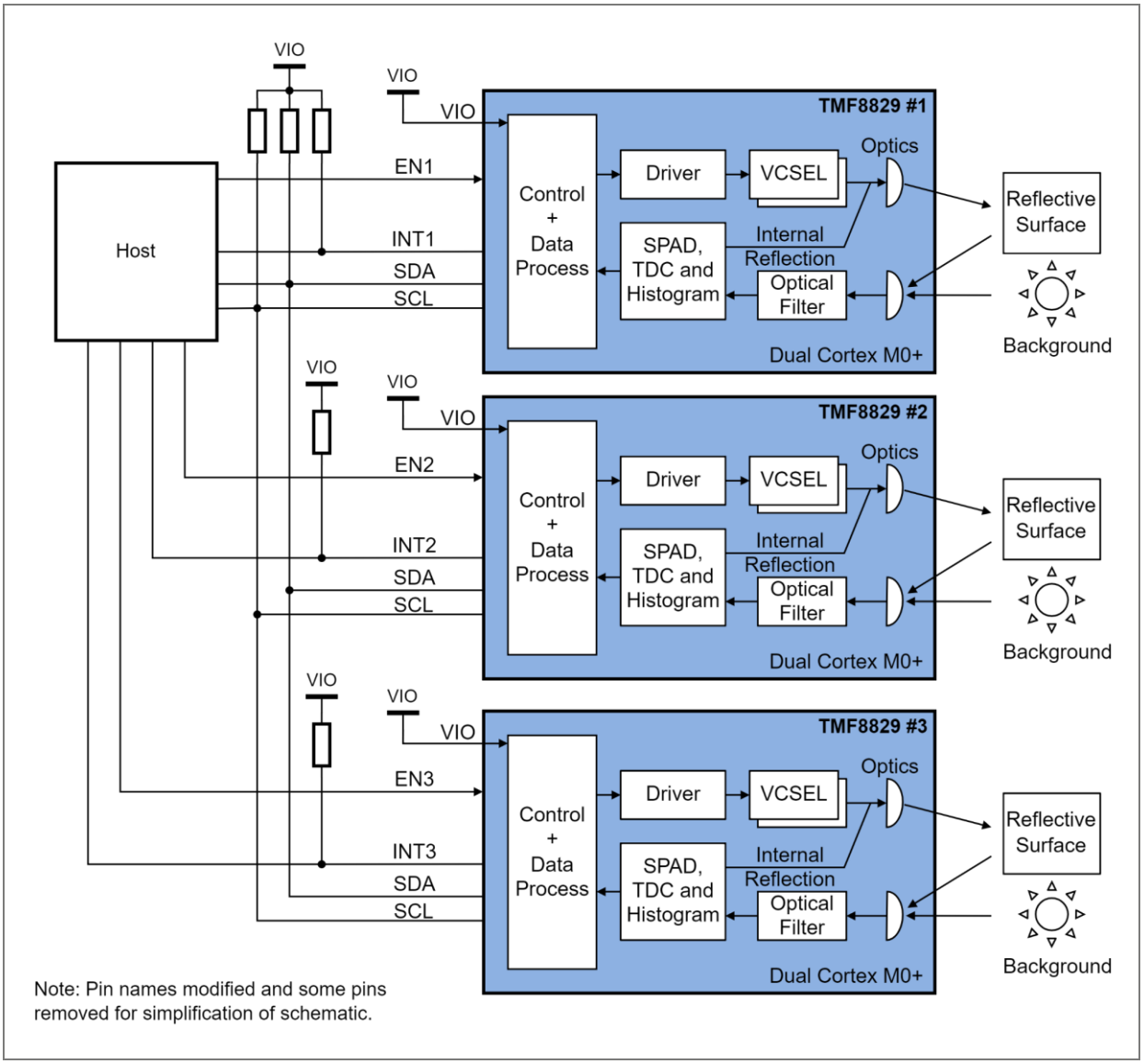
I3C already supports connecting several TMF8829 devices in parallel to a shared bus as I3C has an address arbitration concept, which supports this feature. To identify the physical location of one of the devices, you can utilize the GPIO pins.

Example: Device A has connected MOSI/GPIO0 to VDD, device B has connected MOSI/GPIO0 to GND. Reading MOSI/GPIO0 pin value through the I3C bus (register *gpio_value_0*) can now clearly identify which device is device A (logic H) respectively device B (logic L).

9.1.1.2 I²C

Several TMF8829 devices can share a single I²C bus if there are dedicated enable (EN) connections to each of these devices.

Figure 24: Sharing a single I²C bus for operating several TMF8829's



The procedure to initialize the devices to different I²C addresses is as follows:

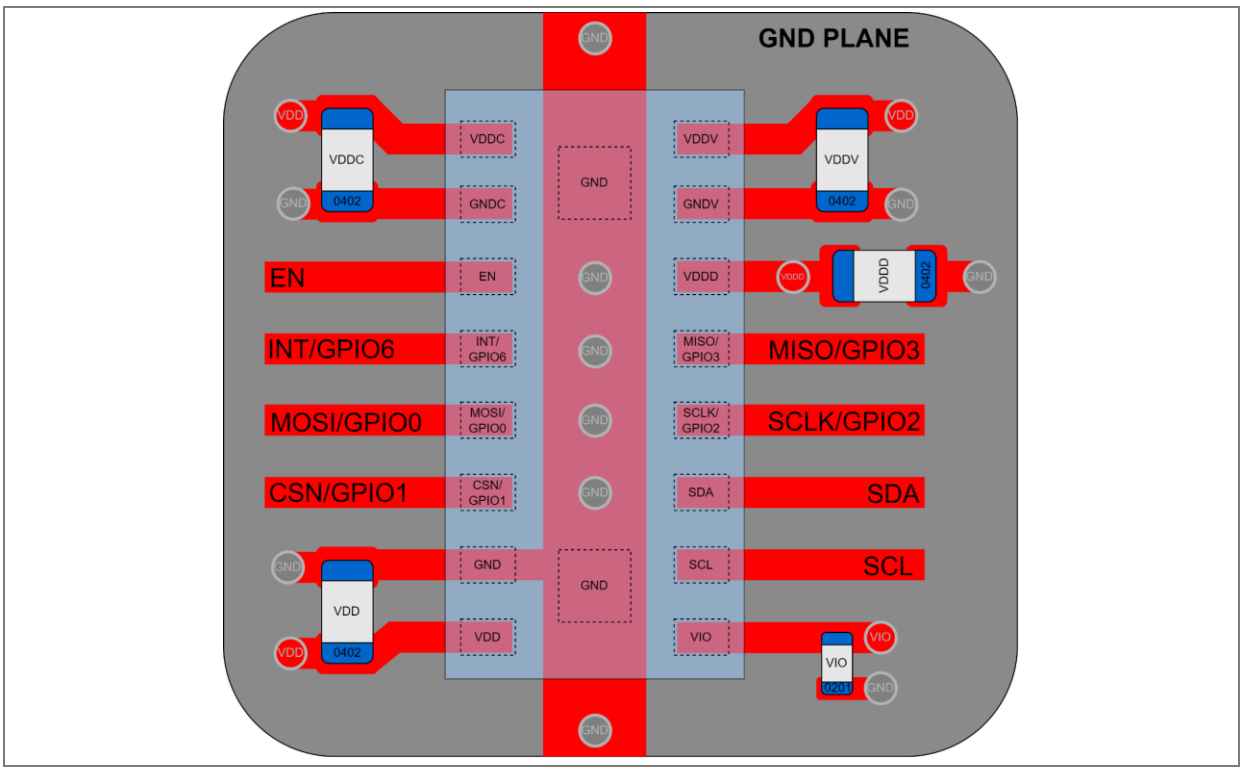
1. Set EN1=0, EN2=0, EN3=0 (reset all devices)
2. Set EN1=1
3. Startup first TMF8829 in I²C/I3C mode
4. Reprogram I²C address for first TMF8829 by setting *i2c_devaddr* = I²C address for first TMF8829
5. Set EN2=1
6. Startup second TMF8829 in I²C/I3C mode
7. Reprogram I²C address for second TMF8829 by setting *i2c_devaddr* = I²C address for second TMF8829
8. Set EN3=1
9. Startup third TMF8829 in I²C/I3C mode
10. Reprogram I²C address for third TMF8829 by setting *i2c_devaddr* = I²C address for third TMF8829
11. If there are further devices, repeat the last three steps accordingly.

Information:

With setting of EN=0, the programmed I²C address returns to the default address.

9.2 PCB layout

Figure 25: PCB layout recommendation



Use a ground plane to connect all GND's together as shown in Figure 25 above.

9.3 PCB pad layout

Use the same size and location of the package pads shown in Figure 25 as PCB pads – this is a recommendation only. The actual pad layout shall be optimized for the customer production line.

9.4 Calibration and crosstalk

The TMF8829 is already calibration at ams OSRAM production site, see section 7.5.1. In an application, the crosstalk needs to meet the requirements defined by the ams OSRAM optical design guide (ODG) available on the ams-osram.com website:

- Optical design guide

9.5 Software drivers

ams OSRAM recommends using one of the available software drivers to operate the TMF8829. The drivers are available from the ams-osram.com website and github.com/ams-OSRAM:

- ams-osram.com/tmf8829

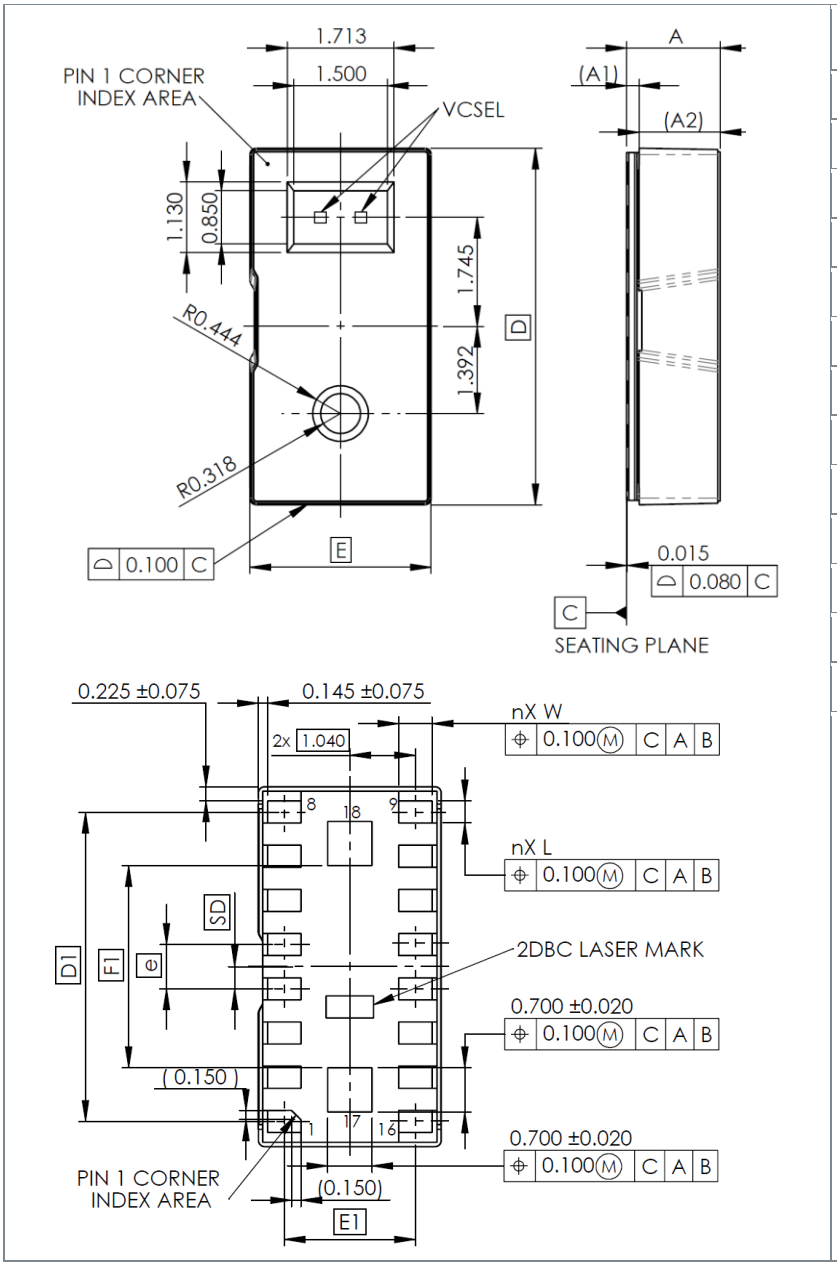
The following drivers are available:

Table 115: Software drivers

Type	File	Explanation
Arduino	TMF8829_Driver_Arduino_Source_v*.zip github.com/ams-OSRAM/tmf8829_driver_arduino	C source code driver intended to be easy portable to any other platform. This is the driver used for the TMF8829 shield EVM TMF8829_EVM_EB_SHIELD board if piggy-packed on an Arduino Uno (not included).
Python	TMF8829_Driver_Python_Source_v*.zip github.com/ams-OSRAM/tmf8829_driver_python	Python driver. This is the driver used for the TMF8829 shield EVM TMF8829_EVM_EB_SHIELD board if directly connected to the PC through processor used as interface chip. The processor chip is included with the TMF8829 shield EVM board and pre-programmed before delivery.
Linux	TMF8829_Driver_Linux_v*.zip and TMF8829_Driver_Linux_Source_v*.zip github.com/ams-OSRAM/tmf8829_driver_linux	Use for any Linux system (e.g. Android) where the driver is running on the application processor. This is the driver running on TMF8829 demo kit - TMF8829_EVM_DB_DEMO.

10 Package drawings & markings

Figure 26: Package outline drawing

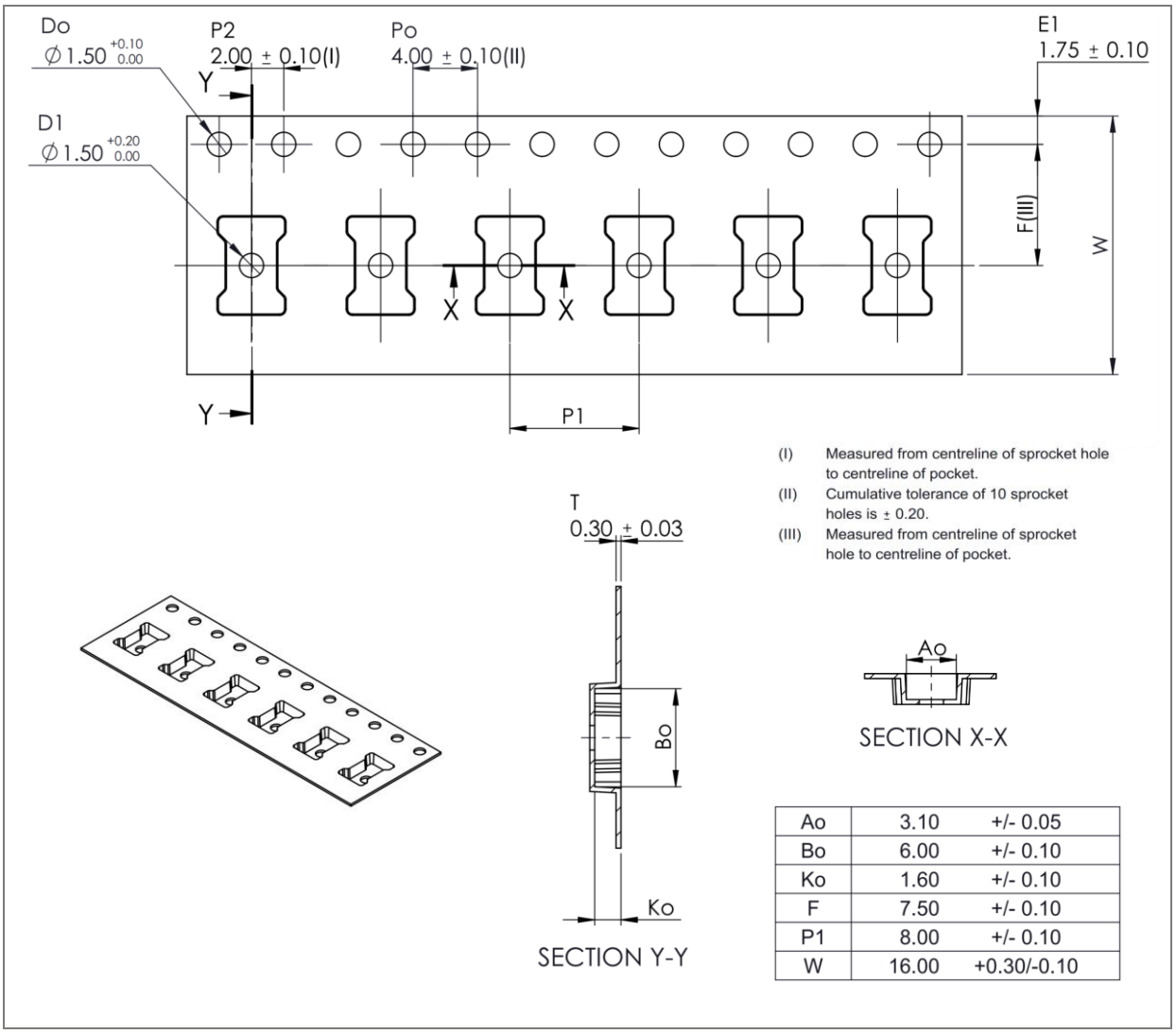


Ref	Min	Nom	Max
A	1.460	1.5	1.540
A1		0.2	
A2		1.3	
D	5.675	5.7	5.750
E	2.875	2.9	2.950
W	0.510	0.530	0.550
L	0.330	0.350	0.370
e		0.7	
n		16	
D1		4.900	
E1		2.080	
SD		0.350	
F1		3.200	

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) n is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.
(6) 2DBC unique tracecode only on bottom side of the package.

11 Tape & reel information

Figure 27: Tape and reel drawing



Ao	3.10	+/- 0.05
Bo	6.00	+/- 0.10
Ko	1.60	+/- 0.10
F	7.50	+/- 0.10
P1	8.00	+/- 0.10
W	16.00	+0.30/-0.10

(1) All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
(2) The dimensions on this drawing are for illustrative purposes only. The dimensions of an actual carrier may vary slightly.
(3) Symbols on drawing A0, B0, and K0 are defined in ANSI EIA Standard 481-B 2001.
(4) There are two-reel sizes available (see section 2).
  i) 7″ reels: Each reel is 7 inch in diameter and contains 500 parts.
  ii) 13″ reels: Each reel is 13 inch in diameter and contains 3500 parts.
(5) ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481-B.
(6) In accordance with EIA standard, device pin 1 is located next to sprocket holes in the tape.
(7) This drawing is subject to change without notice.

12 Soldering & storage information

12.1 Soldering information

The package has been tested and has demonstrated the ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these tests are detailed below.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 28: Solder reflow profile graph

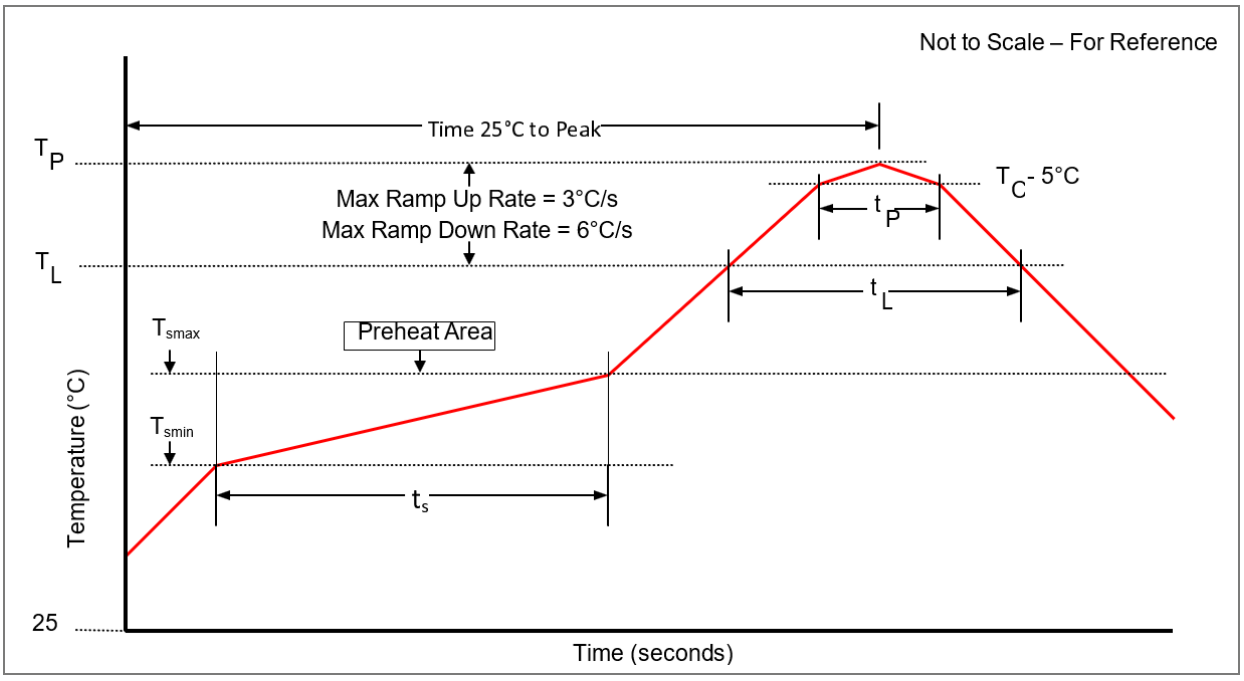


Table 116: Solder reflow profile

Parameter	Value
Temperature Min (T_{smin})	150°C
Temperature Max (T_{smax})	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp of 260°C. For suppliers T_P must equal or exceed the classification temp of 260°C
Time (t_P)(1) within 5°C of the specified classification temperature (T_c)	30 (1) seconds
Ramp-down rate (T_P to T_L)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

(1) Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

12.2 Storage information

Moisture sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package.

To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40 °C
- Relative Humidity: <90 %

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60 %

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking instructions

When the shelf life or floor life limits have been exceeded, rebake at 50 °C for 12 hours.

13 Laser eye safety

The TMF8829 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC / EN 60825-1:2014, EN 60825-1:2014+A11:2021 and Class 1 consumer laser product according to EN 50689:2021. This applies to the stand-alone device and the included software supplied by ams OSRAM. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions. Use outside of the recommended condition or any physical modification to the module during development could result in hazardous levels of radiation exposure.

Figure 29: Laser eye safety certificate

IEC 60825-1:2014,
EN 60825-1:2014+A11:2021 and
EN 50689:2021

Complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

CAUTION:

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Example: Adding a converging lens on top of the TMF8829.

14 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade

Other definitions

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A short datasheet is intended for quick reference only, it is an extract from a full datasheet with the same product number(s) and title. For detailed and full information always see the relevant full datasheet. In case of any inconsistency or conflict with the short datasheet, the full datasheet shall prevail.

Changes from previous released version to current revision v2-00	Page
Document security class is updated as “PUBLIC” in the footer	
Clarified 2DBC position	8, 92
Improved t_{SPI_H} and t_{SPI_L} timings.	14
Update performance parameters	16
Removed *min_distance_uq*	25, 70, 71
Added section motion detection	27
Added device orientation diagram	35
i2c_devaddr is RO, updates shall be done with *i2c_slave_address*	47
Added *int2/3* and *int2/3_enab* register.	47, 48
poff enters standby mode (corrected)	52
Added *hv_cp_overload_detect*	68
Added *post_processing* mode 2	73
Added *prox_distance*	74
Updated package D and E tolerances and added exact location of apertures and GND pads	94

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal information

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