Product Document

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Application Note

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ams Optical Sensors Design Recommendations

System EMI and ESD

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Content Guide

1 Introduction

The electromagnetic interference (EMI) problem is between an emission culprit and susceptible victim which are coupled through a means, either radiation through space or conducted through wires or PCB traces. The optical sensors from **ams** use both analog and digital circuits so attention to basic EMI prevention measures are critical to achieve the best performance for sensors, and to pass EMC regulatory requirements for the systems with these sensors being designed in.

Electrical current flowing in a wire or PCB trace creates a magnetic field that can couple into nearby traces. This is more pronounced in high frequency signals, but even low frequency clock signals can contain high frequency components. In addition, digital circuits can create high frequency bursts when switching states. This app note is intended to cover circuits with **ams** optical sensors, and therefore does not cover all aspects of High Speed PCB design. For **ams** optical sensors, the frequencies of their internal clock sources can be as high as several megahertz. And the clock used by the sensor I^2C block can reach a maximum speed of 1 MHz. For **ams** Time of Flight (ToF) family parts, the internal CPU clock can be as high as 80 MHz.

The three main methods to reduce EMI noise from affecting the sensor output data that will be discussed in this app note are proper grounding, good PCB / FPC layout, and power supply filtering.

System design for ESD is always challenging especially for handheld devices like smart phones. While the same design rules preventing EMI issues can apply to rules preventing ESD issues, special care needs to be taken for certain specific system designs with certain specific **ams** sensor parts.

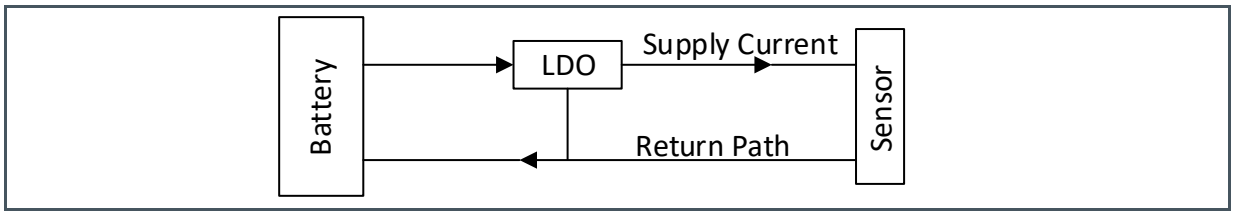
This document serves mainly as practical recommendations of system designs with **ams** optical sensors for EMI/ESD considerations. A comprehensive EMI/ESD tutorial is beyond the scope of this document.

2 Preventing EMI Issues

2.1 Proper Grounding

The most important precaution in any design that will reduce the noise, including EMI, is to have proper grounding in the circuit and system. The ground in a circuit is the base voltage that all other voltage levels are referenced. Care must be taken to ensure that all circuits are operating at the same ground level. When considering EMI the ground must be thought of as a return path for the circuit current rather than just a ubiquitous 0 V level. In mobile devices, this means a path from the sensor all the way back to the battery. It is a good idea to remember that every bit of current used by the sensor and IR LED must travel in a path through the ground back to the battery.

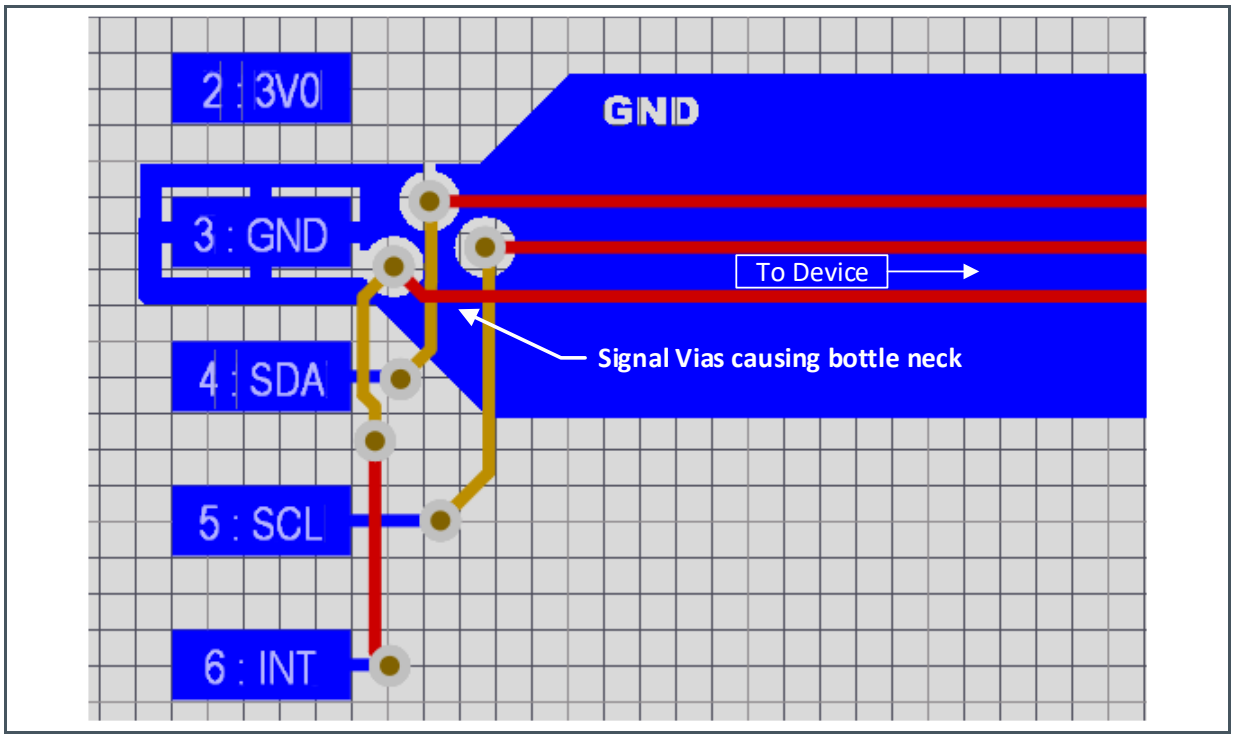
Figure 1 :
System Current Path



The impedance between the sensor ground and battery should be minimized. There should be no series elements placed in the ground path between the sensor and the power supply return. Any series element that adds impedance in the ground path can cause noise that may affect the accuracy of the measurements. Inductive elements are the most problematic, because the impedance increases with frequency. If any inductive elements are introduced for the purposes of isolation, they should be placed in series with the VDD signal and not with the GND signal. This approach provides isolation without causing noise, EMI, and ESD issues. Since most EMI noise consists of high frequency components series inductive elements in the return path should be avoided. The pulsing of an LED or VCEL for proximity sensors will have high speed transients that can cause noise if there is inductance in the ground path.

As with most components, **ams** optical sensor devices should be connected to ground as close to the device as possible. In multi-layered PCBs, an unbroken ground plane provides the best method for low impedance return signal path. Adding a flooded copper pour to the top and bottom of the PCB adds additional grounding, but vias should still be added near to the device to quickly connect the return signal to an inner ground plane or to the bottom copper pour. Using multiple vias will also reduce the ground path impedance as described in the next section. On PCBs where there is no ground plane the number of non-ground vias in the ground path should be minimized. This can cause a bottle neck and be a source for noise as shown in Figure 2.

Figure 2 :
Bad Layout Example Where Signal Vias Cause Grounding Issues



In a system where multiple pieces of test equipment are used, such as a laptop, development system (i.e. Raspberry Pi), and EVM; each system's ground needs to be connected together. This ensures all the systems are working with the same reference, otherwise differences in ground levels could cause noise in the readings.

2.2 Proper PCB / FPC Layout

Proper circuit layout is critical for EMI reduction. The PCB itself has to be considered as part of the circuit rather than just a means of connecting different components. Since EMI is caused by the magnetic field produced by electric current flowing in a wire or PCB trace, reducing the magnetic field will reduce the EMI noise. Placing the return path trace close by will create an opposite magnetic field and both fields will cancel each other out and will greatly reduce or cancel the noise. Many EMI issues are resolved through proper routing of the ground return path such that it flows near the signal path. One example in multi-layer boards is to place a ground via next to a supply via to reduce noise created by current flowing through the supply via.

PCB traces are also not free of impedance. The copper cross sectional area and the length of the trace are controllable parameters that will impact the trace resistance for DC signals. The PCB dielectric thickness and copper geometry are controllable parameters that affect the trace impedance for high frequency signals. This is one reason the bypass and filter components should be placed as close as possible to the device. It is also a good idea to connect the ground pins to the PCB ground as close as possible for the same reason.

Vias are useful for connecting signals between PCB layers, but they also act as a passive component by adding resistance, inductance, and even some capacitance in the signal path. In the example shown below in Figure 3 and Figure 4, vias with 8mil drill and 18mil pads are used. Each via adds approximately 1.33 nH in the path. While this is not much, it can add up if several vias are needed to get to the source. If this is an issue and space is available, multiple vias can be used in parallel to reduce the total impedance since they add together like inductors. The inductance of a via is reduced as the drill hole diameter increases which is another method for controlling impedance.

A suggested schematic and layout for the TCS3701 is shown below in Figure 3 and Figure 4. The TCS3701 is a color sensor, but it can also control an external LED for proximity functionality as it is configured below. The VDD bypass caps are place close to the VDD pin. An additional 10 µF cap should be placed near the LED anode (not shown). While there is no internal LED in the part, the VDD pi filter is used because it is configured to sink an external LED current.

Figure 3:
TCS3701 Sample Schematic

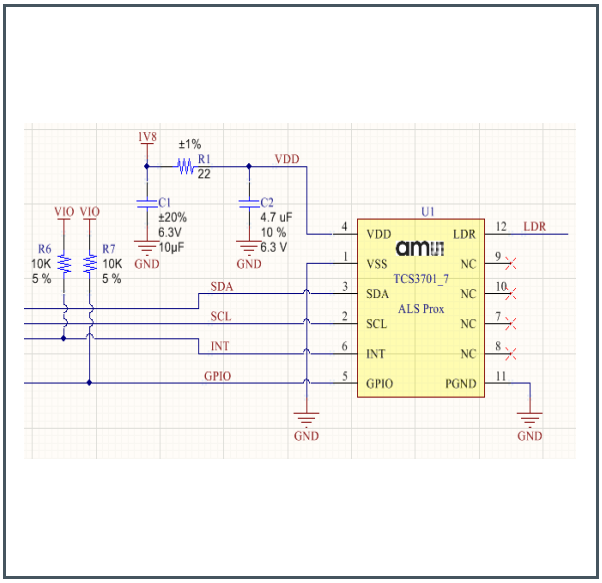


Figure 4:
TCS3701 Sample Layout

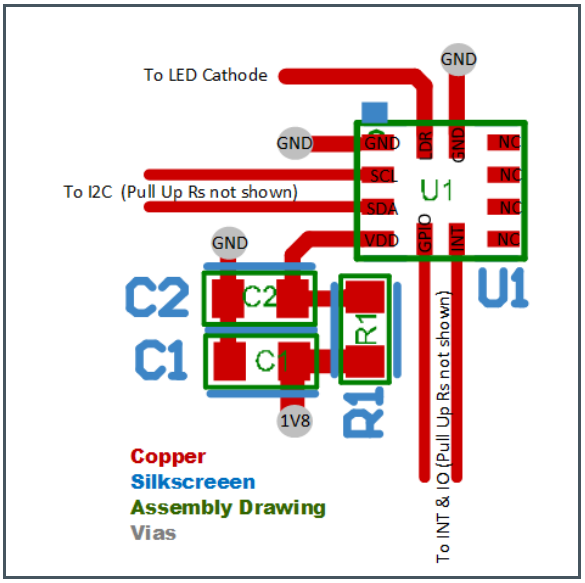


Figure 5 and Figure 6 show a suggested schematic and layout for a TCS3701 which is a color and proximity module. This circuit shows the LEDA bypass cap as well as the interrupt pull up resistor which can be pulled up to the system IO voltage.

Figure 5:
TCS3701 Proximity Circuit Example Schematic

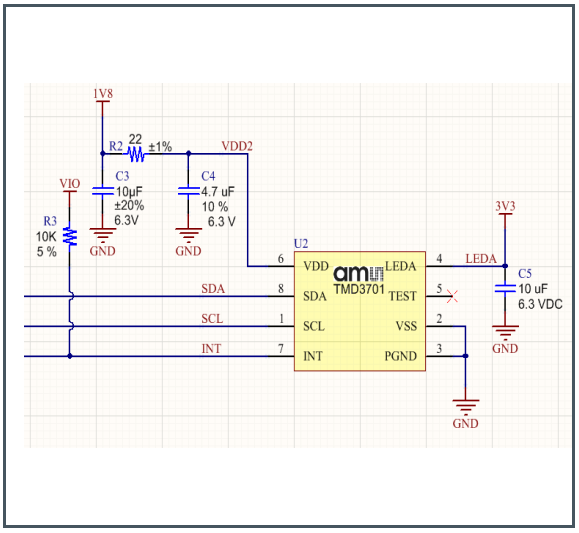
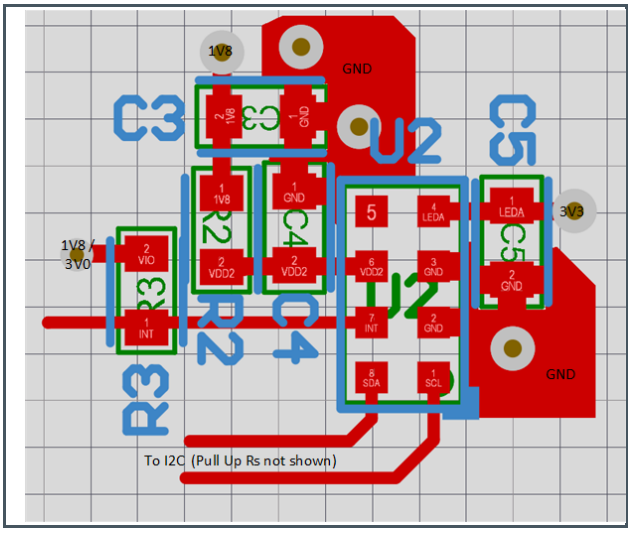


Figure 6:
TCS3701 Proximity Circuit Layout Example



I²C pull up resistors are placed near the I²C source, but if there are long traces this can be a source of EMI since it contains a clock signal. The pull up resistor values are based on the I²C clock speed, but may need to be modified to ensure the acknowledge signal is at the correct level back at the source. Noise on the I²C bus can be addressed with either a small RC filter on the signal or by decoupling the pull up resistor supply by adding a ferrite bead and bypass caps.

Flex circuits are widely used in mobile devices and creates additional layout considerations. Flex circuits can cause extra concern by adding longer trace lengths to the supply and ground traces. Similar to a PCB, adding a ground plane on the flex is the best method for a ground return path. On flex circuits that do not have a ground plane the routing of the ground should provide a low impedance return path for all current. The supply and return current should be routed close together to reduce the impact of external noise as well as to reduce EMI issues. If the LED pulse current generates EMI noise from the flex, it may be helpful to route the LEDA and PGND signals together to the flex connector before joining PGND to the system GND. This is not necessary for the operation of the sensor however. The insertion loss due the flex connector should not be ignored and in general there should be more ground pins than supply pins in order to keep the ground impedance low.

2.3 Bypass Filters

Bypass filters are a key component in both reducing negative effects from EMI as well as filtering noise from a power supply. The bypass filters help clean the power supply signal as well as prevent the device from creating noise on the supply voltage. Power supply filtering should always be placed on the supply side of the circuit and not on the ground side. The exact type and value of the bypass filter components are dependent on the system which the sensor is designed in. Systems with a clean power supply running from an LDO by itself may be able reduce the filter values. Systems with many

devices all running off the same switching power supply may need additional filtering. When using an **ams** sensor without proximity function, a 0.1 µF bypass capacitor on the VDD pin is recommended and is usually sufficient in most systems. For the **ams** modules that have both ALS and proximity functionality, a pi filter is recommended on the VDD as shown in Figure 3 and Figure 5 above. An additional 10 µF cap on the LED anode (LEDA) pin is also recommended. In noisy systems, an additional a 0.01 µF bypass capacitor on the VDD pin or a series ferrite bead before the caps may help clean the supply rail. As previously stated the filter components should be placed as close to the VDD pin as possible.

2.4 Specific Consideration for GSM Transmitter Interferences

GSM RF bands are still required for most smart phone models in the market. Sensor samples are mounted and tested on EMI evaluation boards to pass **ams** internal RF immunity requirements. For ALS-proximity sensors, ADATA/PDATA variations are logged for conducted or radiated immunity tests when injecting GSM900 frequency band RF signals to the sensor under test at pre-defined conducted or radiated levels. Since customers are moving toward more aggressive phone IDs in which the ALS-proximity sensor is placed extremely close to RF antenna, some EMI issues are reported when GSM low band transmitter being turned on around maximum level (33 dBm).

One EMI issue is that GSM RF signal being coupled to I^2C SCL/SDA lines may cause the internal registers to corrupt, hence sensor malfunctioning. To address the issue, ceramic capacitors of around 33 pF needs to be added to each I^2C signal line to bypass the low band GSM signal.

Another EMI issue is that PDATA will have a huge jump due to the radiated low band GSM signal. The theory is that VDD line is polluted and proximity AFE block is affected. It is recommended to add a ceramic capacitor of around 33 pF to VDD line to bypass the GSM signal. For layout, use short/wide traces to connect the capacitor to VDD pin and VSS pin to reduce the line inductance. It is also recommended to use EMI film on the top and bottom layers of sensor PCB to provide additional shielding.

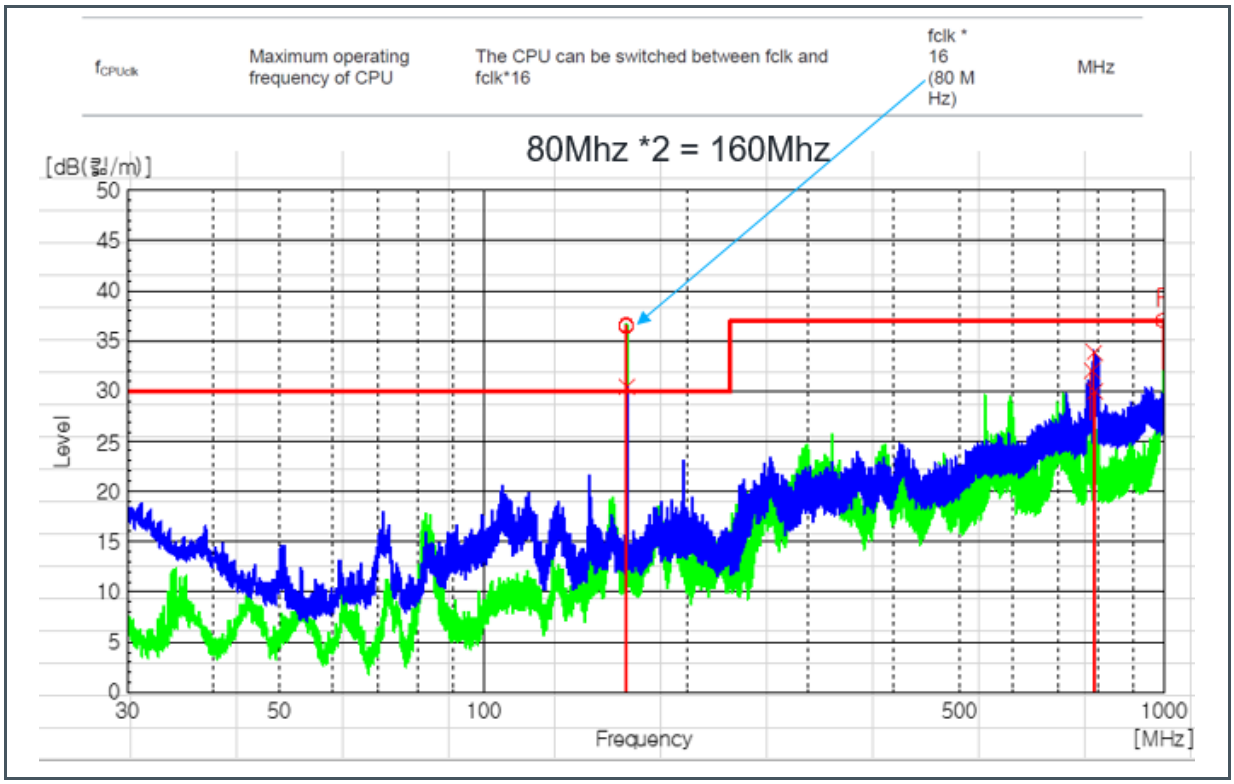
2.5 Specific Consideration for Time of Flight (ToF) parts

As mentioned in the introduction section, the internal CPU clock of **ams** ToF family parts (TMF8701, TMF880x and TMF882x) can be as high as 80 MHz which runs 16x PLL off from an internal oscillator of 5MHz. The CPU clock of 80 MHz and its harmonics can be very problematic because it not only can interfere internally with circuit components and functions in the system, but also with other equipment in the vicinity of the source.

All commercially launched electronic products need to meet radiated emission (RE) limits set by regulatory standards (e.g FCC Part 15 or CISPR 22). There is usually no issue for products with **ams** ToF parts to pass these RE limits as long as designers follow disciplined design practice for EMI. However, pitfalls do exist in some application cases. For an example in TV set design, there is usually a circuitry block called front assembly, which includes functions such as IR receiver for remote, microphone, side-tact-key, ALS and LEDs. Due to low signal speed nature of these functions, a 2-layer stackup of rigid PCB is usually used with a long and slim PCB outline. When an **ams** ToF part

was designed into a new TV front assembly, the 2-layer PCB became insufficient for passing RE limits. Figure 7 below shows RE test failed at 160 MHz with a 2-layer PCB design.

Figure 7:
RE Test Failed at 160 MHz



The issue with the 2-Lyer PCB design is there is no room to designate one layer as a solid ground plane to shield the CPU clock signal. With its long and slim board outline (e.g. 125 mm x 7.9 mm from an actual design) and a B2B connector at one end to connect the front assembly to the mother board, all supply and Ground routing become long traces which surely have very high inductances. All bypass capacitors become ineffective due to high inductance on the ground returns.

After changing the PCB stackup to 4-layer, the PCB routing can now follow recommendations described on Section 2.1 to 2.3 of this document, especially one inner layer is designated as ground plane. The new samples now can pass RE limits without any issue.

So it is recommended to use 4-layer PCB whenever possible especially for designs with odd board outline (e.g. long and slim).

2.6 EMI Design Guideline Summary

EMI noise is caused by signal coupling from one device or trace to another can cause several issue from misread data to inaccurate measurements. Optical sensors from **ams** are mixed-signal devices and therefore basic EMI suppression guidelines should be followed:

- Good Grounding is the most important aspect for EMI prevention.
- There should be no series components in the ground path.
- The complete ground path should be considered which goes from the device back to the power supply / battery.
- When multiple system are used in testing or development, their grounds should all be connected together.
- The PCB is a component and the effects of trace widths and vias should be taken into account during layout.
- Vias add inductance and in series should be minimized in the ground path. However when placed in parallel they will reduce inductance.
- The best ground for a multi-layer PCB is an unbroken ground plane.
- Flex circuits can introduce longer ground path lengths and should be routed with EMI in mind.
- Bypass components should be placed as close to the sensor as possible.
- Filter and bypass components should be placed on the high side of the circuit.
- Special cares need to be taken for mobile designs with high power GSM transmitters.
- Special cares need to be taken for designs with **ams** ToF parts with high CPU clock frequency.

3 Preventing ESD Issues

3.1 ESD Topic Background

There are ESD standards such as Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM) developed for manufacturing environment ESD protection requirement. The HBM ESD voltage range often seen in a device specification defines a component-level ESD protection class level (e.g. HBM voltage range from 2 KV to <4 KV for a Class-2 device).

The more stringent IEC standard allows system designers to identify and correct ESD vulnerability of electronic products under real-world ESD stress conditions. It became very important in the ever changing application environment with the proliferation of handheld devices like smart phones. The IEC 61000-4-2 standard uses two different testing methodologies, contact discharge and air discharge. The standard defines four levels of ESD protection. However, mobile device makers can have their ESD level requirements based on their business requirements. ESD test benches and ESD discharge guns, according to IEC 61000-4-2 standard, are usually equipped in their system ESD test labs.

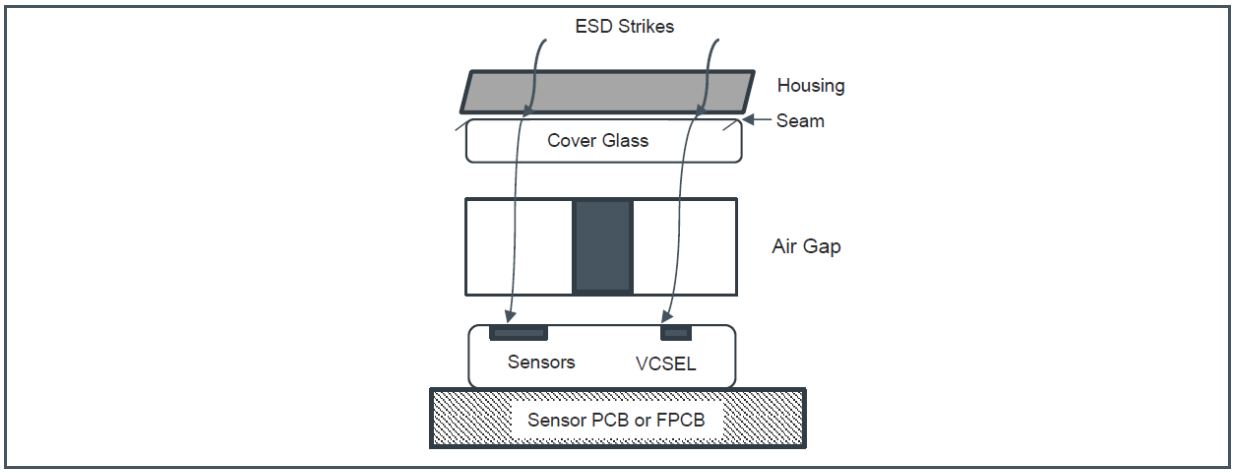
System designers need to understand that the ratings, such as HBM, are only used for protecting ICs in the manufacturing environment and are not equivalent to system level ESD tests defined in the more stringent IEC 61000-4-2 standard for systems in end user environments. ESD protection is required in a system design for a component potentially being exposed to ESD discharges.

3.2 ESD Design Guideline for ams Sensor Parts

The rise-time of an ESD pulse as defined in IEC 61000-4-2 is in the order of 1 ns which implies its effective upper frequency component can be as high as 500 MHZ. So, the same design rules described in Section 2, preventing EMI issues with proper grounding, PCB/FPCB layout, and bypass filters on supplies, are generally applied to system designs for ESD protection as well. For systems in which **ams** parts have high chance being exposed to ESD discharge in a system ESD Lab test or end user environment, extra care in the system design must be taken to improve ESD immunity. They must not only pass the ESD lab test requirement, but also improve the reliability of products in field.

For example, in smart phone design, ALS/Proximity parts are usually placed under the display bezel area. In the past, these parts are behind cover glass and well shielded from ESD strikes with wide display bezel design. However, the current trend in the industry has the display bezel getting narrower and narrower, even for low-end products. Now the seam around the narrower bezel intercepting housing is more likely aligned right over the top of ALS/Proximity part and creates a direct ESD strike entry path toward the part (See Figure 8). Coupling this with low-cost plastic housing frames used in low-end products, ALS/Proximity parts are very susceptible to ESD discharge. They can possibly lose their function or even get damaged, if no measure is taken for ESD protection in the system design.

Figure 8:
ESD Strike Entry Paths to an ams Proximity Part in a Smart Phone Design



Here we will use the TMD2702VC as an example to highlight system design rules for preventing ESD issues. Please see Figure 9 for a high-level abstract of the ESD protection scheme at the TMD2702VC component level.

Figure 9:
TMD2702VC ESD Protection Scheme Abstract

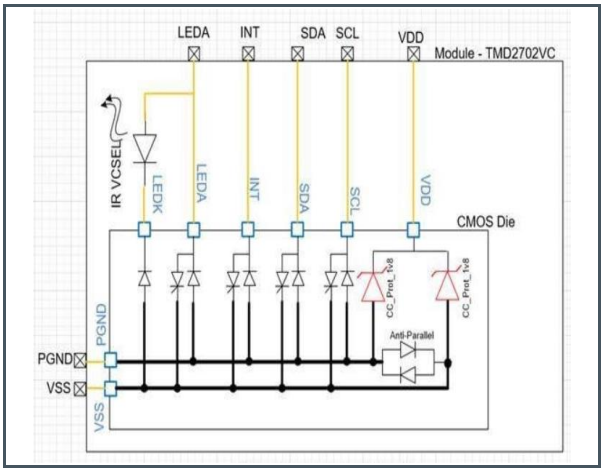
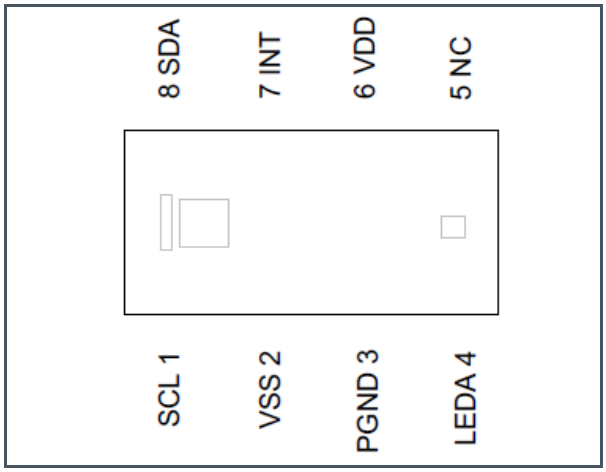


Figure 10:
TMD2702VC Pin Diagram (Top view)



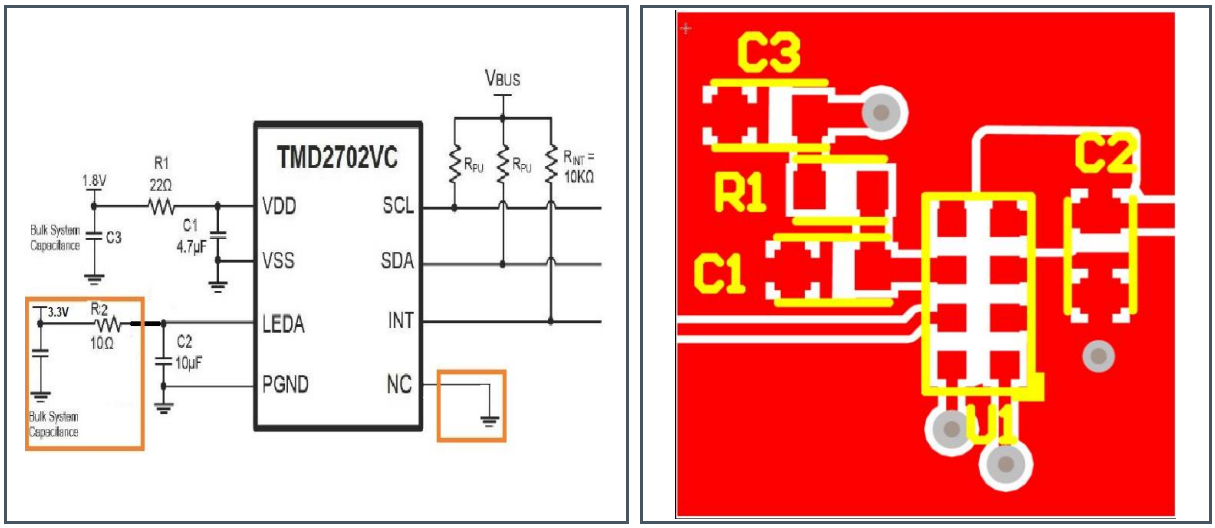
3.2.1 ESD Design General Guideline

A circuit layout example of TMD2702VC is shown in Figure 12 along with its circuit schematic example in Figure 11. As mentioned before, the same design rules preventing EMI described in Section 2 are also applied for preventing ESD issues. Good grounding, proper PCB/FPCB layout and sufficient bypass filters on VLEDA and VDD supplies will create a robust design.

However, if a system design is limited by its form factor (e.g. narrow display bezel), mechanical design (e.g. plastic housing frame), ESD issues can become a serious problem. For example, a lower end smart phone stackup shown in Figure 8 could easily have ESD problems. The measures listed below need to be taken for preventing ESD issues in a system ESD test lab and in the field.

Figure 11:
TMD2702VC Proximity Circuit Schematic Example

Figure 12:
TMD2702VC Proximity Circuit Layout Example



3.2.2 Special Care for Grounding and Board Layout and BOM

The best path for an ESD strike to dissipate is through a robust ground return from the sensor PCB/FPCB to system ground. This is usually main PCB (MPCB) ground and/or mechanical ground. The robust ground return also makes bypass filters on the sensor board much more effective with a reduced inductance return path. It should also be noted that the TMD2702VC NC pin should be grounded (see Figure 10), to prevent it from floating, as the voltage builds up on a floated unused pin due to consecutive ESD strikes can jump onto adjacent signal pins and traces causing ESD issues. This applies to TMD3702VC NC pin too.

In the sensor PCB/FPCB layout, one layer should be reserved for a ground plane. If a sensor board is connected to the MPCB through a B2B or ZIF connector, multiple connector pins should be assigned for ground. Mechanical grounding methods should also be considered for sensor boards, e.g., screws, spring ground contact, conductive tape for rigid PCB ground, and FPCB stiffener ground.

As shown in Figure 11, it is recommended that a bulk capacitor C1 in the bypass filter needs to be placed right next to pin VDD, while capacitor, C2, needs to be placed right next to pin LEDA. This may be not possible in some system designs due to board space limitations. However, one needs to place them as close as possible to their respective pins and route with widened traces. Due to the same space limitation, capacitors with recommended capacitance values may not fit in the layout design. System designers need to place highest capacitance value allowed for C1 and C2. Ideally, at least

2.2 µF with a robust ground design. ESD protection components like zener diode or TVS placeholders can also be reserved for LEDA and VDD pins.

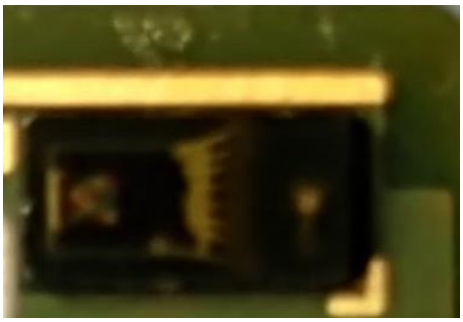
It is also strongly recommended to avoid routing signal/supply traces on the top layer which is likely to be exposed to ESD strikes. Placing discrete parts in this high risk ESD area, on the top layer, also needs to be avoided.

3.2.3 Eliminate or Control ESD Strike Entry Paths

As shown in Figure 7, it is problematic to have an ESD strike get through the seam and hit the sensor. Certain glue material can be applied to the seam at top to eliminate the entry path if possible.

If sealing the seam is not possible, one can try to guide the ESD strike point away from the sensor part to improve system ESD immunity. It has proved very effective to expose a ground copper layer around the sensor part, as shown in Figure 13. As a result ESD strikes are more likely to hit the exposed copper layer rather than the sensor part.

Figure 13:
Exposing Ground Copper Layer to Control ESD Strike Point



3.3 ESD Design Guideline Summary

- The same design rules preventing EMI issues can apply to preventing ESD issues.
- In challenging system designs such as smart phone for ESD protection, special care needs to be taken with grounding, PCB layout and BOM designs.
- One can eliminate ESD strike entry paths, or guide ESD strikes away from the sensor with some mechanical means.
- Software workarounds can only be a last resort to fix minor ESD issues. System designers should rely on solid hardware design practices for ESD issues first.
- Careful hardware design reviews and test validations for ESD early in the project design cycle can avoid lots of ESD fire drills later.

4 Revision Information

Changes from previous version to current revision v1-00	Page
Initial production version	
Information extended to also cover ToF parts	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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