AS1163

Datasheet

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AS1163 SAID - Standalone intelligent driver

1 General description

AS1163 is a mixed signal silicon device optimized for dynamic lighting applications.

The basic purpose of AS1163 is to drive 9 LEDs organized in 3 channel triplets (RGB) with an independent PWM dimming dynamic range up to 16 bits.

AS1163 is often addressed with a different name: “SAID”, an acronym, which stands for Stand-Alone Intelligent Driver.

Daisy chain configurations of multiple AS1163 devices will enable cost effective implementation of complex dynamic lighting effects.

AS1163 will support single layer slim PCB designs.

The communication protocol supported by AS1163 is Open System Protocol (OSP), which makes the SAID fully compatible with the ams OSRAM OSIRE E3731i. AS1163 will support additional features such as I²C gateway, parallel connection, power-rail feedback, analog readout.

Each AS1163 device in the chain will be usable by a MCU to read and write an external I²C device, e.g. EEPROM, temperature sensor, Ambient Light Sensor.

AS1163 is with Functional Safety QM and supports to achieve ASIL-B on system level.

1.1 Key benefits & features

The benefits and features of AS1163, SAID - Standalone intelligent driver are listed below:

Table 1: Added value of using AS1163

Benefits	Features
Cost effective system design	Single layer PCB
Slim layout	3x RGB channels per IC
Sensing integration	I²C gateway (compatible with 5V and tolerant for 3V3 and 1V8)
Open system protocol	• Auto-addressing 2.4 Mbit/s two-wire daisy chain protocol • Up to 1000 nodes • CRC protected communication
Adjustable output current	1.5, 3, 6, 12, 24, 48 mA (3×outputs: Max. 48mA; 6×outputs: max. 24mA)
Configurable output power	Output clustering options (up to 288 mA)
Brightness adjustment	16-bit equivalent dynamic range when LSB dithering function is activated. 15-bit PWM engine @ 500 Hz 14-bit PWM engine @ 1000 Hz
• Low EMI • Low power consumption • Reduced phantom effect	Enhanced driving mode (Dithering)
Star network implementation	External setting of parallel addressing (also called branching)
Sync pin	External HW sync for display application
Remote analog input for sensing	Integrated 10-bit ADC + MUX – range VDD – VDD-3.56 V
Functional Safety	QM (compliant with ASIL-B on system level)
Automotive	AEC-Q100 grade 1

1.2 Applications

- Interior dynamic lighting effect
- Ambient lighting
- Functional lighting
- Exterior lighting (e.g. grill application)
- Roof lighting
- Smart surface

1.3 Use case overview

In this section possible use cases of AS1163 are presented.

Figure 1: Use case 1

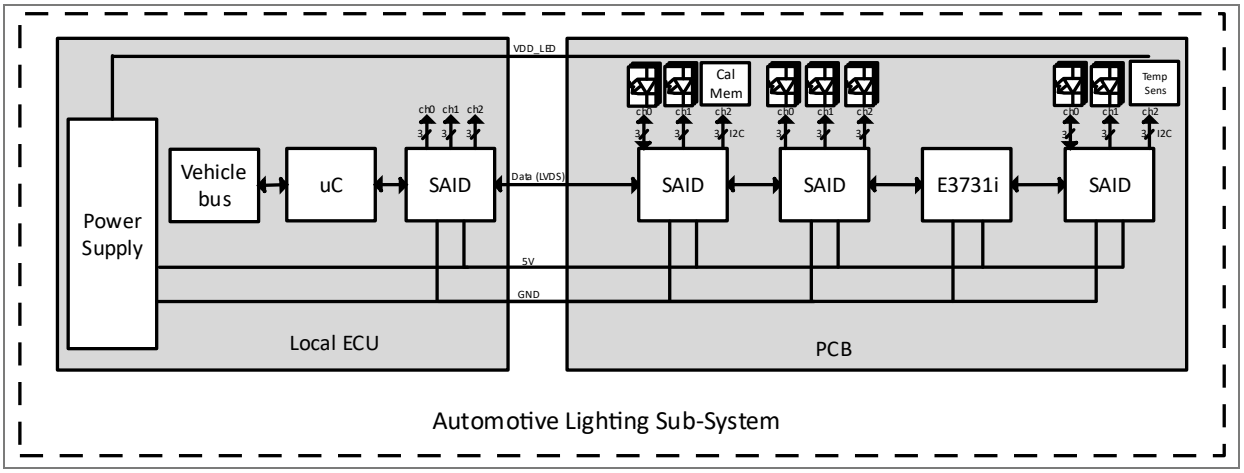


Figure 1 shows daisy chain using LVDS as local bus and supporting OSIRE E3731i and I²C device interfacing.

Figure 2: Use case 2

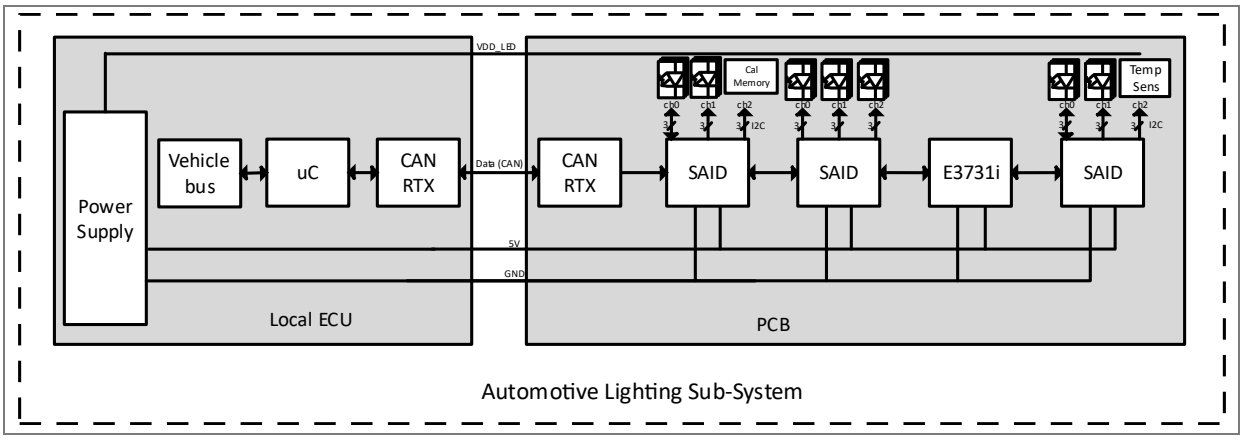


Figure 2 shows daisy chain using CAN bus and supporting OSIRE E3731i and I²C device interfacing.

MCU mode having Manchester downstream and data & clock upstream will produce communication error flags at parallel devices that are not addressed, while MCU - SPI mode supports parallel communication, given its symmetry in downstream and upstream flows (See Chapter 6.5).

Figure 3: Use case 3

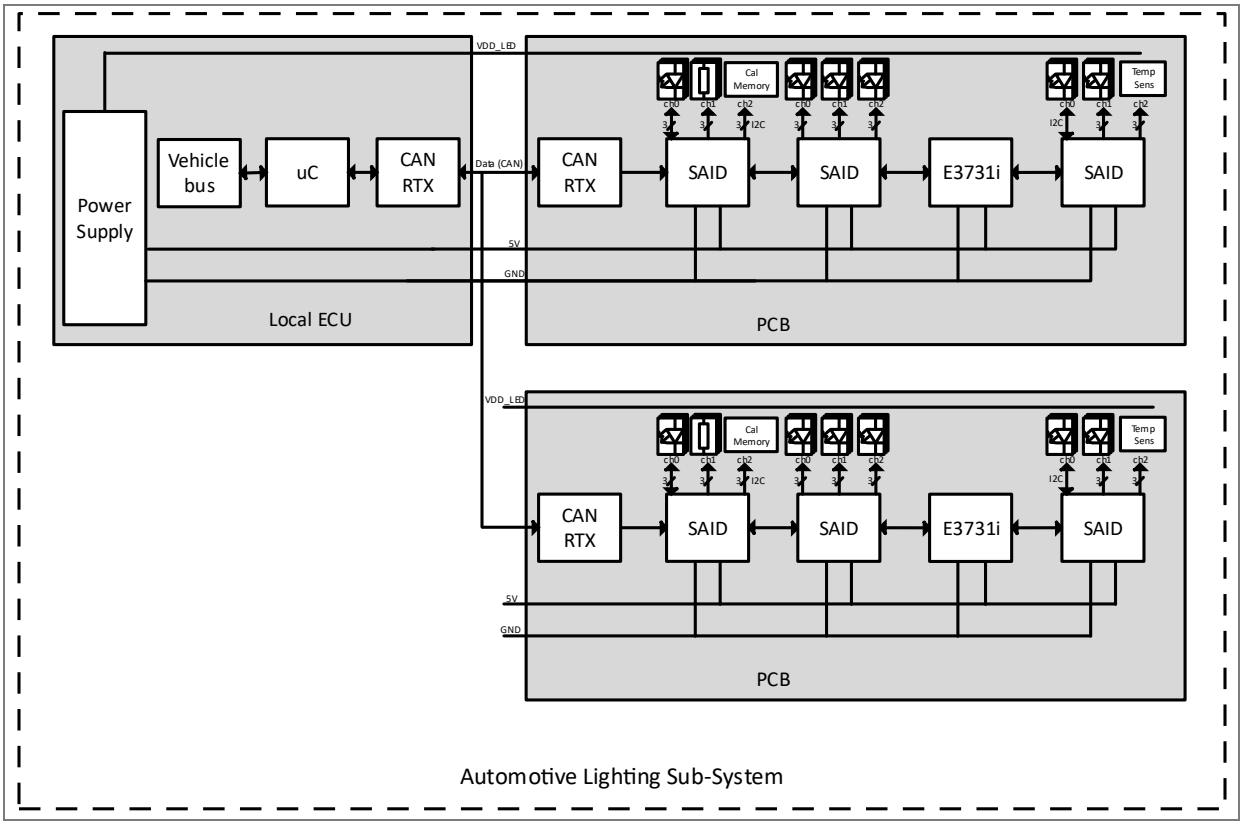


Figure 3 shows parallel connection of Daisy Chains using local CAN bus, supporting OSIRE RGBi and I²C device interfacing.

Parallel addressing (Figure 4) is fully supported with symmetrical communication modes, such as SPI-mode, LVDS mode, CAN mode (also called USE mode).

Figure 4: Use case 4

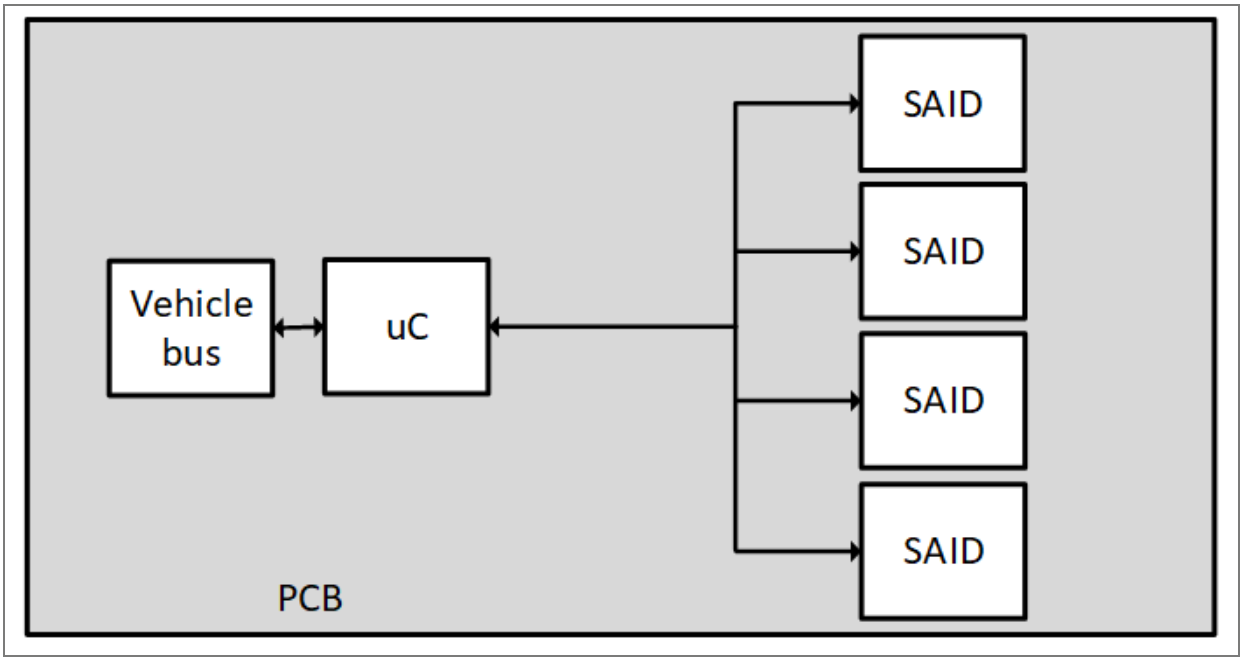
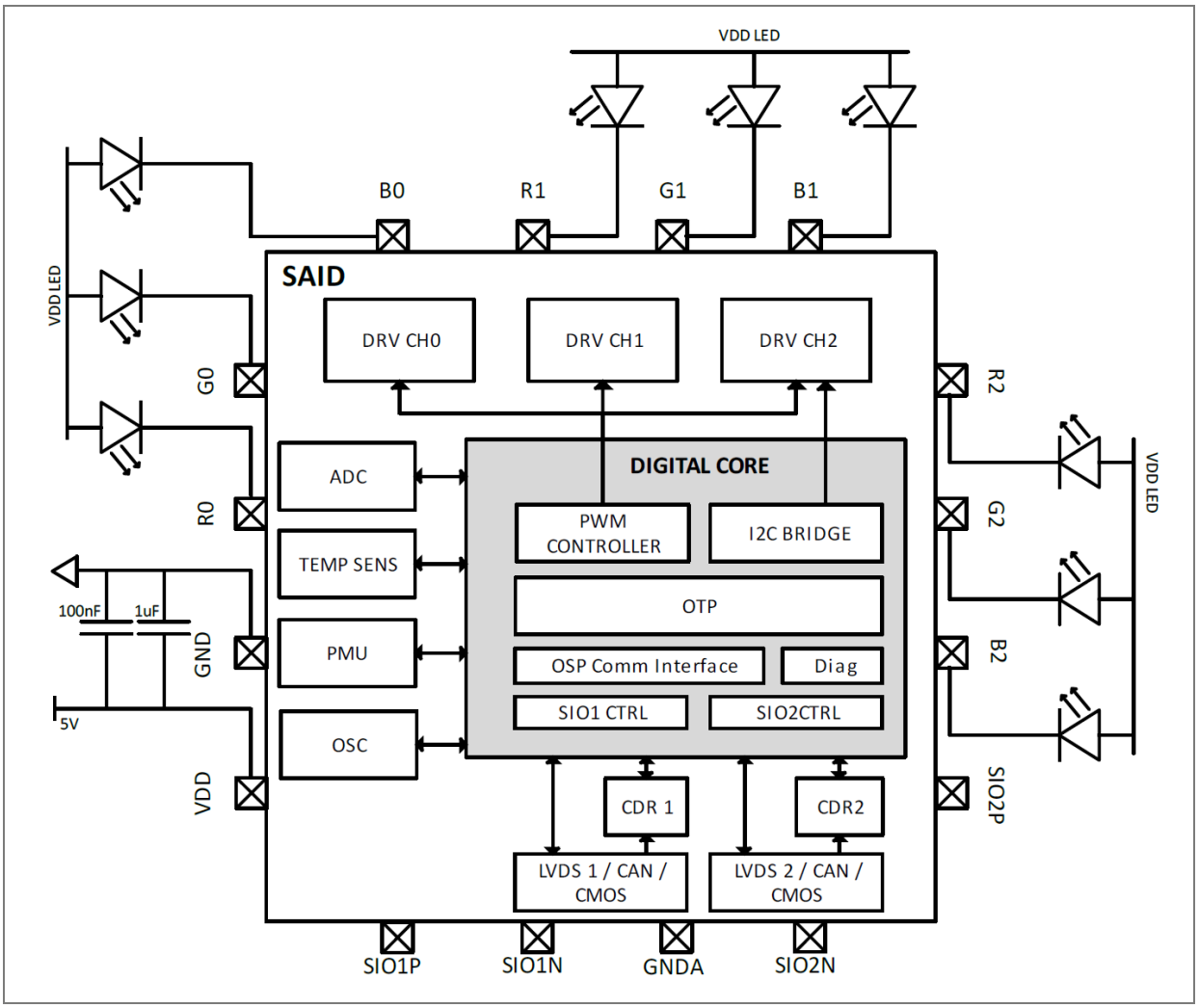


Figure 4 shows parallel connection of SAID devices with direct MCU connection.

1.4 Block diagram

The functional blocks of this device are shown below:

Figure 5: Functional blocks of AS1163



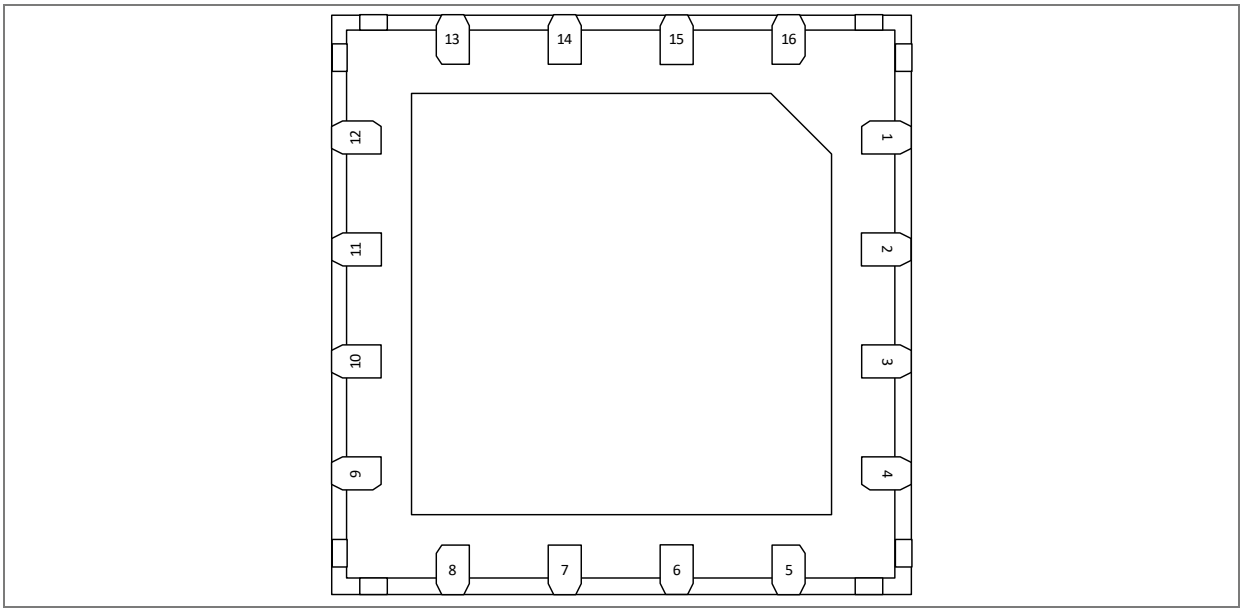
2 Ordering information

Ordering code	Package	Product type/Marking	Delivery form	Delivery quantity
Q65113A6575	QFN16	AS1163	Tape & reel	5k pcs/reel
Q65113A9863	QFN16	AS1163	Tape & reel	1k pcs/reel

3 Pin assignment

3.1 Pin diagram

Figure 6: Block diagram and pinout (package bottom view)



(1) The heat pad on bottom side is connected to the device substrate. It is recommended to connect the heat pad to GND or leave it floating, do not connect to any other signal.

3.2 Pin description

Table 2: Pin description of AS1163

Pin number	Pin name	Pin type(1)	Description(2)
QFN 3x3 16			
1	G0	ANA	Driver 1 of channel 0 (Green)
2	R0	ANA	Driver 0 of channel 0 (Red)
3	GNDP	PWR	Power ground
4	VDD	PWR	5 V power supply
5	SIO1P	ANA/DIO	Positive digital IO for SIO1 interface
6	SIO1N	ANA/DIO	Negative digital IO for SIO1 interface
7	GNDA	PWR	Analog ground
8	SIO2N	ANA/DIO	Negative digital IO for SIO2 interface, test-bus
9	SIO2P	ANA/DIO	Positive digital IO for SIO2 interface, test-bus
10	B2	ANA	Driver 2 of channel 2 (Blue), also INT
11	G2	ANA	Driver 1 of channel 2 (Green), also SCL
12	R2	ANA	Driver 0 of channel 2 (Red), also SDA
13	B1	ANA	Driver 2 of channel 1 (Blue), also SYNC
14	G1	ANA	Driver 1 of channel 1 (Green), also for parallel address configuration
15	R1	ANA	Driver 0 of channel 1 (Red), also for parallel address configuration
16	B0	ANA	Driver 2 of channel 0 (Blue)

(1) Explanation of abbreviations:
DIO Digital input and output
ANA Analog pin
PWR Power pin
(2) Pin name: R, G and B are only for naming purposes, not necessarily to be bound to red, green or blue color.

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS1163

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V_{DD} / V_{GND}	Supply voltage to ground	-0.3	7	V	Referenced to GND
V_{IN}	Input pin voltage to ground	-0.3	V_{DD}+0.3	V	
I_{SCR}	Input current (latch-up immunity)	± 100		mA	AEC-Q100-004
Continuous power dissipation (T_A = 70 °C)					
P_T	Continuous power dissipation		600	mW	
Continuous power dissipation (T_A = 125 °C, V_{OUT} = 2.5 V, R_{TH} = 71.6 °C/W)					
P_T	Continuous power dissipation		300	mW	
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM	± 4		KV	AEC-Q100-002
ESD_{CDM}	Electrostatic discharge CDM	± 500		V	AEC-Q100-011, ±750V for corner pins
Temperature ranges and storage conditions					
T_A	Operating ambient temperature	-40	125	°C	
T_J	Operating junction temperature	-40	150	°C	
T_{STRG}	Storage temperature range	-55	150	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			ICP/JEDEC J-STD-033

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Voltages are referred to the GNDA pin unless differently specified.

Table 4: Electrical characteristics of AS1163

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Startup time					1	ms
VDD_com_stop	VDD communication stop (stop of communication when VDD drops below)			3		V
VDD	Positive supply voltage		4.3		5.5	V
IDD	Supply current	All drivers at full current		50		mA
IDD_sleep	Sleep current			1.6		mA
IDD_Dsleep	Deep sleep current			1.5		mA
VLED_Head	Min headroom LED driver	1% current compression relative to 2.5V		600		mV
LED_Short	LED short detection threshold		VDD-1.8	VDD-1.2	VDD-0.5	V
LED_Open	LED open detection threshold		50	250	550	mV
LED_Pers	Minimum PWM duration and fault duration for LED_open / LED_Short functionality			27		µs
ILED_abs_acc	LED current absolute accuracy	Max ILED absolute driver accuracy. Over the whole temperature range and max current setting. Tested with VDD=5V	-8.5		8.5	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ILED_C2C_Mis	LED channel to channel matching(1)	Max ILED Channel to Channel over the whole temperature range and max current setting. Tested with VDD=5V	-5		5	%
ILED_Mis	LED channel current matching(2)	Max ILED Driver to Driver (same channel). Over the whole temperature range and max current setting. Tested with VDD=5V	-2.5		2.5	%
ILED_rise/fall	LED rising / falling edge	From 10 to 90%		50		ns
LED Off	LED Off current			3		µA
PWM_freq	PWM freq. fast			1.172		kHz
PWM_freq	PWM freq. slow			0.586		kHz
PWM_res	PWM freq. fast			14		bit
PWM_res	PWM freq. slow			15		bit
PWM_freq_acc	PWM freq. accuracy		-5		5	%
PWM_INL				0.2		LSB
VDD_UV	Under voltage threshold			4.15		V
VDD_UV_HYST	Under voltage hysteresis			100		mV
VTH_Dig	Valid digital input(3)		0.5	0.75	1.2	V
ADC_VREF1				0.365		V
ADC_VREF2				0.972		V
ADC_VREF	Buffered ADC reference			1.340		V
ADC_OS	ADC offset(4)	Vf meas.	-2		2	LSB
ADC_RANGE	Typical input range, Vf mode	Vf meas.	VDD - 8/3 ADC_VREF		VDD	V
ADC_GAIN		Vf meas.		3.494		mV/LSB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC_GAIN_ERR	Gain variation	Vf meas, referred to full-scale. Tested with VDD=5V	-1.12		1.12	%
ADC_DNL	DNL	Vf meas. Valid for Tj<125ºC	-1		1	LSB
ADC_INL	INL	Vf meas.	-3		3	LSB
ADC_TSAMPLE		Vf meas.		1.6		µs
T_acc	Temperature sensor accuracy	Room temp.	-8		8	ºC
T_AMB	Ambient temperature		-40		125	ºC
T_J	Junction temperature		-40		150	ºC
Rth	Thermal resistance from junction to ambient temperature	JEDEC 2s2p PCB		64		°C/W
V_th_se_high	Threshold on SIOx_x to detect communication mode (high)		2.85		VDD+0.3	V
V_th_se_low	Threshold on SIOx_x to detect communication mode (low)		-0.3		0.7	V
V_SIOx_P/N(O,L)	Output low level for pin SIOx_P and SIOx_N for single-ended communication	10k Ohm load	0		0.7	V
V_SIOx_P/N(O,H)	Output high level for pin SIOx_P and SIOx_N for single-ended communication	10k Ohm load	VDD-0.7		VDD	V
F_com_mcu	Allowed input data rate for communication in MCU mode. Tested with VDD=5V.		2.23	2.4	2.62	Mbps
DUTY_com_mcu	Allowed input duty cycle in MCU mode. Tested with VDD=5V.		47.5		52.5	%
F_com_can	Allowed input data rate for communication in CAN RTX mode. Tested with VDD=5V.		2.31	2.4	2.55	Mbps

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DUTY_com_can	Allowed input duty cycle in CAN RTX mode. Tested with VDD=5V.		40		55	%
	Time between consecutive telegrams from MCU	Dependent on length of daisy chain	8.3			µs
VIH_SE	High level input voltage single ended communication		2.4		VDD+0.3	V
VIL_SE	Low level input voltage single ended communication		-0.3		0.7	V
LVDS_VCM	LVDS common mode voltage with active communication			1.2		V
LVDS_VDIFF	LVDS differential voltage			300		mV
LVDS_VCM_IDLE	LVDS common mode voltage with no active communication			0		V
LVDS_RTERM	LVDS termination resistance	Included in the IC		200		Ohm
LVDS_ITX	LVDS current			1.5		mA

(1) Channel to channel relative accuracy is calculated with the following formulas:
ILED_C2C_Mis(ch0_x) = ((0.5*I(ch0_x) – average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)) / average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)))*100
ILED_C2C_Mis(ch1_x) = ((I(ch1_x) – average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)) / average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)))*100,
ILED_C2C_Mis(ch2_x) = ((I(ch2_x) – average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)) / average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)))*100,

Where:
a) ILED_C2C_Mis(ch0_x) refers to a general driver x inside channel 0, for example: ch0_R refers to the R driver in channel 0. Similarly, for ILED_C2C_Mis(ch1_x), ILED_C2C_Mis(ch2_x).
b) I(ch0_x) refers to the high current level of a particular driver in channel 0. Similarly, for I(ch1_x) and I(ch2_x)
c) I(ch0_RGB) refers to the sum of the high current levels for the drivers belonging to channel 0. Similarly, for I(ch1_RGB) and I(ch2_RGB).

(2) In-channel relative accuracy is calculated with the following formula:
ILED_Mis(chx_y) = ((I(chx_y) – average(I(chx_RGB))) / average(I(chx_RGB)))*100

Where:
a) ILED_Mis(chx_y) refers to a general driver y inside a general channel x, for example: ch0_R refers to the R driver in channel 0.
b) I(chx_y) refers to the high current level of a general driver y in a general channel x.
c) I(chx_RGB) refers to the sum of the high current levels of all drivers belonging to a general channel x.

(3) LED drivers can be used as receiving path for I²C bridge, Sync pin, parallel address setting by external HW.
(4) Relative accuracy. For absolute accuracy, calibration in applications is necessary.

5.1 Power supply

For operating SAID a voltage supply VDD of typical 5 V is required. Each SAID can sink up to nominal 288 mA from the LEDs and the power delivery network needs to be sized accordingly.

Decoupling caps are recommended between VDD and GND, placed as close as possible to the device power pins.

Recommended values for these caps are:

- 1 µF elco capacity
- 100 nF high ESR capacitor
- VDD voltage up to 6 V

5.2 Startup sequence

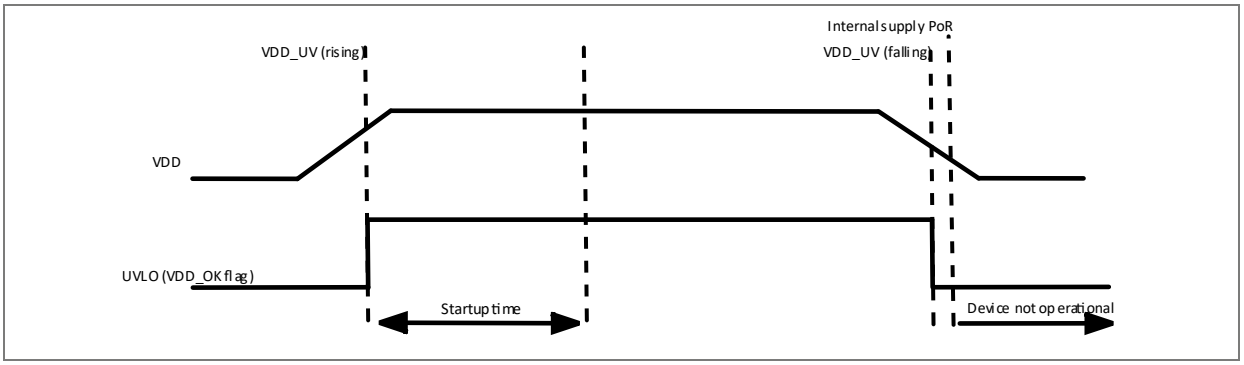
The device starts-up with VDD overcoming the UVLO (undervoltage lockout) threshold. After the bandgap reference starts-up, the voltage regulator generates an internal voltage, VREG.

The internal blocks supplied by VREG (nominally 1.5 V) are reset until the supply reaches the POR_N threshold. The RC oscillator is also enabled with POR_N. In this state, for a trimmed device, the OTP is downloaded, and the trimming/configuration bits activated (~200 µs).

All internal blocks supplied by the external VDD supply start up after the supply reaches the UVLO threshold. At this point the communication interface and the led drivers are functional. Once the communication is enabled, also in case of an under-voltage event, the device does not lose functionality until an internal falling POR_N event. The VDD_OK flag signals that the VDD is above the VDD_UV threshold.

Note: VREG, POR_N are internal signals. At startup the current is increased up to 6mA to ensure stable readout from the OTP for proper operation.

Figure 7: Startup sequence



6 Functional description

6.1 Compatibility of features

The following table shows the programming compatibility of features. For example: Dithering is available in 1 kHz mode.

Table 5: Programming compatibility of features

	Current setting	PWM freq.	Haptic	Channel clustering	I²C bridge	HW star address	Dithering	Sync pin
Current setting	+							
PWM freq.	+	+						
Haptic	+	+	+					
Channel clustering	+	+	-	+				
I²C bridge	+	+	-	CH2 drivers not available for clustering when I²C enabled.	+			
HW star address	+	+	-	If HW address used CH1 R,G drivers not available: Limited clustering configurations	+	+		
Dithering	+	500 Hz only	-	+	+	+	+	
Sync pin	+	+	-	CH1 B not available: Limited clustering configuration	+	+	+	+

6.2 One time programmable memory (OTP)

The OTP contains trimming data burned at manufacturing as well as configuration bits.

Bytes from 13 to 31 (0x0D to 0x1F) are dedicated to customer settings and customer data. They contain bits for enabling the I²C bridge, various star configuration aspects, enabling sync via pin, SPI mode communication in MCU mode, haptic driver enabling and channel clustering. Remaining bytes can be used to store customer LED calibration data or other data to be read from the MCU.

At startup the OTP is copied to a RAM, so registers can be overridden at run-time and this operation is non-persistent unless a burn follows. Since some configuration bits (eg. SPI_mode) are read at boot, overriding them in RAM is not effective at run-time, unless a reset telegram is issued.

Table 6: OTP customer area

OTP address	Bits								
	7	6	5	4	3	2	1	0	
0D	CH_clustering[2:0]			haptic_driver	SPI_mode	sync_pin_en	star_net_en	i2c_bridge_en	customer area
0E					otp_add_en	star_net_otp_addr[2:0]			
0F									
10									
11									
12									
13									
14									
15									
16									
17									
18									
19									
1A									
1B									
1C									
1D									
1E	Cust_lock								
1F	CRC2<7:0> (could also be used for other data)								

6.2.1 OTP burn procedure

OTP required voltage@25°C: 2.7V ± 100mV, additionally a 10µF bypass capacitor is required on VDD.

To program the OTP customer section (from address 0x0D to 0x1F), the following steps must be followed, once the device is accessible via a dedicated command:

1. Reset/init
2. Settestpw
3. Setotp
4. Cust
5. Burn
6. Lower voltage (within 15µs)
7. Wait 5ms
8. Raise voltage
9. Idle
10. settestpw(0)

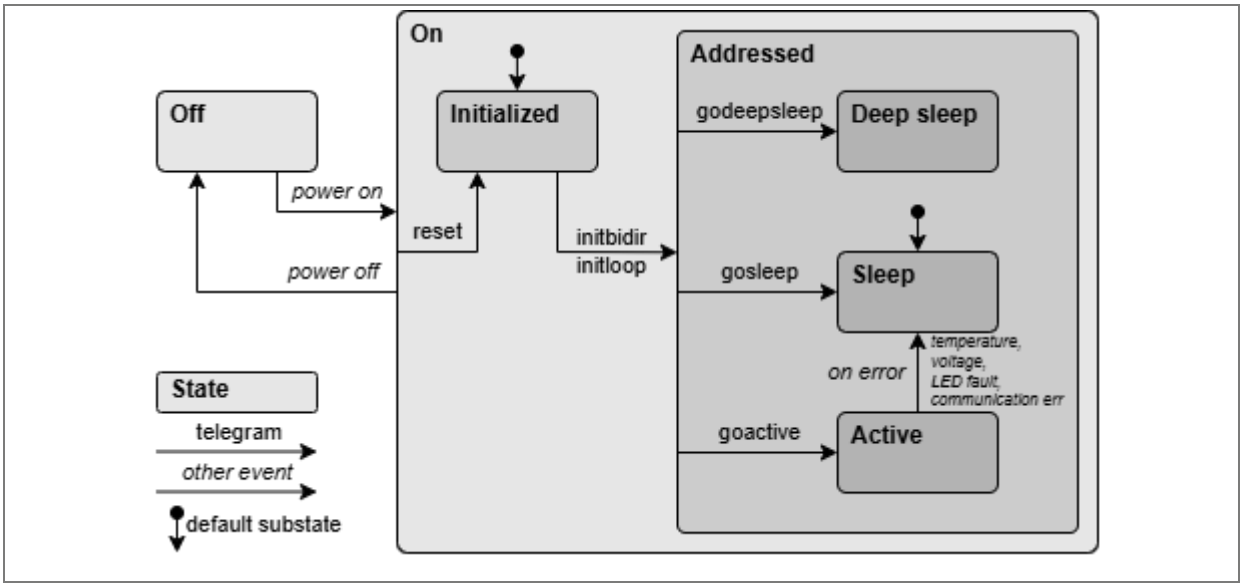
Based on qualification data of the pfuse OTP element, a burning yield loss of typically around 3ppm/bit has to be considered while using the specified optimum burn conditions. Furthermore any burning yield loss higher than 50ppm/bit is an indicator that for some reasons the burning conditions are not in the optimum qualified range. To verify the correctness of burned values:

1. Write different data to OTP (e.g. all OTP bytes at 0x1A1A)
2. Send CUST command
3. Send GLOAD command (optional, only for GLOAD check)
4. Send LOAD command
5. Send IDLE command
6. Read back all OTP and verify the burned values
7. Once the bit 1F.7 (Cust_lock) is 1, the OTP can no longer be changed

6.3 Device state overview

Once the VDD supply is above the UVLO threshold and after an internal pre-defined startup time the device is ready for communication. The device does not lose functionality until VDD drops below the typical value of 2.6V. Internal startup time is below 1 ms.

Figure 8: Device state machine



6.3.1 UNINITIALIZED state

The device will reach the UNINITIALIZED state after power up, a power cycle from any other state or via RESET command. In this state the register content is lost and reset to defaults. PWM values are 0, LED drivers are disabled. Address is 0. From application point of view, the nodes in the daisy chain must be assigned an address and each node is waiting for the first correct telegram. Nodes are accepting only a limited number of telegrams in this state:

- INITBIDIR or INITLOOP (bi-directional or loop back mode respectively)
- RESET
- CLRERROR
- P4ERRBIDIR or P4ERRLOOP (bi-directional or loop back mode respectively)
- Register broadcast writes

Any other or incorrect telegrams are ignored.

6.3.2 ADDRESSED state

With a correct INITBIDIR / INITLOOP telegram the SAID IC reaches the INITIALIZED state. A SAID, receiving the address, latches the received address, changes the address field to the next possible value and sends it via output SIO port. After this operation, it waits for a new telegram. Any further INITBIDIR / INITLOOP telegrams will not change the state of the device. In this way the received address is incremented by +1 and sent to next device in the chain. If the IC has detected it is the last node in a chain, it sends a response telegram back to the MCU.

6.3.3 ACTIVE state

The transition to this state is via GOACTIVE command only. LED drivers are activated if the PWM parameter is greater than 0 and no diagnosis flag bit occurred, according to the wanted error trapping behavior specified via SETUP register. Received PWM parameters for drivers are latched till the next SETPWMCHN / SETPWM command is received. Since SAID has the OV_FLAG set after RESET, it will not switch to ACTIVE state unless the error trapping behavior is changed beforehand in the SETUP register. It is recommended to send a READSTATUS or READTEMPSTAT / CLEAREVENT before GOACTIVE is transmitted.

6.3.4 SLEEP state

The device enters SLEEP mode after following conditions:

- After initial INITBIDIR / INITLOOP(default state)
- An error bit gets flagged whose trapping is enabled in the SETUP register (if previous state is the active state)
- Receiving a GOSLEEP telegram.

The LED drivers are disabled. The last PWM parameters remains latched. A PWM parameter update is possible SETPWMCHN telegram.

The faults/diagnostic flags that lead to SLEEP mode are specified in the SETUP register.

During SLEEP mode reading diagnostic flags and temperature is possible.

6.3.5 DEEPSLEEP state

The device enters in power save sleep mode after GODEEPSLEEP and waits for activating via GOSLEEP, GOACTIVE or RESET.

Only communication is supported. Diagnostic not possible. Temperature measurement not possible.

Transition to ACTIVE mode is supported via GOACTIVE command, provided fault flags are clear.

6.4 ADC

The ADC is meant for measuring the difference between VDD and the LED driver outputs, also referred to as Vf of the LED.

User can utilize the ADC readings for:

- Power rail optimization
- LED aging estimation
- General purpose measurement request (selected LED driver can be turned OFF by setting PWM to 0). As the Vf, this measurement is referred to VDD.

The main features are:

- Sampling window < 2µs
- Fresh measurement at each driver < 18 ms
- Resolution: 10-bit
- Typical Input range from VDD to VDD – 3.574 V (Vforward measurement)
- Analog multiplexer for measuring the LED Vforward at all driver outputs.
- Synchronous measurement triggered with PWM rising-edge, to capture the Vds while the driver is turned on.
- Asynchronous measurement possible with dedicated bit set in measurement request command.

Equation 1:

$$Vf = VDD - VDRV = ADC\_GAIN\_VF * (VF\_ADC\_DATA - 2)$$

Where,

Vf is the forward voltage in V,

VDD is the applied external supply at VDD pin of AS1163 in V,

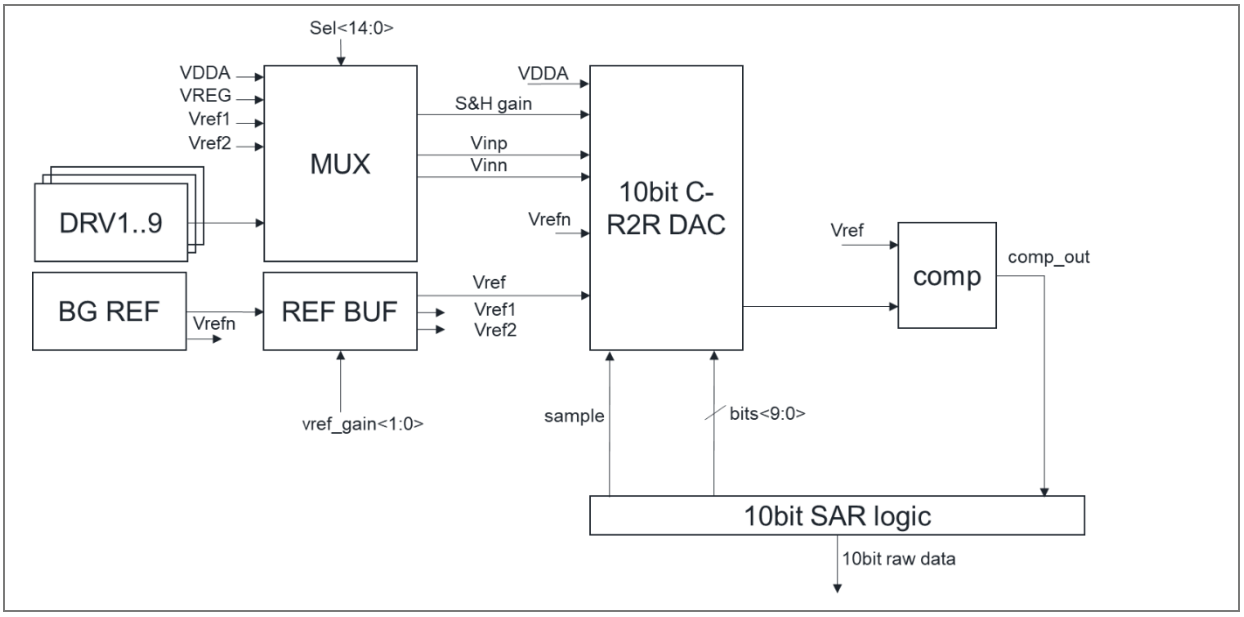
ADC_GAIN_VF is a parameter,

VDRV is the selected driver output voltage,

VF_ADC_DATA is the ADC reading in Vf mode,

-2 is a systematic offset.

Figure 9: ADC block diagram



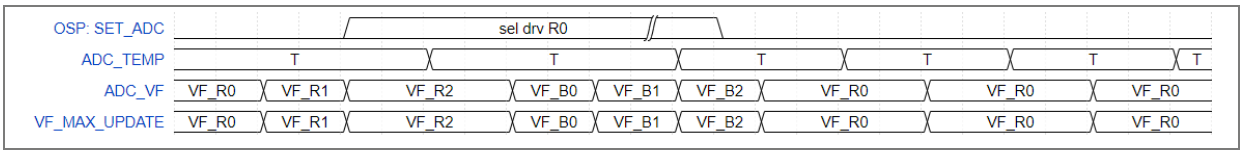
Considering the 500 Hz mode as an example, PWM period is effectively <1.8ms (5% clk tolerance included). After SETADC command, wait time is suggested to be two PWM cycles.

In this particular mode, the device alternates a temperature measurement with a Vforward measurement of the selected driver. Once the ADC data is read, using the READADCDAT command, the device returns to the default measurement routine.

In case no ADC measurement is requested, the internal measurement routine is observed according to the PWM activation sequence, which results in a fresh reading nominally every 18ms. This is only relevant for the ASKVINFO functionality.

The picture below shows, not in scale, the behavior of the ADC when a measurement on a specific driver is requested.

Figure 10: Typical behavior of the ADC



6.4.1 Measurement routine

The ADC, when enabled, is periodically executing a measurement routine:

- Temperature sensor measurement
  R0, R1, R2 Vf voltage
- Temperature sensor measurement
  B0, B1, B2 Vf voltage
- Temperature sensor measurement
  G0, G1, G2 Vf voltage

The temperature sensor reading is stored in the temperature register, while the forward voltage readings (from R0 to G2 if applicable) are constantly updating the VFMAX register (only for drivers that are not used for addressing, SYNC. pin or I²C bridge). VFMAX register stores the largest forward voltage observed in the node.

Upon receiving the command SETADC, which specifies the particular driver of the total 9 drivers to be measured, the ADC DATA register is filled with the next measurement of the specified driver output.

The 9 drivers are addressable with the command payload with numbering from 1 to 9 in the following order: R0, R1, R2, B0, B1, B2, G0, G1, G2.

From now on, the device alternates a forward voltage measurement with a temperature measurement, until the command READADCDAT is received. This command returns the last forward voltage measurement and causes the device to resume the measurement routine across all active drivers

After a SETADC command a READADCDAT must follow. Changing PWM value or issuing a new SETADC command requesting a measurement on a different driver is not permitted until the previous result has been read.

6.4.1.1 DRVx Vf measurement routine

DRVx Vf measurements are triggered by the respective PWM signal and are valid only for PWM duty cycles above the minimum conversion time or sampling time.

This sequence allows a temperature measurement nominally every 5.7 ms when PWM at 500Hz is selected with all PWM drivers on.

The adjusted temperature sensor reading is stored in the temperature register (8 bits right aligned out of the 10 bits of the ADC), while the DRVx OUT voltage readings are constantly updating the VFMAX register (only for drivers that are not used for addressing, synch pin or I²C bridge) and is stored in the READADCDAT register.

If the ADC_VLED_MUX_CTRL field in the SETADCSET register specifies a particular driver to be measured, the ADC will cycle between the specified voltage to be measured and the temperature, and the READADCDAT register is filled with the selected measurement.

DRVx measurements are triggered only if the respective driver is active, because all DRVx voltage measurements are synchronized with the PWM start signal. If a particular driver is not active or PWM setting is 0x00, the measurement is skipped, unless the bit ADC_VLED_DISABLE_SYNC is selected in the SETADCSET register (this is also valid when a measurement is triggered with the ADC_VLED_MUX_CTRL). In this case, the driver output remains high-Z. To be noted: Driver output measurements are always referred to VDD. Moreover, to ensure a correct measurement, the PWM output must be still active during the ADC sampling time , otherwise the voltage measurement is not saved.

This poses a limitation to the minimum PWM setting in combination with Vforward measurements.

6.4.1.2 Temperature sensor

The temperature sensor relies on the 8 least significant bits of the 10-bit reading from the ADC, that measures an internally generated PTAT voltage.

The temperature value is obtained as follows, where TEMPVALUE is obtained via READTEMP (or READTEMPSTAT):

T(C) = (TEMPVALUE – 116) / 0.85 + 25

The overtemperature flag is set when the actual measurement is larger than OT_HIGH_VALUE.

Before the flag is set, an error counter is incremented and compared with a threshold. The OT_CYCLE register defines this threshold.

A similar down-counting is performed before setting the overtemperature flag to zero, when the temperature measurement is lower than OT_LOW_VALUE.

Table 7: Overtemperature cycle counter mechanism

OT_CYCLE<1:0>	Low pass filter cycle length (number of consecutive measurements)
2'b00	1 cycle
2'b01	2 cycles
2'b10	3 cycles
2'b11	4 cycles

6.5 Serial I/O interface (SIO)

SAID is compatible with the OSP protocol. This section provides an introduction, while an in-depth description of the protocol is left to the supporting OSP documentation.

New features from the OSP protocol are supported by SAID, such as:

- Multi-cast commands
- SW, HW sync
- Power-rail-info-feedback serial broadcast message
- Parallel addressing with dedicated OTP fuse and external programming
- I²C bridge

A SAID device features two SIO interfaces (= Serial IO) which are used for communication between devices and between a device and an MCU. Each SIO interface consists of a P terminal and an N terminal. The function of each terminal depends on the configured SIO mode.

From the functional mode point of view, a SAID is symmetrical in its two SIO interfaces.

Each of the two SIO interfaces supports several different communication modes.

Each SIO operates in half-duplex mode meaning it either receives or transmits a telegram. On the other hand, it is possible to contemporarily receive a telegram at one SIO and transmitting at the other SIO interface.

The expected data rate is 2.4 Mbit/s ± some allowed variance (for exact values see Table 4).

The four communication modes are:

1. “LVDS mode”: The SIO uses LVDS signaling on P and N lines for transmitting and receiving telegrams. Manchester encoding is used to transfer DATA & CLK. Up to 15pF capacitive load is supported.
2. “MCU mode, normal”:

   Type A MCU mode: The SIO uses a single-ended mode for signaling. Incoming commands are Manchester encoded and are expected on the SIOx_P port. Outgoing responses are transmitted also on SIOx_P in NRZ format together with the corresponding clock on SIOx_N.

   Type B MCU mode: Implemented as a flavor of the MCU mode, is selectable by OTP setting. Also called 2-wire SPI mode, it enables incoming communication to SAID using a DATA line and CLK line on SIO1 port, respectively on P and N lines. Outgoing communication is the same as for Type A MCU mode. Outgoing communication is the same as for Type A MCU mode.

   Default is MCU mode type A, but with SPI_mode bit set in OTP, the MCU mode type B is selected.
3. “MCU mode, EOL (End Of Line)”: This is similar to “MCU mode, normal” but the SIO port does consider itself to be at the end of the daisy chain instead of the beginning. This is needed for some commands that require the daisy chain topology information, like for example INIT telegrams.
4. “CAN mode” (officially known as USE mode): Communication via CAN transceiver. SIOx_P is always in output state and transmits telegram as Manchester encoded signals (single-ended), SIOx_N is always in input state and receives telegrams as Manchester encoded signal (single-ended). When connecting two nodes using USE mode, the P and N wire need to be crossed.

The SIO mode is defined by pull-up/pull-down resistors connected to the SIO pins. A device will monitor each SIO pin at startup to detect the programmed SIO mode for SIO1 and SIO2.

The recommended value for the pull-up and pull-down resistors is 10 kOhm. SAID SIO ports are equipped with an internal typical pull-down resistance of 100kOhm, so each of the listed pull-down cases may leave out the external pull-down. An external pull-down is recommended.

Table 8: SIO communication modes vs. pull-up/down resistors

		SIOx_P		SIOx_N		
R @ SIOx_P	R @ SIOx_N	Input	Output	Input	Output	Comment
Pdown	Pdown	LVDS (Manchester)	LVDS (Manchester)	LVDS (Manchester)	LVDS (Manchester)	LVDS mode
Pdown	Pup	-	Data (NRZ)	-	Clock (NRZ)	MCU mode EOL
Pup	Pdown	Clk & Data (Manchester)	Data (NRZ)	-	Clock (NRZ)	MCU mode, normal (Type A)
Pup	Pdown	Data (NRZ) Only SIO1 port	-	Clock(NRZ) Only SIO1 port	-	MCU normal mode (Type B), 2 wire SPI (selectable with OTP)
Pup	Pup	-	Clk & Data (Manchester)	Clk & Data (Manchester)	-	CAN mode

Additionally, the normal MCU communication mode is improved to require less computational power on the MCU side:

- SIO1_N is by default high (always output driving the pad high instead of communicating input/output like SIO1_P). This will help to correctly sample the data on the posedge of SIO1_N clock avoiding spurious posedge transitions at the start of the device answer.
- Device will wait 5 µs before to start an answer. This will leave more time to the MCU to reconfigure the interface direction.

The typical data rate is 2.4 Mbps.

The minimum break time between two consecutive telegrams sent by the MCU is 2 bits.

The protocol does not tolerate interruptions during the telegram, above the specified duty cycle distortion limits.

In case of 2-wire SPI mode (MCU mode Type B), an interruption up to 1 baud is tolerated.

Additional checks on received commands are available:

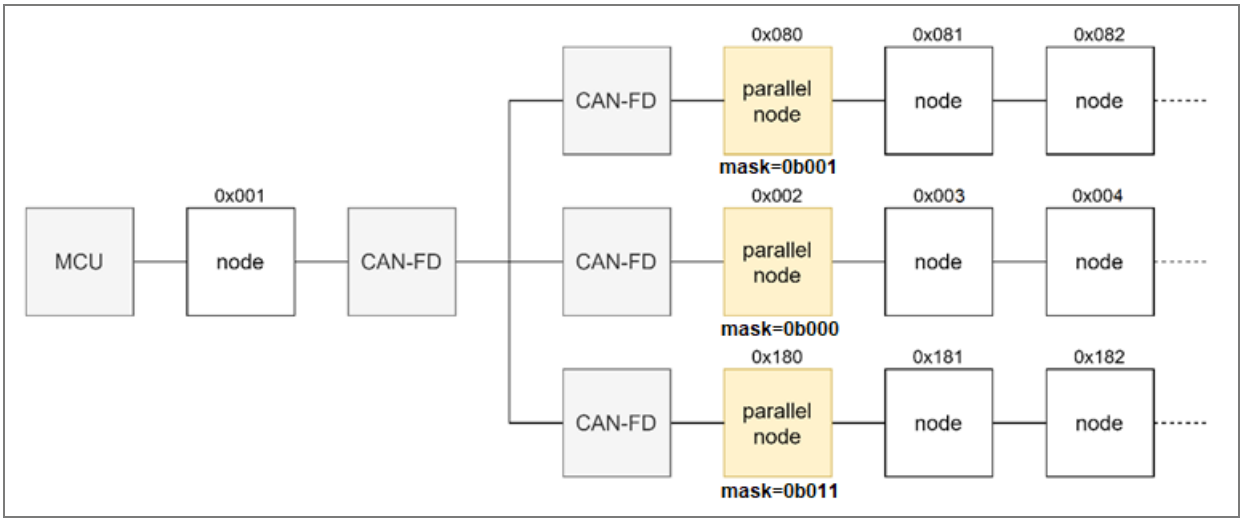
- If a node receives an unknown command with telegram ID > 0x0F, a communication error flag (STAT.CE_FLAG) will be raised.
- If a node receives an unknown command with telegram ID <= 0x0F (OSP specific command), no error will be raised.

6.5.1 Parallel addressing

While the OSP is natively supporting daisy chains, this device AS1163 expands support to more complex network topologies. This is achieved using specific nodes (“parallel” node) as branch starter and standard CAN-FD transceivers for the physical 1-to-N connection (see Figure 11).

All parallel branches must be individually addressed by sending the initialization command containing the address of the respective "parallel" node. After all branches are correctly initialized, devices can be seamlessly addressed as in a simple daisy chain.

Figure 11: OSP network topologies



(1) Only bidirectional mode is possible with star network topology. Loopback mode is not supported.

The use of the first node is optional but simplifies the MCU interface (ME coding/decoding).

Apart from the items listed below, a “parallel” node is just a regular OSP node.

Parallel nodes shall fulfill the following requirements:

A node becomes a “parallel” node by flashing bit star_net_en in OTP to 1.

Each parallel node has a fixed, hard-wired address mask, applied to the top 3 MSBs of incoming addresses. This address mask is given either by the OTP field star_net_otp_addr if otp_add_en bit is set, or from open and short flags of channel 2 green and red colors, when otp_add_en is not set.

The parallel node address defines an address range for its branch. The address range is defined as:

Table 9: Address range

Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
Address mask [2:0]			x	x	x	x	x	x	x

If a parallel node receives a telegram with an address not within its address range (except broadcast and multicast), the telegram is silently discarded.

When branching is enabled via OTP and the branch address range is defined in the OTP too, nevertheless R1 & G1 are not available as LED drivers.

Broadcast messages are forwarded as usual. Multicast messages are forwarded as usual.

To initiate the nodes on the network, the MCU has to send individual INIT commands to each of the “parallel” nodes using the respective hardcoded addresses. INIT refers to either telegram INITBIDIR or INITLOOP.

For example, MCU starts the initialization with the main trunk, e.g. with INIT(0x001), followed by the initialization of the branches, e.g. INIT(0x080), INIT(0x100) ... INIT(0x080) will start the initialization procedure of the first branch only and the nodes in this branch will be initialized with addresses 0x081, 0x082, etc. The nodes of other branches will ignore this initialization command as it is not addressed to their address range.

Due to the fixed address ranges, there is a discontinuity of addresses between the various branches before and after the branching point. Therefore, in order to use serial broadcast commands (see Commands section) each branch has to be addressed individually and only after the response of the previous branch has been received.

Information:

The host is fully responsible for the timing of the telegrams propagating in the network and, in particular, for collision avoidance.

Instead of setting the parallel mask in the OTP, it can also be configured via channel 2 pins, see next section. Parallel addressing is fully supported only with fully symmetrical communication modes, such as SPI-mode, LVDS mode, CAN mode (USE mode). Pure MCU mode will result in communication errors at parallel devices that are not addressed, while MCU - SPI mode supports parallel communication, given its symmetry in downstream and upstream flows.

6.5.2 Parallel address setting with open-short

It is possible to configure 2 LED drivers to receive altogether 2 analog voltage signals that are to be forced externally. Possible configurations are three: Ground shorted, VDD shorted, or thirdly at VDD/2 voltage level, e.g. by resistive ladder.

The LED driver is turned-OFF (high-Z) and in combination with an external resistor divider will set the output voltage.

The 2 analog voltages are digitized by the open-short comparators and result in 9 possible parallel address codes.

The parallel mask configuration is read once at startup.

Table 10: Address mask configuration

G1	R1	Internal bits	Corresponding parallel address
VDD/2	VDD/2	00 00	0b000
VDD/2	GND	00 01	0b001
VDD/2	VDD	00 10	0b010
GND	VDD/2	01 00	0b011
GND	GND	01 01	0b100
GND	VDD	01 10	0b101
VDD	VDD/2	10 00	0b110
VDD	GND	10 01	0b111

6.5.3 MCU mode (Type A MCU Mode)

Figure 12: Incoming telegrams diagram (Manchester encoded)

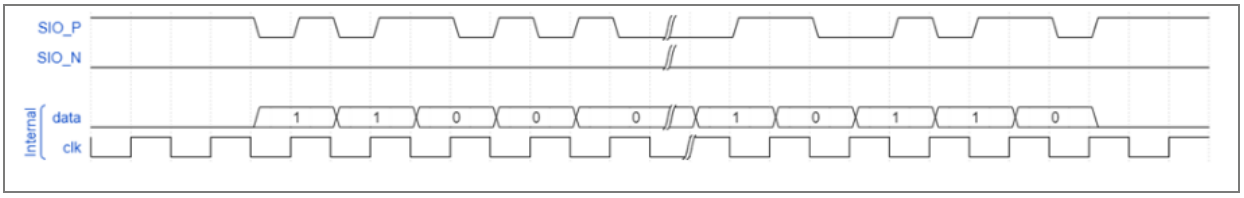
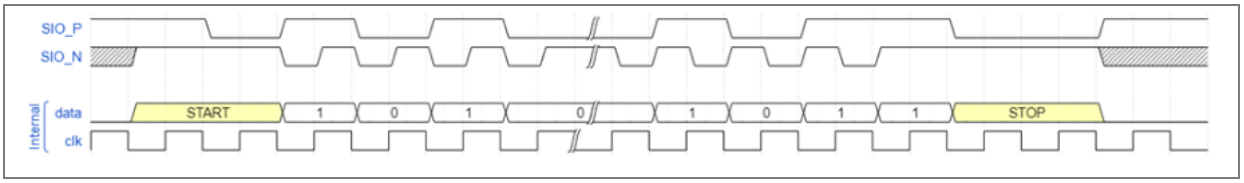


Figure 13: Outgoing telegrams timing diagram (Data and Clock)



The device will wait for nominal 5 µs before sending a response telegram.

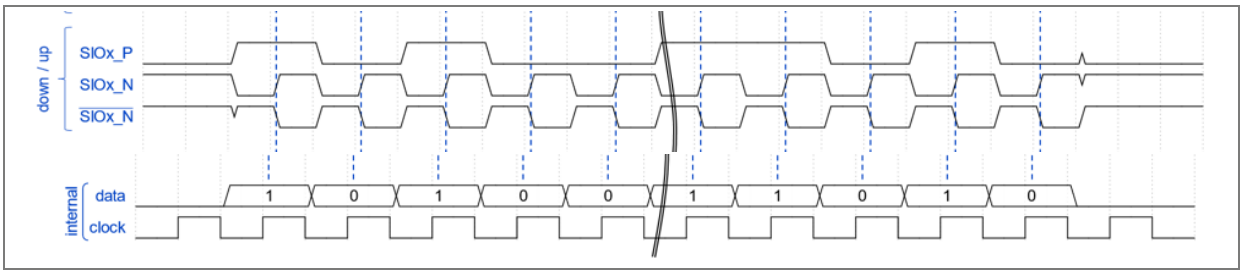
This is intended to leave the time to the MCU to reconfigure the interface direction to receive the response, in case it is required.

SIO2N is always forced high by the device, differently from OSIRE E3731i, where the line is left open to follow the low voltage set by external pull-down (this transition is greyed out in picture and is not visible in AS1163 SAID).

6.5.4 MCU mode, EOL

The figure below illustrates the signals for the MCU mode EoL (pull-down on SIO_P and pull-up on SIO_N and the two possible clock polarities, respectively.

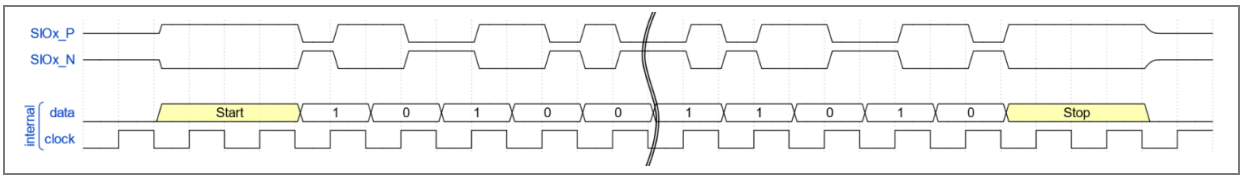
Figure 14: MCU mode EoL



These curves apply both to downstream communication, which is relevant for the loop back mode addressing.

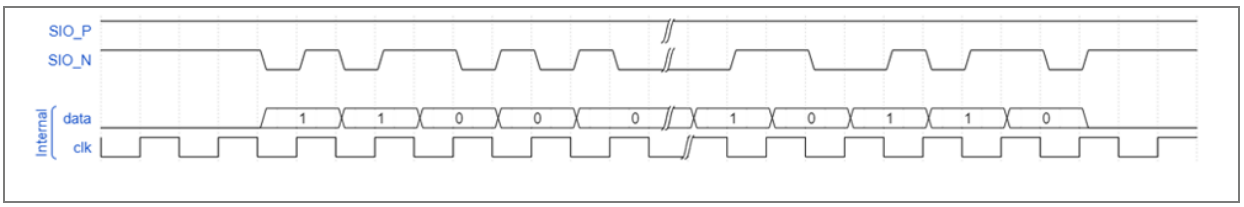
6.5.5 LVDS mode

Figure 15: LVDS timing diagram



6.5.6 CAN mode (USE mode)

Figure 16: CAN timing diagram



In the OSP documentation, this mode is known as USE. It is often referred to as CAN, as it enables the use of CAN-FD transceivers. The signal on the SIO ports is not yet CAN, that is only after the transceiver.

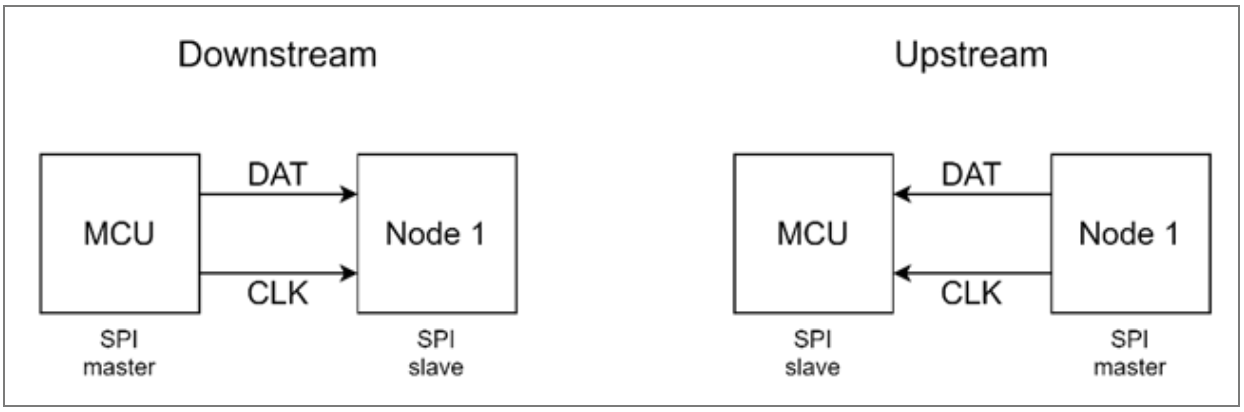
6.5.7 SPI mode (Type B MCU Mode)

This is an alternative option in MCU mode that is activated when the SPI_mode bit is set in the OTP customer block.

In this case, instead of sending a Manchester encoded data SIO1_P, the MCU will send clock and data. Responses (like in MCU mode type A) also use separate clock and data.

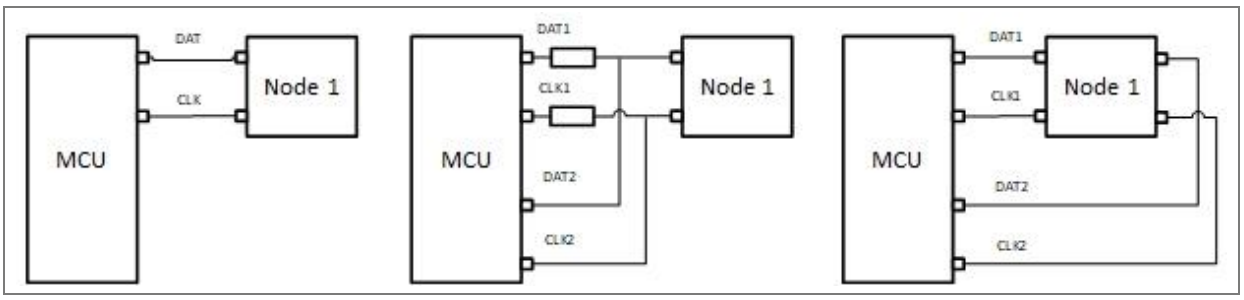
Both downstream and upstream communication use a regular SPI interface with clock and data signals with NRZ coding (no Manchester encoding):

Figure 17: SPI mode



The SPI sender role is always taken by the transmitting device, i.e., for downstream communication by the MCU and for upstream communication by the first node. There are three possible options to realize this on MCU side:

Figure 18: SPI mode – connection options

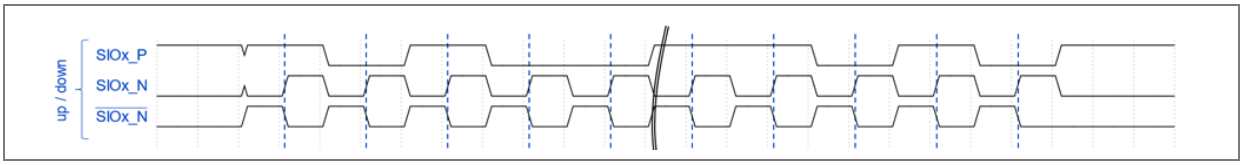


Referring to Figure 18 the first two options work in bidirectional mode, the third option only for the loop-back mode. When 2 SPI ports are used on the MCU, the first is always sender and the second is always receiver. The two resistors in the second case are needed to decouple the sender and receiver pins (the ports in the case that both act as sender at the same time).

When only 1 SPI port is used, the MCU needs to toggle the SPI role between sender and receiver after a message has been sent and before the response is received. SAIDs apply a wait time of min. 5 µs between the end of an incoming telegram and the start of a response that is sent back to the sender. The clock phase on SIOx_N is selectable through register settings, using the COM_INV bit in the SETUP register.

The figure below illustrates the signals for the SPI Type B MCU mode (pull-up on SIO_P and pull-down on SIO_N and the two possible clock polarities, respectively.

Figure 19: SPI mode



Information:

SPI is only supported on SIO1 port.

6.5.7.1 SCK interruptions in SPI mode

An internal counter operating at the system clock is reset periodically at every edge of the external clock (reconstructed clock in case of a Manchester signal).

The internal counter flags a communication error, 8 system clock cycles after the last clock edge.

For example:

- Nominal system clock of 19.2 MHz resulting in a period of about 52 ns.
- The timeout is flagged after 8 system clock cycles, or 416 ns.
- SCK interruptions can be tolerated if below 416 ns. Otherwise, a communication error is detected and communication fails to receive the message.

6.6 LED driver

Each LED driver is implemented as an open-drain current sink.

A slope control circuit defines the steepness of the PWM turn-on and turn-off edges. A bias circuit provides the DC bias current, where 5 levels are selected with a thermometric code.

Drivers are grouped in 3 channels with 3 drivers each. Channels are sized with a current capability of respectively 48 mA (Channel 0), 24 mA (Channel 1), 24 mA (Channel 2).

Selectable current levels are 3 mA, 6 mA, 12 mA, 24 mA, 48 mA for Channel 0.

Selectable current levels are 1.5 mA, 3 mA, 6 mA, 12 mA, 24 mA for Channel 1 and Channel 2.

Table 11: Current levels configuration table

CUR setting	0	1	2	3	4
Channel 0	3 mA	6 mA	12 mA	24 mA	48 mA
Channel 1	1.5 mA	3 mA	6 mA	12 mA	24 mA
Channel 2	1.5 mA	3 mA	6 mA	12 mA	24 mA

ILED_acc, ILED_mis parameters refer to the CUR setting 4, where trimming is performed. A performance degradation for lower settings is to be expected.

The current drivers are controlled by a PWM with a frequency up to nominally 1000 Hz and a PWM resolution (duty cycle) of 14-bit. Higher resolution of 15-bit is achieved with nominal 500 Hz frequency.

Enabling Dithering function allows to achieve 16-bit dynamic range (not available with Sync functionality).

Current driver activation is performed with phase shift in digital to reduce the peak to average power ratio.

The current of the drivers is stable over the full temperature range to avoid any color/brightness shift. The LED dependencies over temperature can be compensated via PWM adjustment depending on the readout value of the temperature sensor.

6.6.1 LED temperature compensation

In color-accurate RGB applications, the host MCU synthesizes a color with the PWM settings of the 3 LED drivers for each channel. In this case, each PWM triplet is already taking into account the chip temperature.

Chip junction temperature is obtained by a status register request, as estimation of the LED temperature, creating an accurate color despite the absolute LED temperature variations.

This feature implements small corrections to the programmed PWM values, proportionally to the difference between the reference temperature and the actual temperature, in steps of 4 LSBs.

The temperature correction factor is sent by the host together with the reference temperature using SETTCOEFFCHN telegram. Once the absolute delta between actual temperature and reference temperature is larger than k*TEMP_STEP, k=1,2,3,… the correction factor is applied to the PWM proportionally using the formula:

Equation 2:

$$PWM(T) = PWM\,(Tref)\,[1 + \alpha\,(Tref)(T - Tref)]$$

Before every new PWM frame is started, the temperature delta is checked and in case compensation is required this is calculated and applied one channel at a time.

Programmed temperature coefficient and reference temperature can be read by the READTCOEFFCHN command.

The compensation happens only when the device is in active state.

The following conditions will automatically trigger a start of compensation calculation process:

1. Host changes any PWM values, current value, reference temperatures or correction factors.
2. Actual temperature changes.
3. Device state goes from sleep/deep-sleep to active state

Within one compensation calculation, compensation of every driver is calculated once and in a sequential manner R0, B0, G0, R1, B1, G1, R2, B2, G2. For each driver it takes 55 system clock cycles to complete (2.86 µs). So, for one entire compensation, it takes nominally (55*9) + 1 clock cycles = 25.83 µs to complete.

To disable this function, host should set the correction factor all to zero.

All corrected PWM values are reset to 0 when the device is not in active state.

The corrected PWM values are clamped between 0 and 16'd65535 to prevent overflow or negative value.

There could be a PWM frame with intermediately (or wrongly) corrected PWM values when host modifies the related registers while the device is actively running. Because the reference temperatures/correct factors/original PWM values may be set separately by host in different time slot. It could happen that the compensation is done with the old reference temperature but with the new correction factor or new PWM values. The compensation is only guaranteed to be correct one PWM frame after all the registers are stable.

There could also be an intermediate (or wrong) RGB combination if the IC temperature changes between the compensation of two drivers within the same channel. The RGB color is only guaranteed to be correct one PWM frame after the IC temperature is stable.

Host MCU can read both the original PWM values or the corrected PWM values with the same READPWMCHN command but with different payload.

Meanwhile the LEDs and the driver chip heat-up or cool-off due to a different self-heating. Until the next temperature readout and PWM setting, color can potentially drift.

6.6.2 LED channel clustering

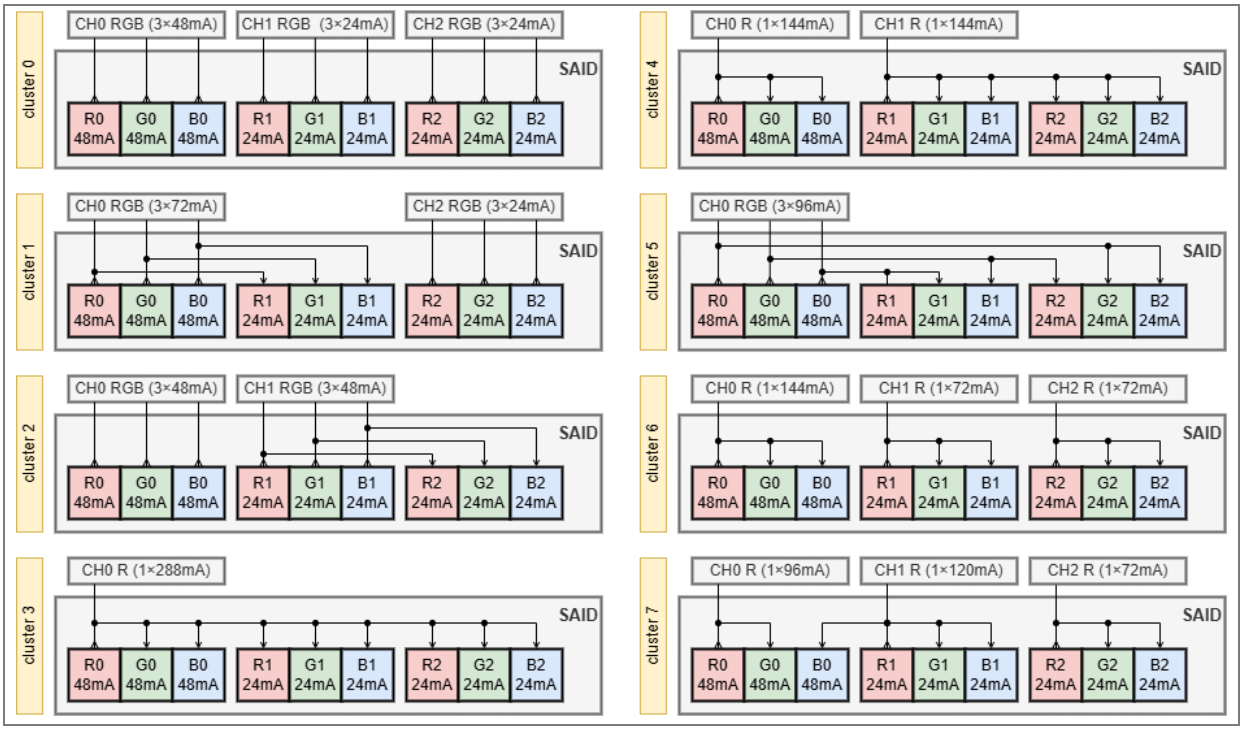
It is possible to connect the output drivers together to a single LED with a higher current. When the drivers are clustered, the output of the drivers is synchronized in power, frequency and shift. As a result, channel clustering preserves color quality. Technically, this means that the SETPWMCHN and SETCURCHN to the main driver is also used for the aggregated drivers.

With the CH_clustering bits in the OTP it is possible to select the configurations that are shown in Figure 20.

When clustering is deployed, the PCB shall short-circuit the clustered drivers to merge the currents. For example, when using clustering 2 (see Figure 20), R1 and R2, G1 and G2, and B1 and B2, shall be connected together in the PCB respectively.

The outgoing arrows in Figure 20 denote the main driver, the incoming arrows the sub or aggregated drivers; only SETPWMCHN to main drivers have effect, SETPWMCHN to sub drivers are ignored. Similarly, SETCURCHN to main drivers have effect, SETCURCHN to sub drivers are ignored."

Figure 20: Output clustering



6.6.3 Haptic driver

AS1163 can be used to drive a haptic actuator, by programming the OTP bit “haptic_driver” to 1. In this mode all drivers are clustered and the PWM frequency is reduced.

The PWM setting is taken over by the channel 0 RED setting (this is equivalent to CH_clustering = 3).

When the haptic actuator driving mode is selected, the PWM frequency is reduced with respect to the normal PWM frequency. So, it will be 146 Hz (nominally 150 Hz) when PWM speed is set to “low” or 293 Hz (nominally 300 Hz mode), when PWM speed is set to “fast”.

6.7 PWM control

PWM engine has a resolution of 15 bits @ 500 Hz and 14 bits @ 1 kHz nominal frame rate, while the PWM word is 16 bits including 1 extra bit for the dithering function.

The additional LSB can be used also for an automatic dithering functionality, where the LSB value is toggled every frame. This can work with 14 bits or 15 bits PWM modes and also with full dithering mode.

6.7.1 PWM LSB dithering (Auto dithering)

The engine cannot work natively with 16 bits, as the resulting PWM carrier frequency would be too low for high quality lighting (ghosting, flicker effects).

An interpolation mechanism is provided, which automatically activates if the LSB is 1.

For example, if the 16-bit PWM register is set to 2, the PWM will execute the code 1 in 15-bit word, furthermore, setting it to 3 will result in the alternate execution of codes 1 and 2 in a 15-bit word. Same behavior is followed in 1 kHz mode, when the PWM will use only 14-bit: In this case the code 4 in 16-bit word will be executed as 1 in a 14-bit word, and the code 6 will be executed alternatively with the codes 1 and 2 in 14-bit word (the LSB of the 16-bit word will be discarded with the 1 kHz mode).

Information:

With 500 Hz mode, LSB dithering will be disabled if the register is written with 0xFFFF (it would cause a wrap around) and with 0x0001 (it will cause continuous ON and OFF states of the PWM driver).

With 1 kHz mode, LSB dithering will be disabled if the register is written with 0xFFFE and 0xFFFF (it would cause a wrap around) and with 0x0002 (it will cause continuous ON and OFF states of the PWM driver).

6.7.2 PWM dithering

The PWM dithering function is meant to increase the effective PWM carrier frequency. In order to reduce under-sampling artifacts in human vision, the PWM duty cycle is broken down in 8 equally spaced pulses.

Setting the DITHERING_EN bit in the CURRENT register will enable the dithering functionality on the PWM engine. The automatic dithering to extend the 15-bit mode to 16-bit will remain active, but the dithering setting will have effect on the 15-bit PWM engine. The dithering mode must be used with 500 Hz mode only. The normal PWM period is divided in 8 parts, and the PWM high period is also divided by 8, so that the nominal PWM frequency becomes 4 kHz (4688 Hz in reality) for every PWM code that is higher than 8 LSB in the 15-bit word (16 bits in the 16-bit word).

For PWM settings lower than 8, the period is divided by the number of high-cycles (the effective frequency will depend on this number).

For PWM settings that result in a number of high-cycles distant less than 8 cycles from full-scale, the period is nevertheless sub-divided in 8 parts by a low cycle. This results in an effective maximum PWM setting of full-scale minus 8. This means that the maximum value that is representable without saturation is 0xFFF8, all other higher values are saturated to the maximum PWM output.

6.7.3 PWM frequency selection

The PWM frame frequency is programmable with the settings being 160 Hz, 320 Hz, 500 Hz, 1 kHz. The first two settings are meant to be used for the external haptic actuator driving.

Approximations to the values, to achieve the frequencies by division from the clock frequency are accepted.

6.7.4 PWM linearity

The integral nonlinearity (INL) of the PWM after removal of systematic offsets is less than 0.2 LSB over the full PWM operating range.

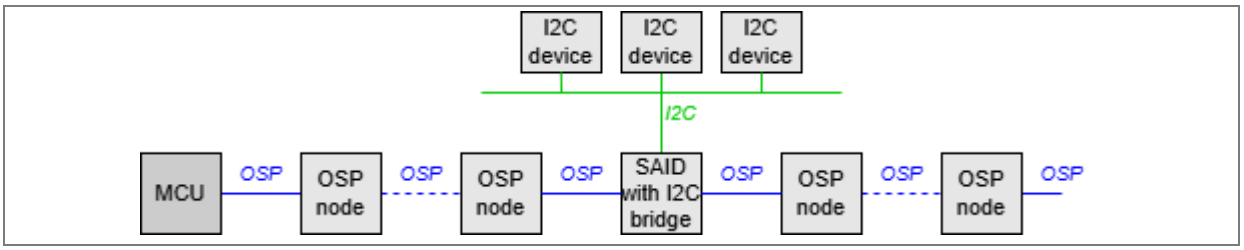
6.7.5 PWM phase shift

Each driver is shifted by 1/9 of period respect to the other drivers (in this way every 1/9 of a period 1 driver is active at low duty cycles).

6.8 I²C bridge

The device can operate as an OSP-to-I²C-gateway as illustrated in the Figure 21, using one LED channel for the I²C pads.

Figure 21: OSP-to-I²C bridge



Note: In an I²C read transaction, the AS1163 does not generate the clock pulse for the last ack/nack.

6.8.1 I²C bridge configuration

If the OTP bit I2C_BRIDGE_EN is high, channel 2 is configured as I²C bridge.

A dedicated de-glitch filter provides protection against glitches with nominal duration < 50 ns, complying with the I²C standard.

Specifically, the drivers belonging to channel 2 are re-purposed to serve as I²C-compatible interface (R2, G2, B2 become SDA, SCL and INT) as shown in Table 2 and Table 3 external pull-up resistors to VDD are required: The value of the pull-ups depends on system design, see “I²C-bus specification and user manual” UM10204 section 7.1 for details. A typical value is 4.7kOhm.

The third driver of the channel is permanently OFF and working as digital input for the interrupt bit, which is active low. The interrupt flag is stored into the I²C register and is available to the customer for reading (see READI2CCFG).

Table 12: Channel 2 configuration when I²C bridge is enabled

	R2	G2	B2
I²C function	SDA	SCL	INTERRUPT
Driver enable state (direction)	Input/output	Output	Input

Interrupt is captured by the digital part via a dedicated register.

Note: The I²C master in the AS1163 has one known behavior: In a read transaction the last pulse (clock and data) for final NACK is not emitted. Most I²C devices will sync on the subsequent STOP condition, so the read terminates successfully, however, there might be devices that go out of sync. I²C clock stretching is not supported.

When channel 2 is configured as I²C bridge, the current level of the driver can still be configured via SETCURCHN.

A value of 3mA (CUR=1) is recommended as the minimum current requirement for the lower bound of an external pull up resistor, 2.2 kOhm, is 2.5 mA.

6.8.2 I²C control register

I²C control register is an 8-bit register that contains the division factor to set the I²C speed. Default value at startup is 0xC (1100 or 12 dec). The complete division factor must be left shifted by 3 bits, so that the real division factor is 1100000 (96 dec). This value is used to divide the sys clock to generate the I²C half clock period. With a main clock of 19.2 MHz this means an I²C frequency of about 92 kHz.

The formular to calculate the target I²C frequency from the register setting is the following, assuming nominal I²C loading conditions given by 5 kOhm pull-up resistor and 20 pF parasitic line capacitance (division factor can be subject of minor deviations depending on the bus loading conditions as an effect of the I²C master sensing the line to ensure the bus is idle upon starting transmission):

Equation 3:

$$f_{SCL} = f_{osc}/(2 * (8 * I2C\_SPEED + 7))$$

Note: Typically, f_SCL=1371kHz at I2C_SPEED=0; f_SCL=417 kHz at I2C_SPEED=2.

Information:

Divisor must be different from 0, so writing it to 0 must be avoided.

Table 13: I²C control register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3:0
I2C_INT	I2C_12BITADDR	I2C_NACKACK	I2C_BUSY	I2C_SPEED
Read	Read/write	Read	Read	Read/write
High when INT pad (B2) is connected to GND	Sets 12-bit addressing mode for I2CREAD and I2CWRITE telegrams	Status of ack bit of last I²C transaction	Set if the last I²C transaction was completed	Division factor to set the speed of the I²C bus (see formula above)

Within the I2CCFG register only bit 3:0 plus bit 6 can be written, the other bits are read only.

The I2CCFG register allows to check the actual division factor for I²C speed. It is also recommended to read this register after every I²C operation and check the bit 5 with nack/ack information: When this is 1, it means that last I²C read or write operation ended with a NACK from the I²C device so an error occurred, if this bit is 0 the last communication ended correctly with an ACK.

If bit 4 is still 1, it means that the I²C device is still busy and the last read or write operation is not finished yet.

Setting bit 6 of I²C control register will enable the use of devices that require 12-bit addressing via I²C.

Bit 7 will be set if the I²C interrupt pin is low; there is no latching.

6.9 SYNC configuration

When the SYNC_EN bit is set in the CURRENT register, new PWM values are not applied until a sync signal is received. The sync can be either software, given form the SYNC command, or hardware, from a toggling of the sync pin. In this last case, also the SYNC_PIN_EN bit must be set in the OTP.

This functionality is required for display-like applications.

6.9.1 SYNC pin activation

The SYNC pin functionality is activated by a dedicated OTP bit SYNC_PIN_EN (see Table 6). If the OTP bit is not set, the SYNC telegram can be used instead.

6.9.2 SYNC operation

Upon reception of a SYNC event, either from an external pin or OSP command, the device activates all drivers with pre-configured settings.

Default state of the SYNC line is high. To give a sync, the SYNC line is pulsed low for at least 3 clocks a 2.4MHz (1.25µs).

6.10 Multicasting

In addition to the broadcast, multicast groups can be defined. Devices can be assigned to one or more groups within this range via a dedicated command. Once assigned, these devices react to both the general broadcast address 0x000 as well as to the multicast group address.

Multicast group addresses are within the range from 0x3F0 to 0x3FE.

There are 15 different addresses for multicast groups available. A node can be registered to any of these by setting the respective bit in the 16-bit mask register:

Table 14: Multicast group address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Group	-	3FE	3FD	3FC	3FB	3FA	3F9	3F8	3F7	3F6	3F5	3F4	3F3	3F2	3F1	3F0

Messages addressed to a multicast group are always fast-forwarded.

6.11 Diagnostics

All error/diagnostic modes will set a unique flag bit if it occurs. An automatic transition into SLEEP mode & disabling of the LED can be configured via the SETUP register. The last PWM parameters are retained. The flag bit will be cleared by a status readout (READSTAT, READTEMPSTAT). If the failure is still present the flag is raised again. RESET also clears all flags.

6.11.1 Undervoltage failure

Sets STATUS.UV_FLAG (bit 0) when there is an under voltage event.

The event takes place with VDD_UV. If VDD falls below the VDD_UV threshold, the corresponding flag bit will be set after a de-glitch time. The flag bit will be deleted when the Status Register is requested by host and VDD is recovered to VDD>VDD_UV.

6.11.2 Overvoltage failure

In case the internal regulator fails (an unlikely and rare event) resulting in an over-voltage condition for the internal circuitry being supplied by it, an over-voltage monitor provides a flag to enable detection. Such conditions can be dangerous, as oscillator and digital circuitry can suffer reduced lifetime and failure while operating above maximum absolute limits.

This flag can be used at system level to react accordingly and implement functional safety measures.

This event sets STATUS.OV_FLAG (bit 4).

The flag is cleared upon read-out of the status register and is raised again if the condition persists.

When a SAID comes out of RESET, its OV_FLAG is always set. It is advised to broadcast a CLRERROR or perform an individual READSTAT / READTEMPSTAT after RESET and INIT.

6.11.3 Overtemperature failure

Sets STATUS.OT_FLAG (bit 1) when an overtemperature event occurs.

The temperature level and relative hysteresis is defined in Table 4 and it is required to avoid thermal overstress of the IC. The flag bit will be deleted when the Status Register is requested by host and temperature is lower than the hysteric value.

Refer to commands SETOTTH, READOTTH for accessing the overtemperature threshold register. Default or lower values are mandatory.

6.11.4 Driver fault – LED short to VDD

Set STATUS.LOS_FLAG (bit 2) when there is an LED short event (see also LED open). READLEDSTCHN register shows the detailed error status.

A fault can be detected while a driver is active and the PWM value is larger than the minimum PWM value set in the OTP non-customer area). This behavior is related to parameter LED_Pers.

This function is available while the device is in active mode and at least 1 full PWM frame after active mode is entered. Also, after a READSTAT, READLEDSTCHN (which clear the flags) at least 1 full PWM frame is needed to re-check the status.

The flag bit will be deleted, when the Status Register is requested by host and the corresponding fault is no longer present.

Note: Default (minimal PWM) value is 512. At high quantity orders, other threshold values can be programed by ams OSRAM.

Table 15: Min PWM values for SHORT detection

OTP bit1	OTP bit 0	OPEN/SHORT min. PWM threshold value
0	0	512
0	1	-
1	0	-
1	1	-

6.11.5 Driver fault – LED open

Set STATUS.LOS_FLAG (bit 2) when there is an LED open event (see also LED short). READLEDSTCHN register shows the detailed error status.

A fault can be detected while a driver is active and the PWM value exceeds the minimum PWM value set in the OTP non-customer area (. This behavior is related to parameter LED_Pers.

This function is available while the device is in active mode and at least 1 full PWM frame after active mode is entered.

The flag bit will be deleted, when the Status Register is requested by host and the corresponding fault is no longer present.

Note: Default value is 512. At high quantity orders, other threshold values can be programed by ams OSRAM.

Table 16: Min PWM values for OPEN detection

OTP bit 1	OTP bit 0	OPEN/SHORT min PWM threshold value
0	0	512
0	1	-
1	0	-
1	1	-

6.11.6 Communication failure

Sets STATUS.CE_FLAG (bit 3) when there is a communication error. A flag bit is set if a message is wrong (PSI, CRC) for all messages even when they do not address the device. The transfer will not be stopped.

A CE flag bit due to a wrong command will be set only if this message was addressed to this device (for forward compatibility).

The flag bit will be deleted when the Status Register is requested by host or deleted.

Table 17: Communication error matrix

Device addressed	PSI matches payload	CRC is correct	PSI matches command	Communication error
Yes	Yes	Yes	Yes	No
Yes	-	-	No	Yes
Yes	-	No	-	Yes
Yes	No	-	-	Yes
No	Yes	Yes	-	No
No	-	No	-	Yes
No	No	-	-	Yes

PSI (Payload Size Indicator): The size of the payload is defined by the PSI field in the telegram. The following table shows the PSI value vs. payload size:

Table 18: PSI

PSI			Payload size (byte)
Bit2	Bit1	Bit0	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	8

6.11.7 OTP signature failure

Sets STATUS.TEST_FLAG (bit 5) when there is an OTP signature error related to the reserved area.

7 Command and register description

The Figure 22 illustrates how the communication block handles each telegram (in open system protocol OSP) in case the device has already been addressed while Figure 23 the case for un-addressed device.

Figure 22: Telegram handling for addressed device

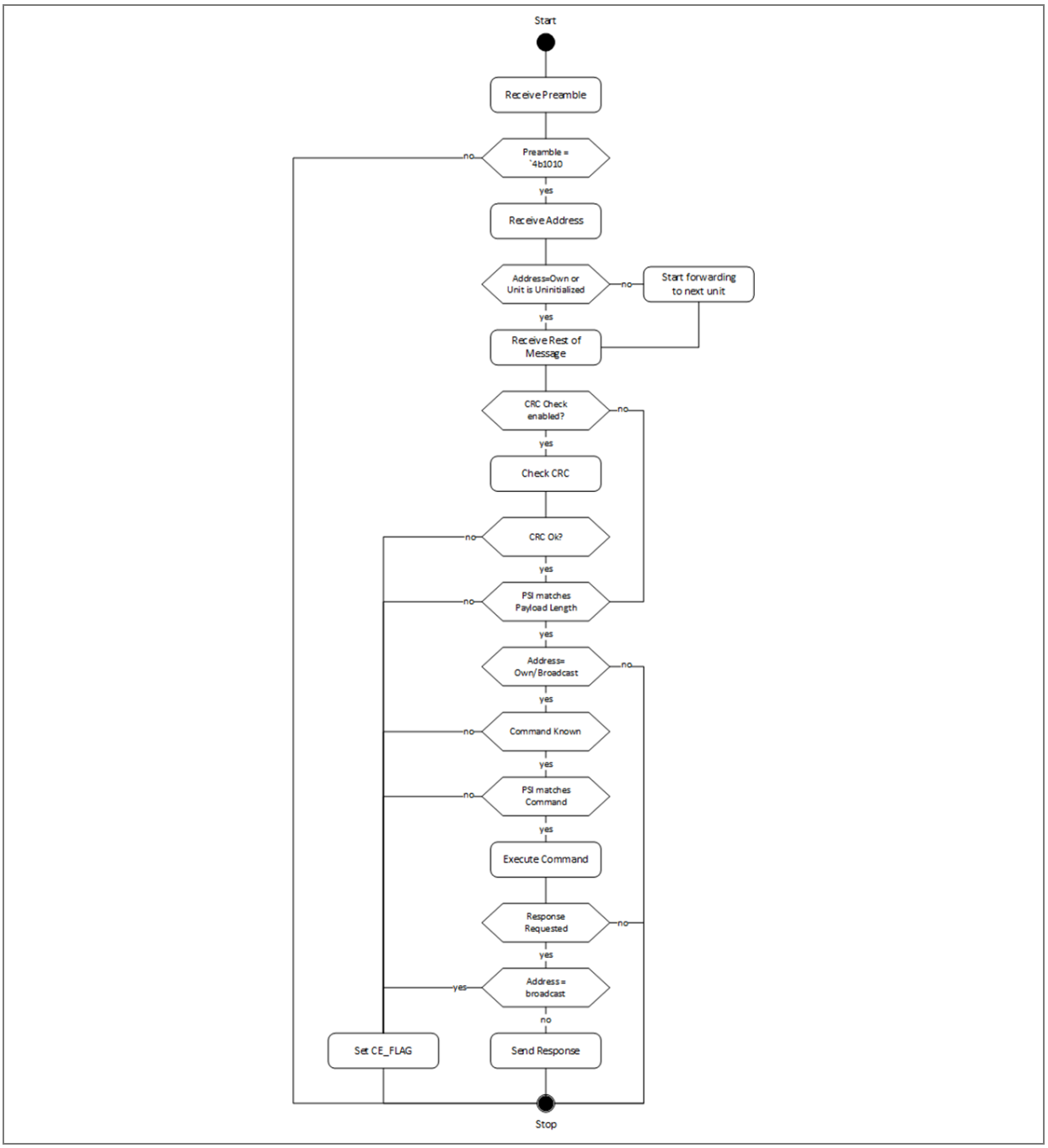
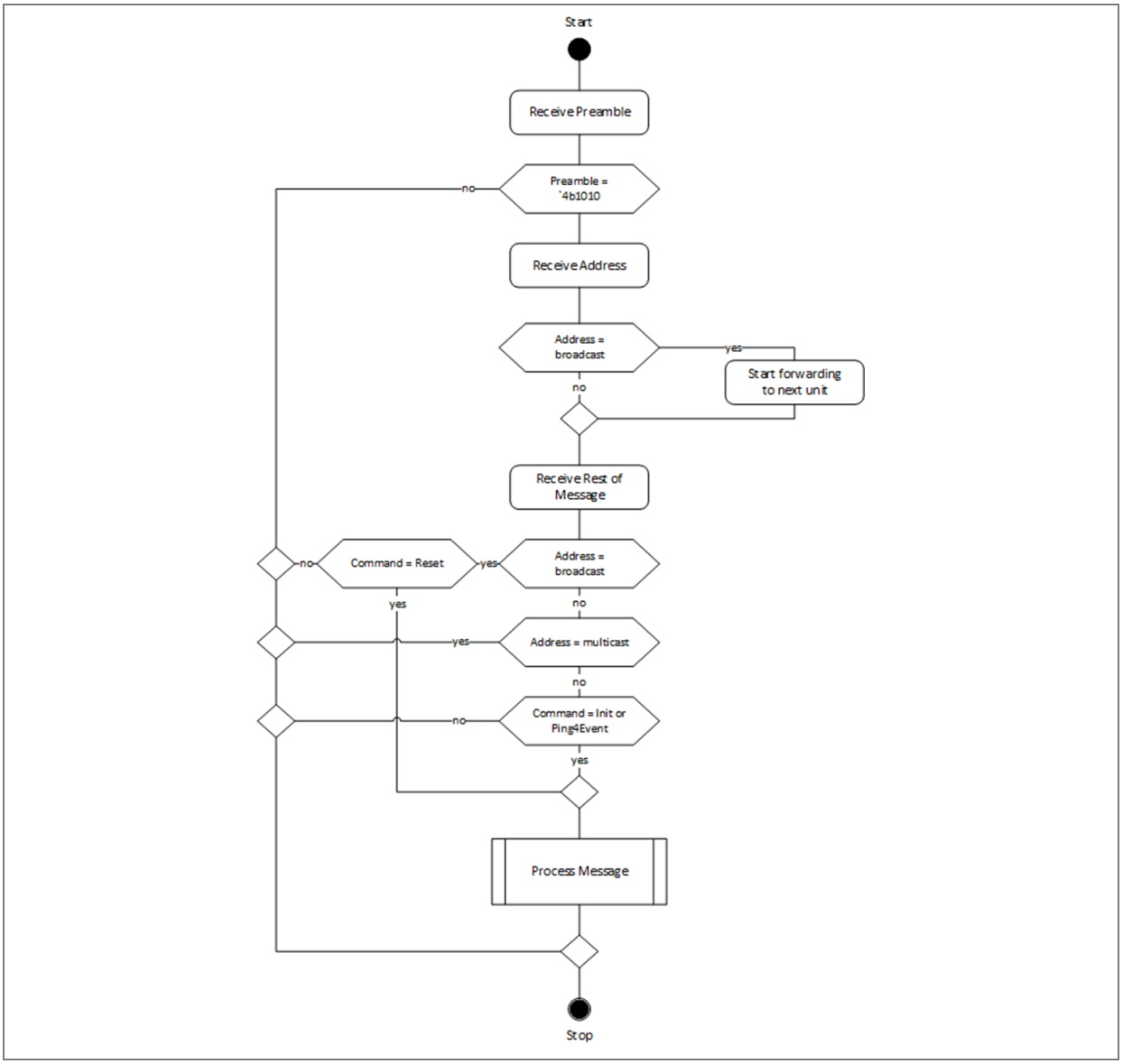


Figure 23: Telegram handling for un-addressed device



7.1 Incorrect preamble

Telegrams with incorrect preamble will be silently discarded without raising an error flag. They will not be forwarded. The command will not be interpreted by the node.

7.2 Invalid address

Telegrams with an address 0x3FF will be silently discarded without raising an error flag. They will not be forwarded. The command will not be interpreted by the node.

7.3 Premature end of message

If the transmission ends before the expected number of bits (given by the PSI value) has been received, an error flag will be raised. The command will not be interpreted by the node.

As forwarding may start before the message has been fully received, forwarding will not be stopped.

7.4 Additional data after end of message

If the transmission continues after the expected number of bits (given by the PSI value) has been received, these additional bits will be silently discarded. No error flag will be raised.

As forwarding may start before the message has been fully received, forwarding will not be stopped.

7.5 Incorrect CRC

If the CRC check word is incorrect, an error flag shall be raised. The message shall not be interpreted by the node.

As forwarding may start before the message has been fully received, forwarding shall not be stopped.

7.6 Unknown command

If a node receives an unknown command an error flag will be raised.

The unknown command will not be executed.

7.7 Incorrect length of argument

Some commands expect an argument delivered in the payload.

If the length of the argument does not match the expectation, an error flag will be raised.

In this case the command will not be executed.

7.8 Broadcast readout attempt

If a readout command is received via the broadcast address 0x000, an error flag will be raised.

The command will not be executed.

7.9 Inappropriate broadcast / multicast attempt

If a serial broadcast command (INIT, INIT_LOOP, PING4EVENT) is received via the broadcast address 0x000 or via a multicast address, an error flag will be raised.

The command will not be executed, and forwarding will be stopped.

7.10 Command overview

The structure of the available 7 bits for a command (= command encoding) is as shown in Table 19. For each command and a potential answer sent back to a MCU, the payload is defined. Payload is transmitted with MSB-first (big-endian).

Device registers are used to control the device behavior and can be used to monitor the device status. A register can be read only or can support read/write operations, following the marking below:

R: Bit or bit field is read only.

RW: Bit or bit field can be written and read.

RC: Bit or bit field is read only and bit(s) will be automatically cleared after readout.

W: Bit or bit field is write only, readout will deliver always 0.

Table 19: Command overview

6 R/C[1]	5 SR[2]	4	3	2	1	0	Name	Function	Code	Broadcast / multicast	Payload sent #of bit	Payload answer # of bit
0	0	0	0	0	0	0	RESET	Reset	0x00	Yes	0	-
0	SR	0	0	0	0	1	CLRERROR	Clear error flag	0x01 0x21	Yes	0	16 if SR
0	0	0	0	0	1	0	INITBIDIR	Init Address bidir	0x02	Serial	0	16
0	0	0	0	0	1	1	INITLOOP	Init address loopback	0x03	Serial	0	16
0	SR	0	0	1	0	0	GOSLEEP	Enter sleep	0x04 0x24	Yes	0	16 if SR
0	SR	0	0	1	0	1	GOACTIVE	Go Active	0x05 0x25	Yes	0	16 if SR
0	SR	0	0	1	1	0	GODEEPSLEEP	Deep Sleep	0x06 0x26	Yes	0	16 if SR
0	0	0	0	1	1	1	IDENTIFY	Ask device ID	0x07	No	0	32
0	0	0	1	0	0	0	P4ERRBIDIR	Ping4Err in bidir mode	0x08	Serial	0	16
0	0	0	1	0	0	1	P4ERRLOOP	Ping4Err in loopback	0x09	Serial	0	16
0	0	0	1	0	1	0	ASKTINFO	Max/Min Temp feedback	0x0A	Serial	0/16	16
0	0	0	1	0	1	1	ASKVINFO	Max/Min Volt feedback	0x0B	Serial	0/16	16
0	0	0	1	1	0	0	READMULT	Read multicast reg	0x0C	No	0	16
0	SR	0	1	1	0	1	SETMULT	Set multicast reg	0X0D 0x2D	No	16	16 if SR
0	0	0	1	1	1	1	SYNC	Sync chain	0x0F	Yes	0	-

6 R/C(1)	5 SR(2)	4	3	2	1	0	Name	Function	Code	Broadcast / multicast	Payload sent #of bit	Payload answer # of bit
0	SR	1	0	0	0	1	IDLE	OTP in idle	0x11 0x31	No	0	16 if SR
0	SR	1	0	0	1	0	FOUNDRY	OTP in foundry	0x12 0x32	No	0	16 if SR
0	SR	1	0	0	1	1	CUST	OTP in cust mode	0x13 0x33	No	0	16 if SR
0	SR	1	0	1	0	0	BURN	OTP in burning	0x14 0x34	No	0	16 if SR
0	SR	1	0	1	0	1	AREAD	OTP analog reag	0x15 0x35	No	0	16 if SR
0	SR	1	0	1	1	0	LOAD	OTP Load	0x16 0x36	No	0	16 if SR
0	SR	1	0	1	1	1	GLOAD	OTP Gload	0x17 0x37	No	0	16 if SR
0	SR	1	1	0	0	0	I2CREAD	Read I²C	0x18 0x38	Yes	24	16 if SR
0	SR	1	1	0	0	1	I2CWRITE	Write I²C	0x19 0x39	Yes	24-64	16 if SR
0	0	1	1	1	1	0	READLAST	Read last I²C read	0x1E	No	0	64

(1) R/C indicates a “command” when R/C bit is 0 or indicates a “Register access” when R/C bit is 1.
(2) SR requests the Status Register response. SR = 0 means no answer is required, SR=1 requires the device to reply with Status information. Not allowed for broadcast and multicast messages.

In case a command is broadcast to all devices (ADDRESS == 0x000), no device is allowed to send out an answer.

For commands allowed to request a status from a device, bit no. 5 in command must be set. This is only allowed when a command is addressing a specific device (ADDRESS > 0x000). A device receiving a command with bit no.5 set (is allowed) will send back an answer to a controller containing at 16-bit payload with STATUS and TEMPERATURE register content, similar to the READTEMPSTAT command.

7.11 Register command overview

Table 20: Register overview

6 R/C[1]	5 SR[2]	4	3	2	1	0 W/R	Name	Function	Code	Broadcast/ multicast	Payload sent # of bit	Payload answer # of bit
1	0	0	0	0	0	0	READSTAT	Read status	0x40	No	0	8
1	0	0	0	0	1	0	READTEMPSTAT	Read Temp & Status	0x42	No	0	16
1	0	0	0	1	0	0	READCOMST	Read Com Status	0x44	No	0	8
1	0	0	0	1	1	0	READLEDSTCHN	Read LED Status	0x46	No	0	8
1	0	0	1	0	0	0	READTEMP	Read Temp	0x48	No	0	8
1	0	0	1	0	1	0	READOTTH	Read OV_THE	0x4A	No	0	24
1	SR	0	1	0	1	1	SETOTTH	Set OV_THE	0x4B 0x6B	Yes	24	16
1	0	0	1	1	0	0	READSETUP	Read Setup	0x4C	No	0	8
1	SR	0	1	1	0	1	SETSETUP	Set Setup	0x4D 0x6D	Yes	8	16
1	0	0	1	1	1	0	READPWMCHN	Read PWM	0x4E	No	8	48
1	SR	0	1	1	1	1	SETPWMCHN	Set PWM	0x4F 0x6F	Yes	64	16 if SR
1	0	1	0	0	0	0	READCURCHN	Read Current setting	0x50	No	8	16
1	SR	1	0	0	0	1	SETCURCHN	Set Current	0x51 0x71	Yes	24	16 if SR
1	0	1	0	0	1	0	READTCOEFFCHN	Read T coeff.	0x52	No	8	40
1	SR	1	0	0	1	1	SETTCOEFFCHN	Set Temp coeff.	0x53	Yes	40	16 if SR
1	0	1	0	1	0	0	READADC	Read ADC	0x54	No	0	8
1	SR	1	0	1	0	1	SETADC	Set ADC	0x55 0x75	Yes	8	16 if SR
1	0	1	0	1	1	0	READI2CCFG	Read I²C cfg	0x56	No	0	8
1	SR	1	0	1	1	1	SETI2CCFG	Set I²C cfg	0x57 0x77	Yes	8	16 if SR
1	0	1	1	0	0	0	READOTP	Read OTP	0x58	No	8	64
1	SR	1	1	0	0	1	SETOTP	Set OTP	0x59 0x79	Yes	64	16 if SR
1	0	1	1	1	0	0	READADCDAT	Read ADC input data	0x5C	No	0	10

6 R/C(1)	5 SR(2)	4	3	2	1	0 W/R	Name	Function	Code	Broadcast/ multicast	Payload sent # of bit	Payload answer # of bit
1	SR	1	1	1	1	1	SETTESTPW	Set TESTPW	0x5F 0x7F	No	48	16 if SR

(1) R/C indicates a “command” when R/C bit is 0 or indicates a “Register access” when R/C bit is 1.
(2) SR requests the Status Register response. SR = 0 means no answer is required, SR=1 requires the device to reply with Status information. Not allowed for broadcast and multicast messages.

7.12 Telegram commands

7.12.1 RESET (0x00)

Performs complete reset of one or all devices (RESET access takes time; wait 150µs after sending this telegram before sending next.), goes into default state, delete error flags, all registers are reset to their default, this includes the devices address (no longer in "addressed" state) but excludes the OTP P2RAM.

Due to its startup behavior, the AS1163 comes out of RESET with the OV-FLAG set blocking the AS1163 to execute a GOACTIVE telegram. It is advised to send a CLRERROR after INIT.

7.12.2 CLRERROR (0x01)

Clears all error flags, if an error still exists (for example short/open), the error flag is set again.

7.12.3 INITBIDIR (0x02)

This command initializes the chain of SAIDs in bidirectional mode.

If a device is not addressed: Device sets device address to received ADDRESS, transfers same command with new address field ADDRESS+1 to next device. Last device sends TEMPSTAT register with device address to controller.

This command will set the answer direction to controller to BIDIR mode.

7.12.4 INITLOOP (0x03)

This command initializes the chain of SAIDs in loop-back mode.

If a device is not addressed: Device sets device address to received ADDRESS, transfers same command with new address field ADDRESS+1 to next device. Last device sends TEMPST register with device address to controller.

This command will set the answer direction to controller to LOOPBACK mode.

7.12.5 GOSLEEP (0x04)

Puts device into "SLEEP" state: The LED drivers are disabled. The last PWM parameters are stored. PWM settings and current settings are possible. During SLEEP mode diagnostic is possible and readable.

7.12.6 GOACTIVE (0x05)

Puts device into "ACTIVE" state: The LED drivers are disabled. The last PWM parameters are stored. PWM settings and current settings are possible. During SLEEP mode diagnostic is possible and readable.

7.12.7 GODEEPSLEEP (0x06)

Puts device into "DEEPSLEEP" state: The LED drivers are disabled. The last PWM parameters are stored. PWM settings and current settings are possible. During SLEEP mode diagnostic is possible and readable.

7.12.8 IDENTIFY (0x07)

No payload. Answer is 32-bit DEVICE ID.

DEVICE ID is 0x00000040.

7.12.9 P4ERRBIDIR (0x08)

It will check only the selected flag bits which leads to SLEEP state (setup register).

If an error flag is set in STATUS with its FSAVE set in SETUP, then: Answer to host (state + temperature) in reverse (BIDIR) direction.

If not: Same command will be forwarded to next device with a new address field (STARTADDRESS+1).

If no error flag bit in chain: Last device sends status + temperature register in reverse (BIDIR) direction.

Serial broadcast message.

Information:

The command shall be used with the address of the first device of the chain only. Using an address from a unit in the middle of the chain might lead to unpredictable behavior of the chain until a reset condition (e.g. power loss).

7.12.10 P4ERRLOOP (0x09)

It will check only the selected flag bits which leads to SLEEP state (setup register).

If an error flag is set in STATUS with its FSAVE set in SETUP, then: Answer to host (state + temperature);

If not: Same command will be forward to next device with a new address field (STARTADDRESS+1).

If no error flag bit in chain: Last device sends status + temperature register.

Serial broadcast message.

Information:

The command shall be used with the address of the first device of the chain only. Using an address from a unit in the middle of the chain might lead to unpredictable behavior of the chain until a reset condition (e.g. power loss).

7.12.11 ASKTINFO (0x0A)

Returns the aggregated maximum and minimum temperature (see Chapter 6.4.1.2) across the daisy chain.

Serial broadcast message.

Last node responds with min and max temperature.

The 16-bit payload contains the max temperature and the min temperature in this order.

Table 21: Payload of ASKTINFO

Payload of answer		ASKTINFO		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
15:8	TEMPMAX[7:0]	0x0	R	8-bit value of the max. temperature in daisy chain
7:0	TEMPMIN[7:0]	0x0	R	8-bit value of the min. temperature in daisy chain

7.12.12 ASKVINFO (0x0B)

Returns the aggregated maximum and minimum local forward voltage among all nodes across the daisy chain.

Serial broadcast message.

Last node responds with min and max voltage of local nodes.

The 16-bit payload contains the max Vf and the min Vf in this order.

Table 22: Payload of ASKVINFO

Payload of answer		ASKVINFO		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
15:8	VFMAX_MAX[7:0]	0x0	R	8-bit value of the max VFMAX
7:0	VFMAX_MIN[7:0]	0x0	R	8-bit value of the min VFMAX

Equation 4:

$$Vf\_MAX = VDD - VDRV = ADC\_GAIN\_VF * (VFMAX\_MAX * 4 - 2)$$

$$Vf\_MIN = VDD - VDRV = ADC\_GAIN\_VF * (VFMAX\_MIN * 4 - 2)$$

Where,

Vf_MAX/Vf_MIN is maximum/minimum VFMAX value of all nodes in the daisy chain,

VDD is the applied external supply at VDD pin of AS1163 in V,

ADC_GAIN_VF is a parameter,

VDRV is the selected driver output voltage,

VFMAX_MAX/ VFMAX_MIN is the ADC reading of VFMAX,

-2 is a systematic offset.

Note: VFMAX is 8-bit internal register for each AS1163. It stored the max. value (Vf) of each AS1163. So, the min. Vf is the minimum local VFMAX in the whole daisy chain (not the lowest Vf of all LEDs).

7.12.13 READMULT (0x0C)

This command returns the multicast register content of the device. For payload information, please refer to Chapter 6.10.

7.12.14 SETMULT (0x0D)

This command specifies the multicast register inside the device. For payload information, please refer to Chapter 6.10.

No answer.

7.12.15 SYNC (0x0F)

Software sync resulting (see Chapter 6.9) in latching of latest PWM settings, assuming SYNC has been enabled for the device (SYNC_EN bit is set in the CURRENT register).

The command can be sent to a specific address, or group or broadcast address.

Takes no argument.

7.12.16 I2CREAD (0x18)

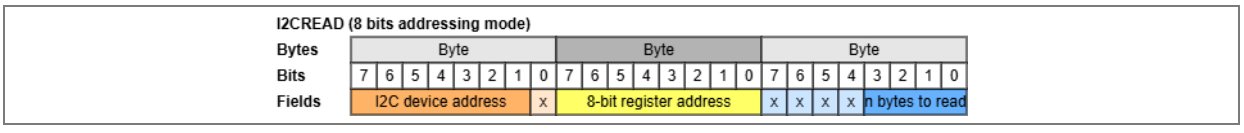
Request n bytes (1≤n≤8) of data from a register in an I²C device.

The SAID I²C bridge first asserts I2CCFG.I2C_BUSY. Next, it starts an I²C transaction consisting of a write segment (with the register address), followed by a read segment (with the data from that register). When the device does not acknowledge during the write segment, the transaction is aborted, and I2CCFG.NACK_ACK is asserted. When the device does acknowledge, the bridge continues with the read segment, which is stopped after the selected number of bytes (n) has been received (always “succeeds” since the devices no longer sends acks); then I2CCFG.NACK_ACK is de-asserted. After abort or successful completion I2CCFG.I2C_BUSY is de-asserted; it would stay asserted as long as the target device pulls the SCL low (“I²C clock stretching”).

The PSI of the I2CREAD telegram is fixed at 3 (a payload length of 24 bits) for both the 8-bit mode and the 12-bit mode (see I2CCFG. I2C_12_BIT_ADDR), but the fields are somewhat different.

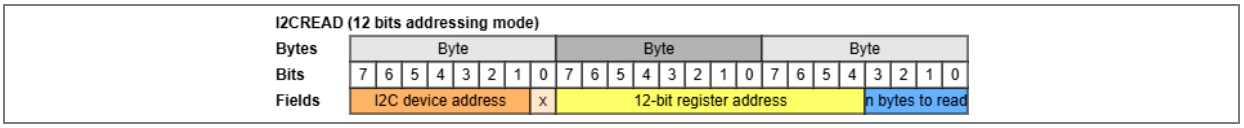
In 8-bit addressing, the first byte is the I²C device address (7-bit I²C address plus adding a 0 LSB). The second byte is the I²C register address from where the read starts. Last 4 bits of the third byte indicate the number of bytes to read (n, with value 1 to 8).

Figure 24: I2CREAD 8-bit addressing



If 12-bit addressing is asserted (I2CCFG. I2C_12_BIT_ADDR), the first byte is the I²C device address (7-bits with appended 0) and the second and third bytes form the 12-bit I²C register address from where the read starts. The I²C write segment is 16 bits, prepending 0b0000. The last 4 bits of the third byte indicate the number of bytes to read (n, with value 1 to 8).

Figure 25: I2CREAD 12-bit addressing



The I2CCFG status register reflects the status of the I²C transaction (fields I2C_BUSY and I2C_NACKACK) but no response telegram is sent with the read data. Instead, the data is stored in a 64-bit register inside the SAID, which can be read with the telegram READLAST.

For details, please refer to application note “I²C bridge – SAID as I²C gateway AN001090”.

7.12.17 I2CWRITE (0x19)

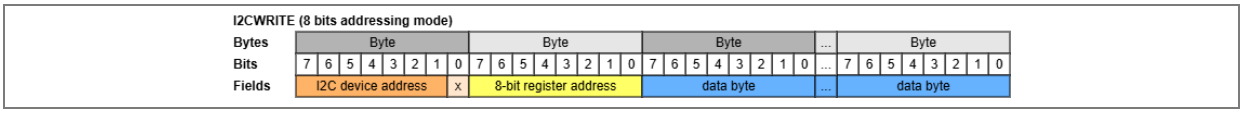
Writes bytes to a register in an I²C device.

The SAID I²C bridge first asserts I2CCFG.I2C_BUSY. Next, it starts an I²C transaction consisting of a single write segment. This contains the register address, followed by data. When the device does not acknowledge one of the bytes, the transaction is aborted, and I2CCFG.NACK_ACK is asserted. When the device does acknowledge all bytes, I2CCFG.NACK_ACK is de-asserted. After abort or successful completion I2CCFG.I2C_BUSY is de-asserted; it would stay asserted as long as the target device pulls the SCL low (“I²C clock stretching”).

The PSI of the I2CWRITE telegram indicates how many bytes will be written, address bytes and data bytes together.

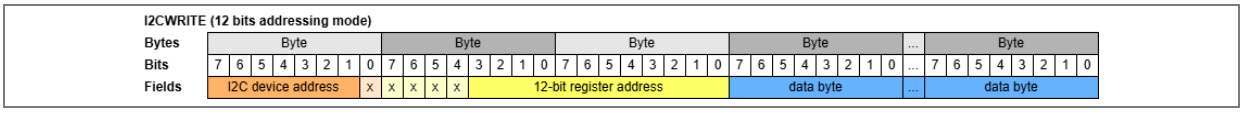
In 8-bit addressing, the first byte is the I²C device address (7-bit I²C address plus adding a 0 LSB). The second byte is the I²C register address where to write to. Next come 1 to 6 data bytes. Because a PSI of 7 cannot be encoded, 5 data bytes cannot be sent.

Figure 26: I2CWRITE 8-bit addressing



If 12-bit addressing is asserted (I2CCFG. I2C_12_BIT_ADDR), the first byte is the I²C device address (7-bits with appended 0) and the second and third bytes form the 12-bit I²C register address where to write to. Only the 12 LSBs in the telegram are significant, the I²C transaction uses 16 bits, prepending 0b0000. Next come 1 to 5 data bytes. Because a PSI of 7 cannot be encoded, 4 data bytes cannot be sent.

Figure 27: I2CWRITE 12-bit addressing



For details, please refer to application note “I²C bridge – SAID as I²C gateway AN001090”.

7.12.18 READLAST (0x1E)

The READLAST returns the bytes from the last I²C transaction. The payload of the READLAST response is always 8 bytes; some constitute the bytes read, some are padding. If the last I2CREAD telegram instructed to read n bytes (n≤8) there are p=8-n padding bytes, and the READLAST response telegram has the following payload.

Table 23: READLAST response telegram

Payload offset	0	1	…	p-1	p	p+1	…	7
Payload content	$padding_0$	$padding_1$	…	$padding_{p-1}$	$data_0$	$data_1$	…	$data_{n-1}$

After every I²C read the data is stored in an internal 64-bit register, no answer is sent on the OSP line to not occupy the bus for a long time. With the READLAST it is possible to read this data after that the previous I²C read operation is completed (see status in READI2CCFG).

7.13 Register access commands

The description of the registers in this section refers to the payloads of the telegrams. Payload is stored in big endian.

7.13.1 READSTAT (0x40)

Read back the status register:

- State (active, sleep)
- Test mode
- Overvoltage
- Communication error
- LED short/open
- Over temperature
- Under voltage

Table 24: READSTAT register

Addr: 0x40		READSTAT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	STATE[1:0]	0x0	R	“00” initialized “01” sleep “10” active “11” deep sleep
5	TEST_FLAG	0x0	R	When this flag is set, a device is either in TEST mode or OTP CRC1 is wrong (= OTP error)
4	OV_FLAG	0x0	RC	Will be set when device detected an overvoltage condition. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
3	CE_FLAG	0x0	RC	When set, device detected an error in a received telegram, either CRC error (when enabled in “SETUP” register) or length error or other error at protocol or data link layer. Telegrams are always checked, no matter is a device had been addressed by a telegram or not. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
2	LOS_FLAG	0x0	RC	Will be “1” when in any of the LED channels either a short or open defect has been detected. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
1	OT_FLAG	0x0	RC	Will be set when device detected overtemperature condition. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
0	UV_FLAG	0x0	RC	Will be set when device detected an undervoltage condition. Will be automatically cleared after readout and set again if error still exists (Sticky flag).

Permanent clearing of LOS_FLAG requires a read-out of LEDSTCHN register beforehand, as the LOS_FLAG signals the presence of any high flag in that register.

7.13.2 READTEMPSTAT (0x42)

Read registers from addressed devices:

- Status
- Temperature

Table 25: READTEMPSTAT register

Addr: 0x42		READTEMPSTAT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
15:14	STATE[1:0]	0x0	R	“00” initialized “01” sleep “10” active “11” deep sleep
13	TEST_FLAG	0x0	R	When this flag is set, a device is either in TEST mode or OTP CRC1 is wrong (= OTP error)
12	OV_FLAG	0x0	RC	Will be set when device detected an overvoltage condition. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
11	CE_FLAG	0x0	RC	When set, device detected an error in a received telegram, either CRC error (when enabled in “SETUP” register) or length error or other error at protocol or data link layer. Telegrams are always checked, no matter is a device had been addressed by a telegram or not. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
10	LOS_FLAG	0x0	RC	Will be “1” when in any of the LED channels either a short or open defect has been detected. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
9	OT_FLAG	0x0	RC	Will be set when device detected overtemperature condition. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
8	UV_FLAG	0x0	RC	Will be set when device detected an undervoltage condition. Will be automatically cleared after readout and set again if error still exists (Sticky flag).
7:0	TEMPVALUE[7:0]	0x0	R	8-bit value of the temperature sensor (see Chapter 6.4.1.2 for format)

7.13.3 READCOMST (0x44)

Read COMSTATUS register:

- Loop/bi-directional
- SIO1_STATE
- SIO2_STATE

Table 26: READCOMST register

Addr: 0x44		READCOMST		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	Reserved	0x0	R	-
4	COM_MODE	0x1	R	Indicates the mode used by a device to send back telegram to a MCU: "0": Bidirectional mode, same SIO used to send back answer telegram "1": Loopback, opposite SIO is used to send back answer telegram
3:2	SIO2_STATE[1.0]	0x0	R	"00" LVDS mode "01" EoL (End of Line) mode "10" MCU mode "11" CAN mode (USE mode)
1:0	SIO1_STATE[1:0]	0x0	R	"00" LVDS mode "01" EoL (End of Line) mode "10" MCU mode "11" CAN mode (USE mode)

7.13.4 READLEDSTCHN (0x46)

Read LED status register.

Payload is 8-bit to select LED channel (0, 1 or 2) to read.

The error flags are set if the fault condition is present for at fixed minimum number of internal clock cycles. See driver fault description.

Each channel contains:

Table 27: READLEDSTCHN register

Addr: 0x46		READLEDSTCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	Reserved	0x0	R	-
6	REDOPEN	0x0	RC	If set indicates a detected OPEN condition on LED3 (= RED). Will be automatically cleared after readout and set again if error still exists (Sticky flag).
5	GREENOPEN	0x0	RC	If set indicates a detected OPEN condition on LED2 (= GREEN). Will be automatically cleared after readout and set again if error still exists (Sticky flag).
4	BLUEOPEN	0x0	RC	If set indicates a detected OPEN condition on LED1 (= BLUE). Will be automatically cleared after readout and set again if error still exists (Sticky flag).
3	Reserved	0x0	R	-
2	REDSHORT	0x0	RC	If set indicates a detected SHORT condition on LED3 (= RED). Will be automatically cleared after readout and set again if error still exists (Sticky flag).
1	GREENSHORT	0x0	RC	If set indicates a detected SHORT condition on LED2 (= GREEN). Will be automatically cleared after readout and set again if error still exists (Sticky flag).
0	BLUESHORT	0x0	RC	If set indicates a detected SHORT condition on LED1 (= BLUE). Will be automatically cleared after readout and set again if error still exists (Sticky flag).

7.13.5 READTEMP (0x48)

Read temperature register.

No payload. Answer is 8-bit.

Table 28: READTEMP register

Addr: 0x48		READTEMP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	TEMPVALUE[7:0]	0x0	R	8-bit value of the temperature sensor (see Chapter 6.4.1.2 for format)

7.13.6 READOTTH (0x4A)

Read OVERTEMPTH register. This register contains low and high thresholds for temperature check.

No payload. Answer is 24-bit.

The values for OT_LOW_VALUE and OT_HI_VALUE are calculated with following formula:

OT_LOW | HI_VALUE = (Tj_C – 25) * 0.85 + 116

Table 29: Format of READOTTH register

Addr: 0x4A		READOTTH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
23:18	Reserved	0x0	R	-
17:16	OT_CYCLE[1:0]	0x3	RW	“00” 1 cycle “01” 2 cycles “10” 3 cycles “11” 4 cycles
15:8	OT_LOW_VALUE[7:0]	0xE6	RW	Low threshold
7:0	OT_HIGH_VALUE[7:0]	0xF0	RW	High threshold

The OT_LOW_VALUE and OT_HIGH_VALUE are defined in the register. For reset values, the overtemperature hysteresis (the difference between low threshold and high threshold) is 10 LSB.

7.13.7 SETOTTH (0x4B)

Set OVERTEMPTH register. This register contains low and high thresholds for temperature check.

Payload is 24-bit. No answer (16-bit TEMPSTAT register if SR bit is set).

The OT_LOW_VALUE and OT_HIGH_VALUE are defined in the register. For reset values, the overtemperature hysteresis (the difference between low threshold and high threshold) is 10 LSB.

7.13.8 READSETUP (0x4C)

Read SETUP register. No payload. Answer is 8-bit.

Table 30: Format of READSETUP register

Addr: 0x4C		READSETUP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	FAST_PWM	0x0	RW	This bit allows to control the PWM speed and by this the dynamic range of the color: 0: 500Hz PWM frame rate with 15 bits dynamic range 1: 1000Hz PWM frame rate with 14 bits dynamic range
6	COM_INV	0x0	RW	This bit does control the clock polarity for transmitted telegrams in “MCU mode”. See chapter 6.5.3 for more details.
5	CRC_EN	0x0	RW	When set to 1, the CRC check is performed on all received telegrams.
4	OTP_FSAVE	0x1	RW	This bit controls how a device behaves when an OTP signature error is detected: 0: Detected error will be set only the flag: TEST_FLAG@STATUS No error answer to P4EVENT command. 1: Detected error will set flag and put device into SLEEP state

Addr: 0x4C		READSETUP		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3	CE_FSAVE	0x0	RW	This bit controls how a device behaves when a communication error is detected: 0: Detected error will be set only the flag: CE_FLAG@STATUS No error answer to P4EVENT command. 1: Detected error will set flag and put device into SLEEP state
2	LOS_FSAVE	0x0	RW	This bit controls how a device behaves when an LED error is detected: 0: Detected error will be set only the flag: LOS_FLAG@STATUS No error answer to P4EVENT command. 1: Detected error will set flag and put device into SLEEP state
1	OT_FSAVE	0x1	RW	This bit controls how a device behaves when an overtemperature error is detected: 0: Detected error will be set only the flag: OT_FLAG@STATUS No error answer to P4EVENT command. 1: Detected error will set flag and put device into SLEEP state
0	UV_FSAVE	0x1	RW	This bit controls how a device behaves when an undervoltage or overvoltage error is detected: 0: Detected error will be set only the flag: UV_FLAG@STATUS OV_FLAG@STATUS No error answer to P4EVENT command. 1: Detected error will set corresponding flag (UV_FLAG or OV_FLAG) and put device into SLEEP state

7.13.9 SETSETUP (0x4D)

Write SETUP register.

Payload is 8-bit. No answer (16-bit TEMPSTAT register if SR bit is set).

7.13.10 READPWMCHN (0x4E)

Read PWM register.

Payload is 8-bit to select the LED channel: 0,1, or 2 for PWM; or 3, 4, and 5 for PWM after temperature correction; or 6, 7, and 8 for driver current.

This command will send back the PWM values of the PWM registers, but also other additional information if the selected channel is higher than 2:

When the payload is 0 to 2, returns the 48-bit PWM register values of the 3 LED drivers for the specified channel.

Table 31: Format of READPWMCHN register (payload from 0 to 2)

Addr: 0x4E		READPWMCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
47:32	RED_PWM[15:0]	0x0	RW	This is the value to be used for the PWM cycle of the RED LED. If FAST_PWM@SETUP = “0” , 15 bits [15:1] are used to realize a 15-bit dynamic range, bit 0 is used for automatic dithering between 2 consecutives PWM frames. If FAST_PWM@SETUP = “1” , 14 bits [15:2] are used to realize a 14-bit dynamic range, bit 1 is used for automatic dithering between 2 consecutives PWM frames.
31:16	GREEN_PWM[15:0]	0x0	RW	This is the value to be used for the PWM cycle of the GREEN LED. If FAST_PWM@SETUP = “0”, 15 bits [15:1] are used to realize a 15-bit dynamic range, bit 0 is used for automatic dithering between 2 consecutives PWM frames. If FAST_PWM@SETUP = “1”, 14 bits [15:2] are used to realize a 14-bit dynamic range, bit 1 is used for automatic dithering between 2 consecutives PWM frames.

Addr: 0x4E		READPWMCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
15:0	BLUE_PWM[15:0]	0x0	RW	This is the value to be used for the PWM cycle of the BLUE LED. If FAST_PWM@SETUP = “0”, 15 bits [15:1] are used to realize a 15-bit dynamic range, bit 0 is used for automatic dithering between 2 consecutives PWM frames. If FAST_PWM@SETUP = “1”, 14 bits [15:2] are used to realize a 14-bit dynamic range, bit 1 is used for automatic dithering between 2 consecutives PWM frames.

When the payload is 3 to 5, returns the PWM register values of the 3 LED drivers after temperature correction for the specified channel.

Table 32: Format of READPWMCHN register (payload from 3 to 5)

Addr: 0x4E		READPWMCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
47:32	RED_PWM_CORR[14:0]	0x0	R	This is the value used for the PWM cycle of the RED LED after the temperature correction algorithm.
31:16	GREEN_PWM_CORR [14:0]	0x0	R	This is the value used for the PWM cycle of the GREEN LED after the temperature correction algorithm.
15:0	BLUE_PWM_CORR [14:0]	0x0	R	This is the value used for the PWM cycle of the BLUE LED after the temperature correction algorithm.

When the payload is 6 to 8, returns the PWM current measured from the current measurement ADC for the 3 LEDs for the specified channel.

Table 33: Format of READPWMCHN register (payload from 6 to 8)

Addr: 0x4E		READPWMCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
23:16	ADC_RED_CURR[7:0]	0x0	R	This is the value of the current measured on the RED LED from the ADC, to check correctness for FUSA.
15:8	ADC_GREEN_CURR [7:0]	0x0	R	This is the value of the current measured on the GREEN LED from the ADC, to check correctness for FUSA.
7:0	ADC_BLUE_CURR [7:0]	0x0	R	This is the value of the current measured on the BLUE LED from the ADC, to check correctness for FUSA.

7.13.11 SETPWMCHN (0x4F)

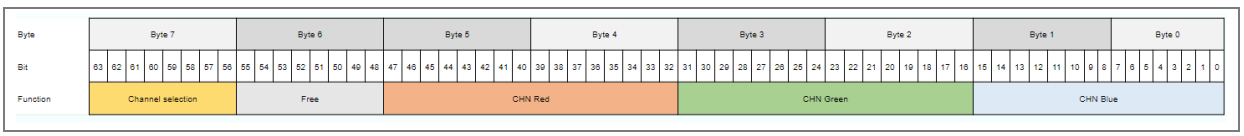
The command contains 3x16-bit words for the PWM setting of the 3 LED drivers and an 8-bit word for the channel selection (0, 1 or 2).

Payload: 64-bit.

Broadcast allowed.

Writes the PWM setting for 3 LED drivers in a specific channel.

Figure 28: SETPWMCHN bit configuration



7.13.12 READCURCHN (0x50)

There is a READCURCHN command for reading each individual LED driver DC current level.

Payload is 8-bit to select LED channel to read (0, 1, or 2).

Broadcast is not allowed.

Answer: 12-bit current configuration for the selected channel.

Table 34: Format of READCURCHN register

Addr: 0x50		READCURCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
15	reserved	0x0	RW	Must be set to 0
14	SYNC_EN	0x0	RW	Enable synchronization of PWM register for the chain: the values written in PWM register are transferred to the PWM engine only after that a SYNC command is received or the SYNC pin is triggered.
13	hyb	0x0	RW	Must be set to 0
12	DITHERING_EN	0x0	RW	Enable dithering mode, PWM frequency will be 4 kHz for PWM values > 8 LSB
11:8	PWM_CURR_RED[3:0]	0x0	RW	This value selects the current output of RED PWM driver. Allowed values in normal operation are from 0 to 4. Values higher than 8 are used only for low current testing.
7:4	PWM_CURR_GREEN[3:0]	0x0	RW	This value selects the current output of GREEN PWM driver. Allowed values in normal operation are from 0 to 4. Values higher than 8 are used only for low current testing.
3:0	PWM_CURR_BLUE[3:0]	0x0	RW	This value selects the current output of BLUE PWM driver. Allowed values in normal operation are from 0 to 4. Values higher than 8 are used only for low current testing.

7.13.13 SETCURCHN (0x51)

Writes the current register of 3 LED drivers in the specified channel.

The command contains 3x4-bit words defining the current levels, an 8-bit word for selecting the channel (0, 1 or 2) and 4 bits for the PWM mode settings (enable, state transition setting, spare bits).

Broadcast is not allowed.

No answer (16-bit TEMPSTAT register if SR bit is set).

Figure 29: SETCURCHN bit configuration

Byte	Byte 2								Byte 1								Byte 0							
Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	Channel selection								free	sync	hyb	dith	Current red				Current green				Current blue			

7.13.14 READTCOEFFCHN (0x52)

Returns the PWM register values of the 3 LED drivers contained in the specified channel.

Payload is 8-bit to select LED channel to read (0, 1, or 2).

Broadcast is not allowed.

Answer: 32-bit PWM configuration for the selected channel.

Table 35: Format of READTCOEFFCHN register

Addr: 0x52		READTCOEFFCHN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
31:24	T_REFERENCE[7:0]	0x0	RW	This value is the reference temperature used to apply the temperature correction.
23:16	T_COEFF_RED[7:0]	0x0	RW	This value selects the temperature coefficient for RED PWM. Default value 0 corresponds to no correction.
15:8	T_COEFF_GREEN[7:0]	0x0	RW	This value selects the temperature coefficient for GREEN PWM. Default value 0 corresponds to no correction
7:0	T_COEFF_BLUE[7:0]	0x0	RW	This value selects the temperature coefficient for BLUE PWM. Default value 0 corresponds to no correction

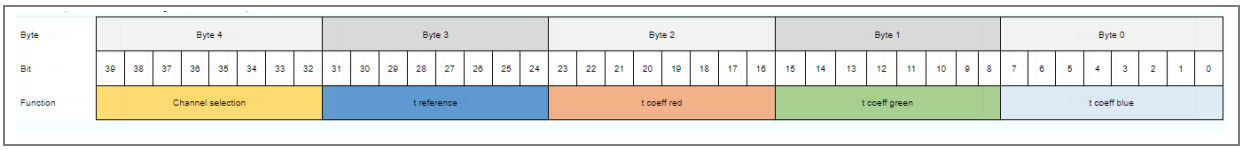
7.13.15 SETTCOEFFCHN (0x53)

Set temperature coefficient in the specified channel.

Contains 40 bits payload: 3x8 bits temperature coefficient, 8 bits temperature reference and 8 bits for channel selection (note that on SAID, having only 3 channels, only 2 bits are used for channel selection using values from 0 to 2).

No answer (16-bit TEMPSTAT register if SR bit is set).

Figure 30: SETTCOEFFCHN bit configuration



7.13.16 READADC (0x54)

The command has no arguments.

The device responds with the ADC register content.

Payload: No payload.

Broadcast is not allowed.

Answer: 8-bit content of the ADC.

Table 36: Format of READADC register

Addr: 0x54		READADC		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	reserved	0x0	RW	-
5	ADC_FUSA_ENABLE	0x0	RW	This enables ADC for LED current measurement for FUSA
4	ADC_VLED_DISABLE_SYNC	0x0	RW	This disable the synchronization of voltage measurement with PWM start pulse (needed if PWM value is 0 and pulse is disabled)
3:0	ADC_VLED_MUX_CTRL[3:0]	0x0	RW	This value selects which LED voltage to measure

7.13.17 SETADC (0x55)

ADC performs the measurements routine with the settings included into the SETADC command.

According to the MUX selection, the ADC register is updated with measurement result.

Payload: 8-bit

Broadcast is not allowed.

Answer: No answer.

7.13.18 READI2CCFG (0x56)

Read the I²C configuration/status register (no payload needed). Answer is 8-bit.

Payload: No payload.

Broadcast is not allowed.

Answer: I²C configuration/status register.

Table 37: Format of READI2CCFG register

Addr: 0x56		READI2CCFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	I2C_INTERRUPT	0x0	R	reflects the status of the INT pin (alternative function of B2)
6	I2C_12_BIT_ADDR	0x0	RW	This enables the 12 bits address mode for I²C.
5	NACK_ACK	0x0	R	Only defined when an I²C transaction is completed (i.e. when I2C_BUSY is de-asserted). This bit is a copy of the last ack bit received from the device (as soon as a device nacks, the I²C transaction is aborted, and this bit will be asserted).
4	I2C_BUSY	0x0	R	When set, the I²C transaction is not yet completed; the SAID is still actively mastering.
3:0	I2C_SPEED[3:0]	0xC	RW	This value selects the divisor factor for I²C speed. (see Chapter 6.8.2)

7.13.19 SETI2CCFG (0x57)

Write the I²C configuration/status register with 8-bit payload. No answer.

Payload: I²C configuration/status register.

Broadcast is not allowed.

Answer: No answer.

7.13.20 READOTP (0x58)

Read data stored in OTP. Payload is 8-bit, address in OTP (mirror) where to start reading. Addresses beyond the OTP size (beyond 0x1F) are read as 0x00 (so no wrap-around).

Answer is 8 bytes read from start byte. The telegram payload has the bytes in big endian. For example READOTP(10) has a response with the read bytes (10..17) in the order 17, 16, .., 10. OTP access takes time; wait 60us after sending this telegram.

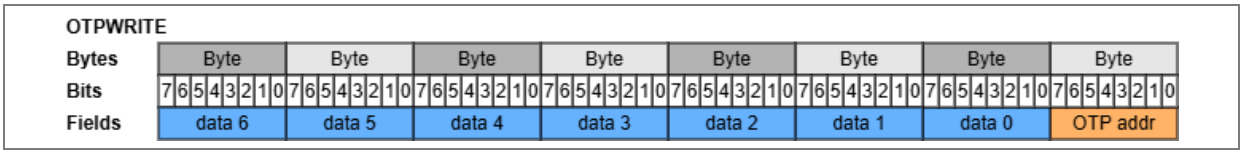
See OTP customer area table (Table 6).

7.13.21 SETOTP (0x59)

Writes 7 bytes to the OTP. It is advised to do read-modify-write on a 7 byte buffer. Addresses beyond the OTP size (beyond 0x1F) are ignored for write (so no wrap-around). The target address is at the end of the telegram, and the 7 data bytes are in reverse order.

The following telegram writes “data 0” to “OTP adder” and “data 1” to OTP addr + 1” and so on up to “data 6” being written to “OTP addr + 6”.

Figure 31: SETOTP



The write is not to the OTP, but to the OTP mirror in device RAM. The mirror is initialized with the OTP content on power on reset. The mirror is not re-initialized by a RESET telegram.

SETOTP only works when the correct password is first sent using TESTPW. Without the TESTPW set, the SETOTP does not update the OTP mirror. The TESTPW must be unset (e.g. set to 0) for normal operation, because when the test password is set, telegram forwarding is impacted.

The OTP access takes time, so wait 60µs after sending this telegram.

The command will be executed only if the authenticated mode is set. This is a test command, so it will be executed also if the device address is not matched. To enter the authenticated mode, please refer to related application note “OTP-burning_AN001081” from ams OSRAM.

See OTP customer area table (Table 6).

7.13.22 READADCDAT (0x5C)

Read ADC data register. Reads ADC data output. Answer is 16-bit (Bit 9 to 0 are related to ADC values) corresponding to the voltage of the LED selected for a measurement in ADC register.

Table 38: READADCDAT register

Addr: 0x5C		READADCDAT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
15:10	ADC_V_OUT[15:10]	0x0	R	Reserved
9:0	ADC_V_OUT[9:0]	0x0	R	This value is the LED voltage measurement

7.14 External components

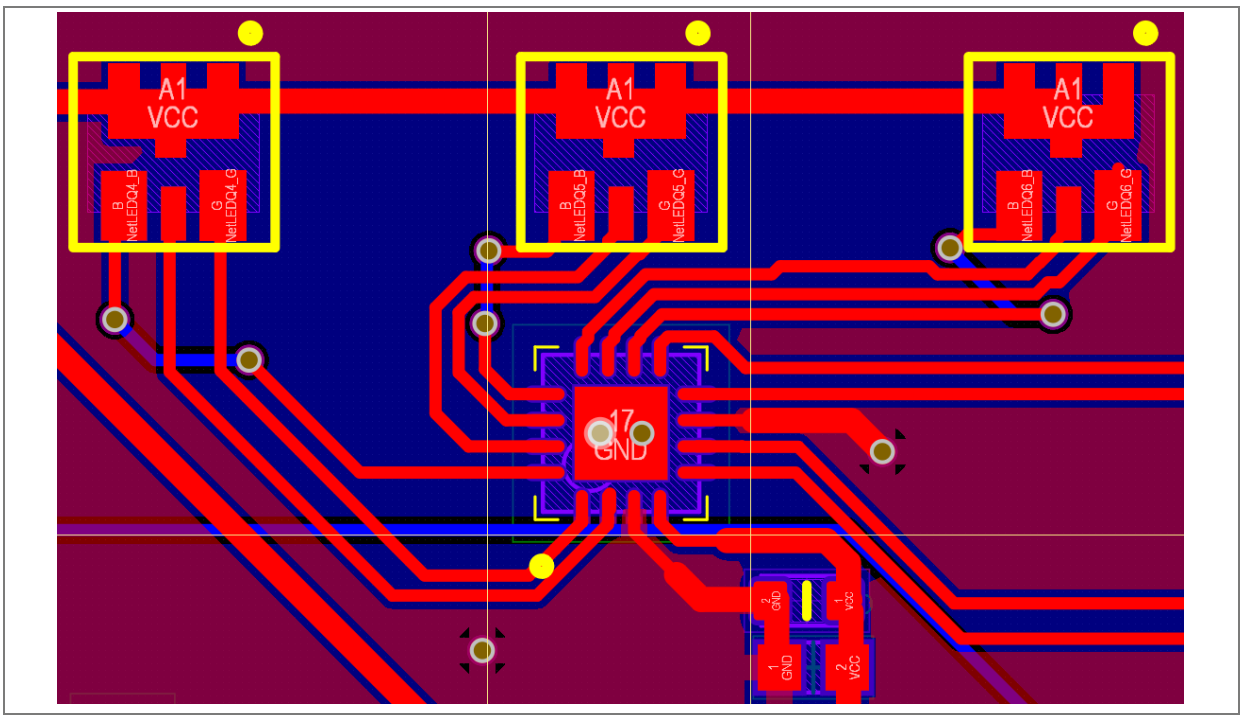
Table 39: Electrical characteristics of AS1163

Symbol	Parameter	Min	Typ	Max	Unit
CVDD	VDD Cap		1		µF
CHFCAP	VDD HF Cap		100		nF
RMODE	Pull-up & Pulldown Res on SIO		10k		Ohm

(1) Recommended values of components to be placed.

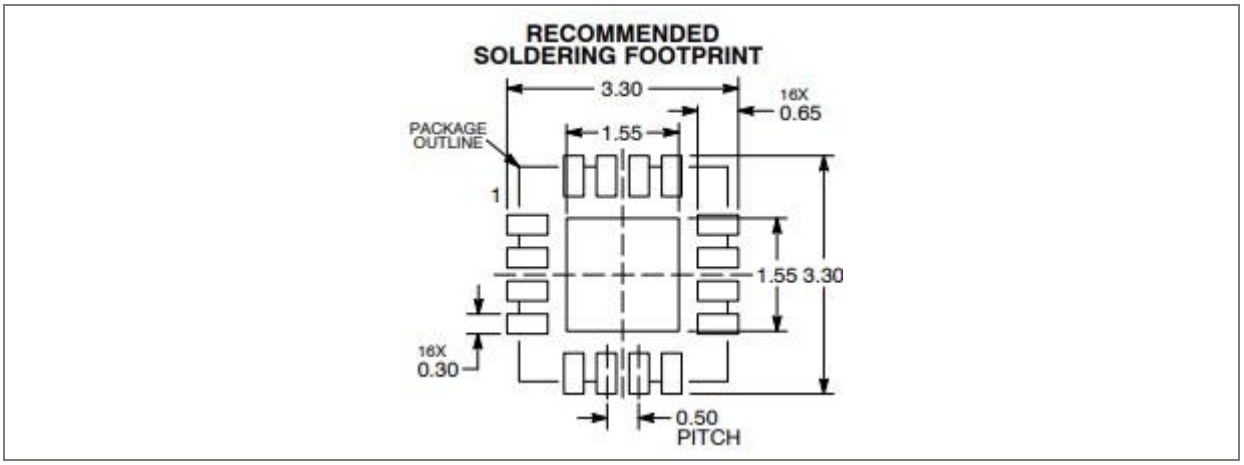
7.15 PCB layout

Figure 32: Single layer PCB layout



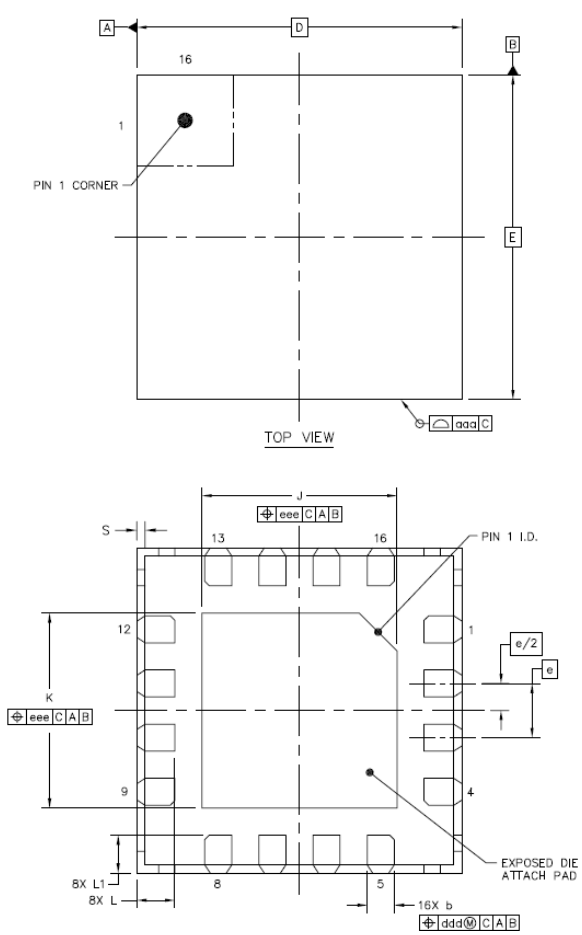
7.16 PCB pad layout

Figure 33: Footprint



8 Package drawings & markings

Figure 34: AS1163 package outline drawing



Ref.	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2		0.65	
A3		0.203	
b	0.2	0.25	0.3
D, E		3	
e		0.5	
J, K	1.7	1.8	1.9
L	0.3	0.35	0.4
L1	0.25	0.35	0.4
aaa,bbb		0.1	
ccc		0.08	
ddd,eee		0.1	

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

9 Tape & reel information

Figure 35: AS1163 tape and reel

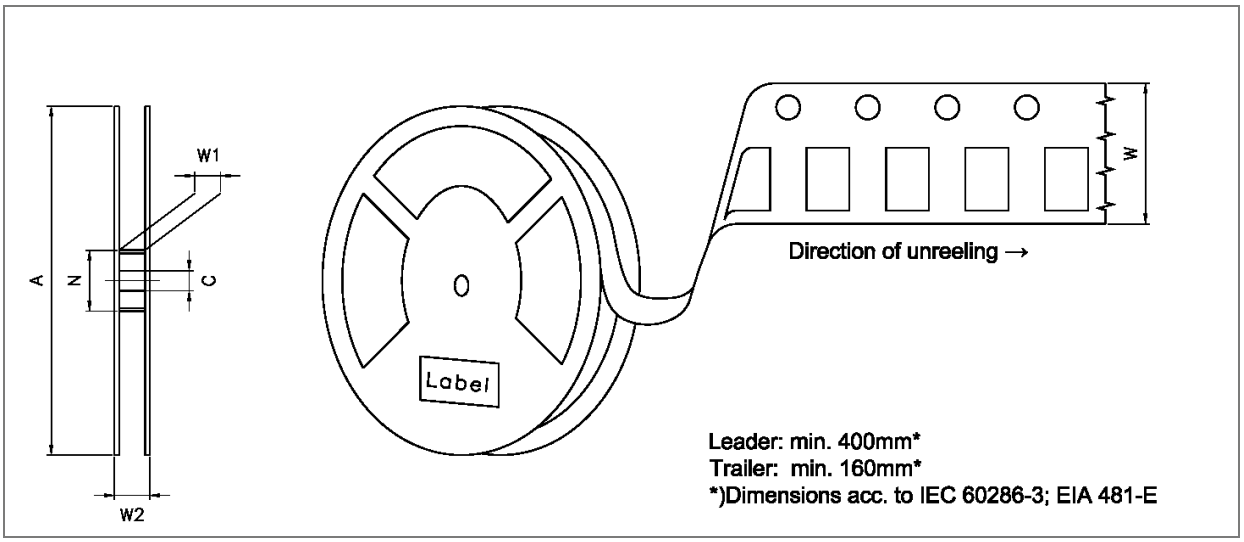


Table 40: Reel dimensions

A	W	N_{min}	W_1	W_{2max}	Pieces per PU
330 mm	12 + 0.3/-0.3 mm	102 mm	12.8 mm	18.2 mm	5000
180 mm	12 + 0.3/-0.3 mm	60 mm	12.4 +2/-0 mm	18.4 mm max	1000

10 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Document security class is updated as “PUBLIC” in the footer	
Command register TCOEFF: All changed to TCOEFFCHN	All
CAN mode updated to CAN mode (also called USE mode).	All
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- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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