

am^{OSRAM} AS5200L

Datasheet

Published by ams-OSRAM AG
Tobelbader Strasse 30,
8141 Premstaetten Austria
Phone +43 3136 500-0
ams-osram.com

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AS5200L 12-bit on-axis magnetic rotary position sensor with redundant I²C and PWM outputs

1 General description

The AS5200L is an easy to program stacked dual die magnetic rotary position sensor with redundant high-resolution 12-bit I²C or PWM outputs. This contactless system measures the absolute angle of a diametric magnetized on-axis magnet. This AS5200L is designed for contactless potentiometer applications and its robust design eliminates the influence of any homogenous external stray magnetic fields.

The industry-standard I²C interface supports simple user programming of non-volatile parameters without requiring a dedicated programmer.

By default the output represents a range from 0 to 360 degrees. It is also possible to define a smaller range to the output by programming a zero angle (start position) and a maximum angle (stop position).

The AS5200L is also equipped with a smart low power mode feature to automatically reduce the power consumption.

AS5200L is designed for automotive applications and is AEC-Q100 grade 1 qualified. To enable safety-critical applications it has two separate sensor die in one MLF-16 (5x5) package with wettable flanks.

1.1 Key benefits & features

The benefits and features of AS5200L are listed below:

Table 1: Added value of using AS5200L

Benefits	Features
Highest reliability and durability	Contactless angle measurement
Simple programming	Simple user-programmable start and stop positions over the I ² C interface
Selectable output	Digital output over I ² C or PWM-encoded output
Low-power consumption	Automatic entry into low-power mode

Benefits	Features
Easy setup	Automatic magnet detection
Small form factor	MLF-16 (5mm x 5mm) package with wettable flanks
Robust environmental tolerance	Wide temperature range: -40°C to 125°C

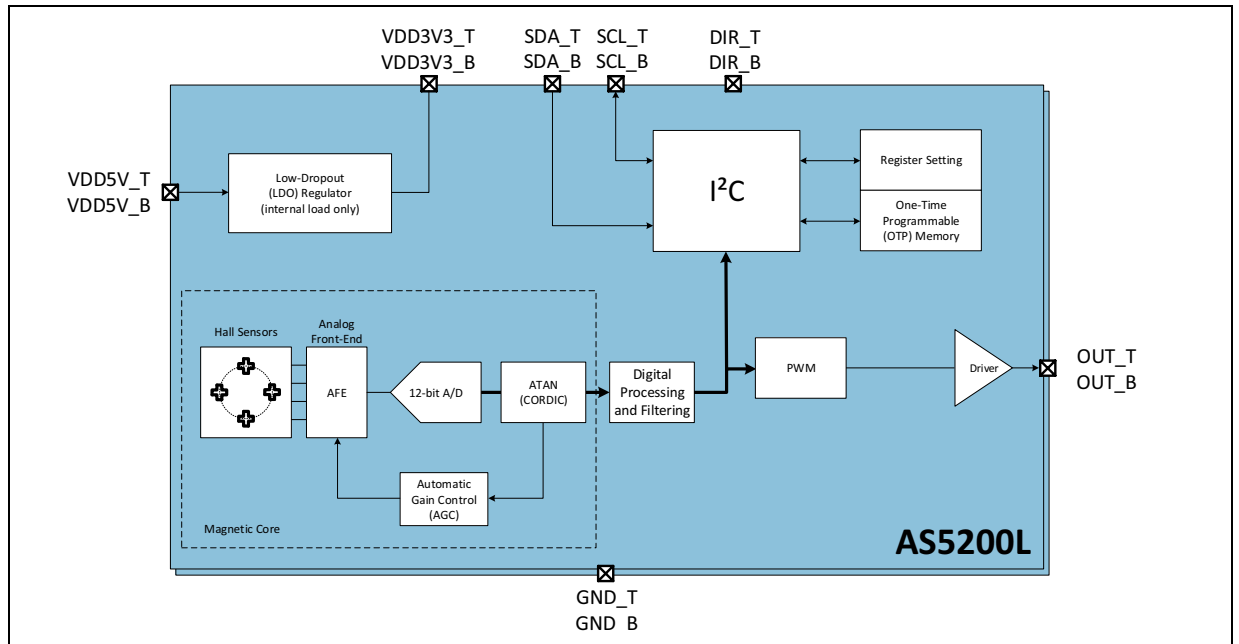
1.2 Applications

The AS5200L is ideally suited for embedded automotive applications where the sensor output is read by a close MCU. The two separate sensor die enable for safety-critical automotive applications like gear-shifters, contactless knobs, pedals, joysticks and other angular position measurement solutions.

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS5200L



2 Ordering information

Ordering code	Package	Marking	Delivery form	Delivery quantity
AS5200L-AMFT	MLF-16	AS5200L	13" Tape & reel in dry pack	5000 pcs/reel
AS5200L-AMFM	MLF-16	AS5200L	7" Tape & reel in dry pack	1000 pcs/reel

3 Pin assignments

3.1 Pin diagram

Device pinout is described below:

Figure 2: MLF-16 pin-out

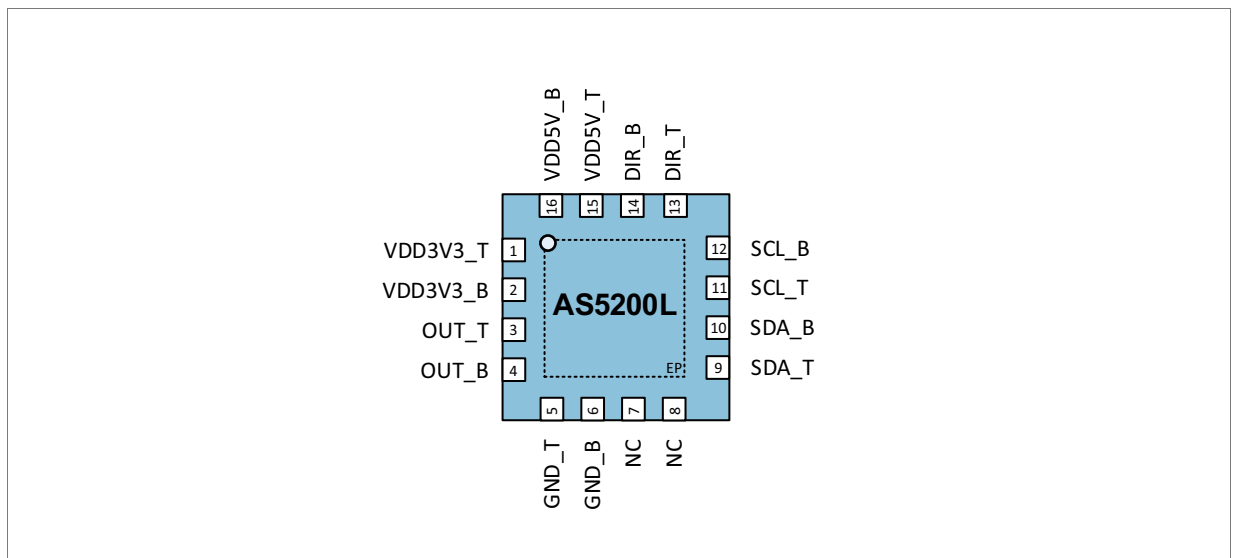


Table 2: Pin description of AS5200L

Pin number	Name ⁽¹⁾	Type	Description
1	VDD3V3_T	Supply	Positive voltage supply in 3.3V mode (requires an external 1 μ F decoupling capacitor in 5V mode)
2	VDD3V3_B		
3	OUT_T	Digital output	PWM output. Fixed to VDD default. Enable in CONF register.
4	OUT_B		
5	GND_T	Supply	Ground
6	GND_B		
7	NC	Digital input, Pull-up	Do not connect
8	NC		
9	SDA_T	Digital input/output	I ² C data (consider external pull-up)
10	SDA_B		
11	SCL_T	Digital input	I ² C clock (consider external pull-up)
12	SCL_B		
13	DIR_T	Digital input	Direction polarity (GND = angle value increases with clockwise rotation, VDD = angle value increases with counterclockwise magnet rotation)
14	DIR_B		
15	VDD5V_T	Supply	Positive voltage supply in 5V mode (requires 100nF decoupling capacitor)
16	VDD5V_B		
	EP	Not connected internally	Do not solder the exposed pad. Remove the exposed pad from PCB land pattern.

(1) Pins with suffix _B belong to bottom die and _T to top die.

4 Absolute maximum ratings

Stresses beyond those listed under Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under these or any other conditions beyond those indicated under Operating conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical parameters					
VDD5V	DC supply voltage at VDD5V pin	-0.3	6.1	V	
VDD3V3	DC supply voltage at VDD3V3 pin	-0.3	4.0	V	
VIO	DC supply voltage at all digital pins	-0.3	VDD+0.3	V	
I _{SCR}	Input current (latch-up immunity)	-100	100	mA	AEC-Q100-004
Continuous power dissipation (T_A = 70°C)					
P _T	Continuous power dissipation		100	mW	
Electrostatic discharge					
ESD _{HBM}	Electrostatic discharge HBM		±2	kV	AEC-Q100-002
Temperature ranges and storage conditions					
T _{STRG}	Storage temperature range	-55	150	°C	
T _{BODY}	Package body temperature		260	°C	ICP/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)
RH _{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level		3		ICP/JEDEC J-STD-033

5 Electrical characteristics

The AS5200L magnetic position sensor integrates two completely separated stacked sensor die. The operation conditions and following descriptions refer to a single sensor die. All limits are guaranteed. The parameters with minimum and maximum values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

5.1 Operating conditions

Table 4: System electrical characteristics and temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD5V	Positive supply voltage in 5.0V mode	5.0V operation mode	4.5	5.0	5.5	V
		During OTP burn procedure ⁽²⁾				
VDD3V3	Positive supply voltage in 3.3V mode	3.3V operation mode	3.0	3.3	3.6	V
		During OTP burn procedure ⁽²⁾				
IDD	Supply current in NOM ⁽¹⁾	PM = 00 Always on			6.4	mA
IDD_LPM1	Supply current in LPM1 ⁽¹⁾	PM = 01 Polling time = 5ms			3.3	mA
IDD_LPM2	Supply current in LPM2 ⁽¹⁾	PM = 10 Polling time = 20ms			1.8	mA
IDD_LPM3	Supply current in LPM3 ⁽¹⁾	PM = 11 Polling time = 100ms			1.5	mA
IDD_BURN	Supply current per bit for burn procedure	Initial peak, 1 μ s			100	mA
		Steady burning, <30 μ s			40	mA
T _A	Operating temperature		-40		125	°C
T _P	Programming temperature		20		30	°C

(1) For typical magnetic field (60mT) excluding current delivered to the external load and tolerance on polling times. Refer CONF register for LPM1, LPM2 and LPM3.

(2) For OTP burn procedure the supply line source resistance should not exceed 10hm.

5.2 Digital inputs and outputs

Table 5: Digital input and output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_IH	High-level input voltage		$0.7 \times V_{DD}$			V
V_IL	Low-level input voltage				$0.3 \times V_{DD}$	V
V_OH	High-level output voltage		$V_{DD} - 0.5$			V
V_OL	Low-level output voltage				0.4	V
I_LKG	Leakage current				± 1	μA

5.3 PWM output

Table 6: PWM output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PWMf1	PWM frequency ⁽¹⁾	PWMF = 00		115		Hz
PWMf2	PWM frequency ⁽¹⁾	PWMF = 01		230		Hz
PWMf3	PWM frequency ⁽¹⁾	PWMF = 10		460		Hz
PWMf4	PWM frequency ⁽¹⁾	PWMF = 11		920		Hz
PWM_DC	PWM duty cycle		2.9		97.1	%
PWM_SR	PWM slew rate	Clload = 1nF	0.5		2	V/ μs
I_O	Output current for PWM output		± 0.5			mA
C_L	Capacitive load for PWM output				1	nF

(1) Frequency is given as typical values, tolerance is $\pm 5\%$

6 Timing characteristics

Table 7: Timing conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_ALPM	Automatic LPM detection time ⁽¹⁾	ALPM = 1		1		min
T_PU	Power-up time				10	ms
F_S	Sampling rate				150	µs
F_AGC	AGC update rate ⁽¹⁾			896		µs
T_SETTL1	Settling time	SF = 00			2.2	ms
T_SETTL2	Settling time	SF = 01			1.1	ms
T_SETTL3	Settling time	SF = 10			0.55	ms
T_SETTL4	Settling time	SF = 11			0.286	ms

(1) Given as typical values, tolerance is ±5%

7 Magnetic characteristics

Table 8: Magnetic characteristics

Symbol	Parameter	Conditions	Min	Max	Units
Bz	Orthogonal magnetic field strength, regular output noise ON_SLOW and ON_FAST	Required orthogonal component of the magnetic field strength measured at the die surface along a circle of 1mm	30	90	mT
Bz_EXT	Magnetic field strength extended range ⁽¹⁾		10	90	mT
Bz_ERROR	Minimum required orthogonal magnetic field strength, Magnet detection level ⁽²⁾			8	mT

(1) The extended range is active if the magnetic field strength is between 10mT and 30mT. Reduced noise performance must be considered for the extended range. Refer to Table 17.

(2) In case the magnetic field is below Bz_ERROR, the MD bit in the STATUS register is set to 0 and if PWM mode is enabled, the output is driven low.

8 System characteristics

Table 9: System specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RES	Resolution			12		bit
INL_BL	System INL	Deviation from best line fit; 360° maximum angle, no magnet displacement, no zero-programming performed (PWM, I ² C)			±1	degree
ON_SLOW	RMS output noise (1 sigma)	Orthogonal component for the magnetic field within the specified range (Bz), after 2.2 ms; SF = 00; 5V operation; for details see Table 17			0.015	degree
ON_FAST	RMS output noise (1 sigma)	Orthogonal component for the magnetic field within the specified range (Bz), after 286 μs, SF=11; 5V operation; for details see Table 17			0.043	degree

9 Detailed description

The AS5200L is a dual-die Hall-based rotary magnetic position sensor using planar sensors that convert the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals coming from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the hardwired CORDIC block (Coordinate Rotation Digital Computer) to compute the angle and magnitude of the magnetic field vector. The intensity of the magnetic field is used by the automatic gain control (AGC) to adjust the amplification level to compensate for temperature and magnetic field variations.

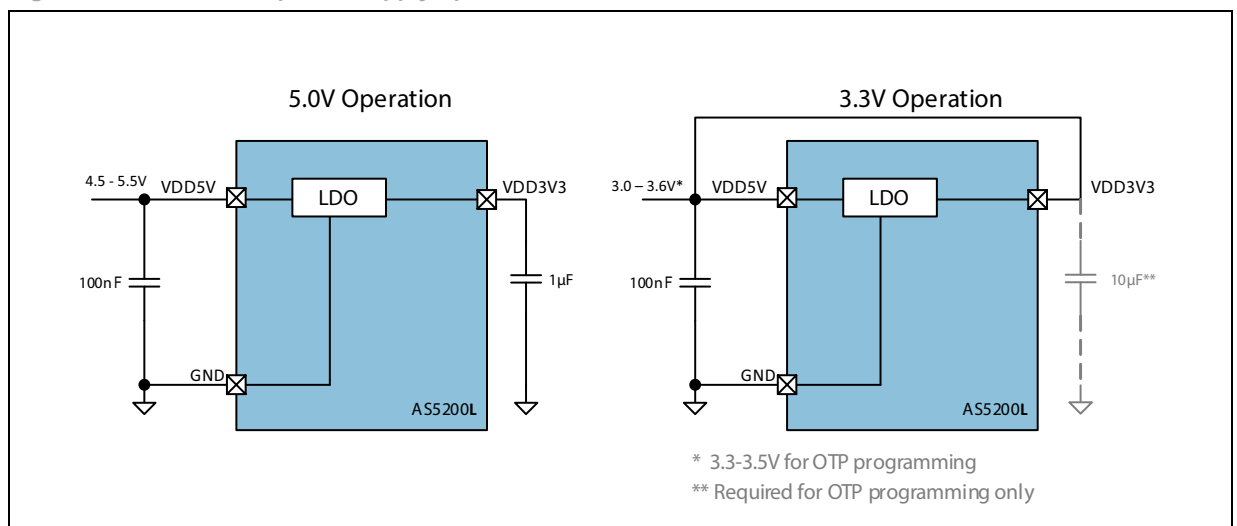
The angle value provided by the CORDIC algorithm is used by the output stage. The user can choose between digital output over I²C and a PWM-encoded digital output.

The AS5200L is programmed through an industry-standard I²C interface to write an on-chip non-volatile memory. This interface can be used to program a zero angle (start position) and a maximum angle (stop position) which maps the full resolution of the output to a subset of the entire 0 to 360 degree range.

9.1 IC power management

The AS5200L can be powered from a 5.0V supply using the on-chip LDO regulator, or it can be powered directly from a 3.3V supply. The internal LDO is not intended to power other external ICs and needs a 1 μ F capacitor to ground, as shown in Figure 3 for one sensor die. The second die requires a separate capacitor as shown in Figure 13. In 3.3V operation, the VDD5V and VDD3V3 pins must be tied together. VDD is the voltage level present at the VDD5V pin.

Figure 3: 5.0V and 3.3V power supply options



9.2 I²C interface

The AS5200L supports the 2-wire Fast-mode Plus I²C-slave protocol in device mode, in compliance with the NXP Semiconductors (formerly Philips Semiconductors) specification UM10204. A device that sends data onto the bus is a transmitter and a device receiving data is a receiver. The device that controls the message is called a master. The devices that are controlled by the master are called slaves. A master device generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions that control the bus. The AS5200L always operates as a slave on the I²C bus. Connections to the bus are made through the open-drain I/O lines SDA and the input SCL. Clock stretching is not included.

The host MCU (master) initiates data transfers. The 7-bit slave addresses of the AS5200L are 40h (1000000 in binary) for the bottom die and 41h (1000001 in binary) for the top die.

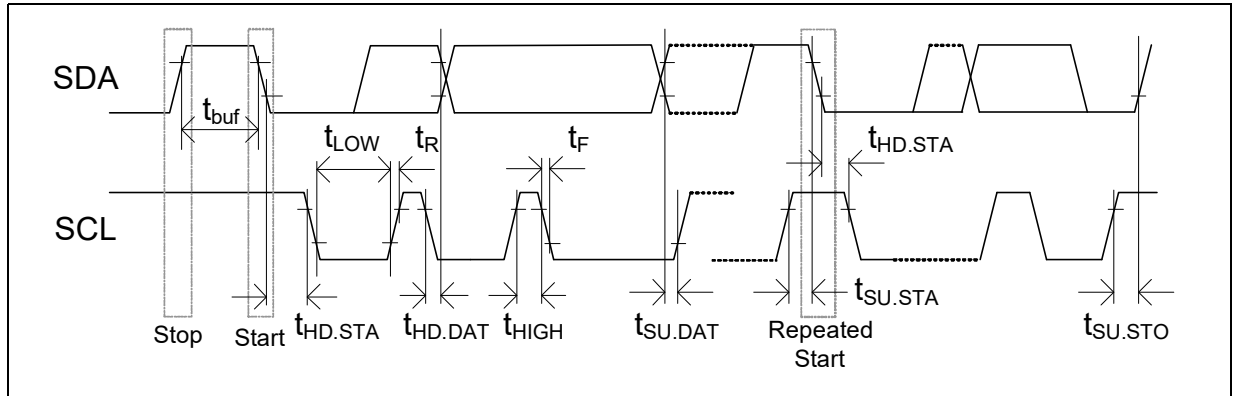
9.2.1 Supported modes

- Random/Sequential read
- Byte/Page write
- Automatic increment (ANGLE register)
- Standard-mode
- Fast-mode
- Fast-mode Plus

The SDA signal is the bidirectional data line. The SCL signal is the clock generated by the I²C bus master to synchronize sampling data from SDA. The maximum SCL frequency is 1 MHz. Data is sampled on the rising edge of SCL.

9.3 I²C interface operation

Figure 4: I²C timing diagram



9.3.1 I²C electrical specification

Table 10: I²C electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Logic low input voltage		-0.3		0.3 x VDD	V
VIH	Logic high input voltage		0.7 x VDD		VDD + 0.3	V
VHYS	Hysteresis of schmitt trigger inputs	VDD > 2.5V	0.05 x VDD			V
VOL	Logic low output voltage (open-drain or open-collector) at 3 mA sink current	VDD > 2.5V			0.4	V
IOL	Logic low output current	VOL = 0.4V	20			mA
t _{OF}	Output fall time from VIHmax to VILmax		10		120 ⁽¹⁾	ns
t _{SP}	Pulse width of spikes that must be suppressed by the input filter				50 ⁽²⁾	ns
I _I	Input current at each I/O pin	Input voltage between 0.1 x VDD and 0.9 x VDD	-10		+10 ⁽³⁾	μA
C _B	Total capacitive load for each bus line				550	pF
C _{I/O}	I/O capacitance (SDA, SCL) ⁽⁴⁾				10	pF

- (1) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used this has to be considered for bus timing.
- (2) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
- (3) I/O pins of Fast-mode and Fast-mode Plus devices must not load or drive the SDA and SCL lines if VDD is switched OFF.
- (4) Special-purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

9.3.2 I²C timing

Table 11: I²C timing

Symbol	Parameter	Min	Max	Unit
f _{SCLK}	SCL clock frequency		1.0	MHz
t _{BUF}	Bus free time (time between the STOP and START conditions)	0.5		μs
t _{HD;STA}	Hold time; (Repeated) START condition ⁽¹⁾	0.26		μs
t _{LOW}	Low phase of SCL clock	0.5		μs
t _{HIGH}	High phase of SCL clock	0.26		μs
t _{SU;STA}	Setup time for a Repeated START condition	0.26		μs
t _{HD;DAT}	Data hold time ⁽²⁾		0.45	μs
t _{SU;DAT}	Data setup time ⁽³⁾	50		ns
t _R	Rise time of SDA and SCL signals		120	ns
t _F	Fall time of SDA and SCL signals	10	120 ⁽⁴⁾	ns
t _{SU;STO}	Setup time for STOP condition	0.26		μs

- (1) After this time, the first clock is generated.
- (2) A device must internally provide a minimum hold time of 120 ns (Fast-mode Plus) for the SDA signal (referred to the V_{IHmin} of SCL) to bridge the undefined region of the falling edge of SCL.
- (3) A Fast-mode device can be used in a standard-mode system, but the requirement t_{SU;DAT} = 250 ns must be met. This is automatically if the device does not stretch the low phase of SCL. If such a device does stretch the low phase of SCL, it must drive the next data bit on SDA (t_{Rmax} + t_{SU;DAT} = 1000 + 250 = 1250 ns) before SCL is released.
- (4) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, this has to be considered for bus timing.

9.4 I²C modes

9.4.1 Invalid addresses

There are two addresses used to access an AS5200L register. The first is the slave address used to select the AS5200L. All I²C bus transactions include a slave address. The slave address of the AS5200L are 40h (1000000 in binary) for the bottom die and 41h (1000001 in binary) for the top die. The second address is a word address sent in the first byte transferred in a write transaction. The word address selects a register on the AS5200L. The word address is loaded into the address pointer on the AS5200L. During subsequent read transactions and subsequent bytes in the write transaction, the address pointer provides the address of the selected register. The address pointer is incremented after each byte is transferred, except for certain read transactions to special registers.

If the user sets the address pointer to an invalid word address, the address byte is not acknowledged (the A bit is high). Nevertheless, a read or write cycle is possible. The address pointer is increased after each byte.

9.4.2 Reading

When reading from an invalid address, the AS5200L returns all zeros in the data bytes. The address pointer is incremented after each byte. Sequential reads over the whole address range are possible including address overflow.

9.4.3 Automatic increment of the address pointer for ANGLE, RAW ANGLE and MAGNITUDE registers

These are special registers which suppress the automatic increment of the address pointer on reads, so a re-read of these registers requires no I²C write command to reload the address pointer. This special treatment of the pointer is effective only if the address pointer is set to the high byte.

9.4.4 Writing

A write to an invalid address is not acknowledged by the AS5200L, although the address pointer is incremented. When the address pointer points to a valid address again, a successful write accessed is acknowledged. Page write over the whole address range is possible including address overflow.

9.4.5 Supported bus protocol

Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever SCL is high. Changes in the data line while SCL is high are interpreted as START or STOP conditions.

Accordingly, the following bus conditions have been defined:

Bus not busy

Both SDA and SCL remain high.

Start data transfer

A change in the state of SDA from high to low while SCL is high defines the START condition.

Stop data transfer

A change in the state of SDA from low to high while SCL is high defines the STOP condition.

Data valid

The state of the data line represents valid data when, after a START condition, SDA is stable for the duration of the high phase of SCL. The data on SDA must be changed during the low phase of SCL. There is one clock period per bit of data.

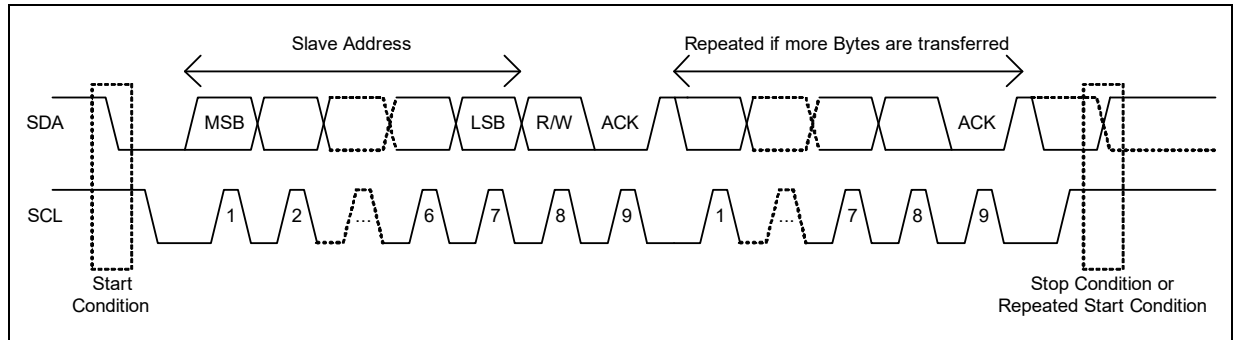
Each I²C bus transaction is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the I²C bus master. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each I²C slave device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The I²C bus master device must generate an extra clock period for this acknowledge bit.

A slave that acknowledges must pull down SDA during the acknowledge clock period in such a way that SDA is stable low during the high phase of the acknowledge clock period. Of course, setup and hold times must be taken into account. A master must signal an end of a read transaction by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave SDA high to enable the master to generate the STOP condition.

Figure 5: Data read



Depending on the state of the R/W bit, two types of data transfer are possible:

9.4.6 Data transfer from a master transmitter to a slave receiver

The first byte transmitted by the master is the slave address, followed by R/W = 0. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. If the slave does not understand the command or data it sends a not acknowledge (NACK). Data is transferred with the most significant bit (MSB) first.

9.4.7 Data transfer from a slave transmitter to a master receiver

The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a NACK is returned. The master generates all of the SCL clock periods and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Because a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

9.4.8 AS5200L slave modes

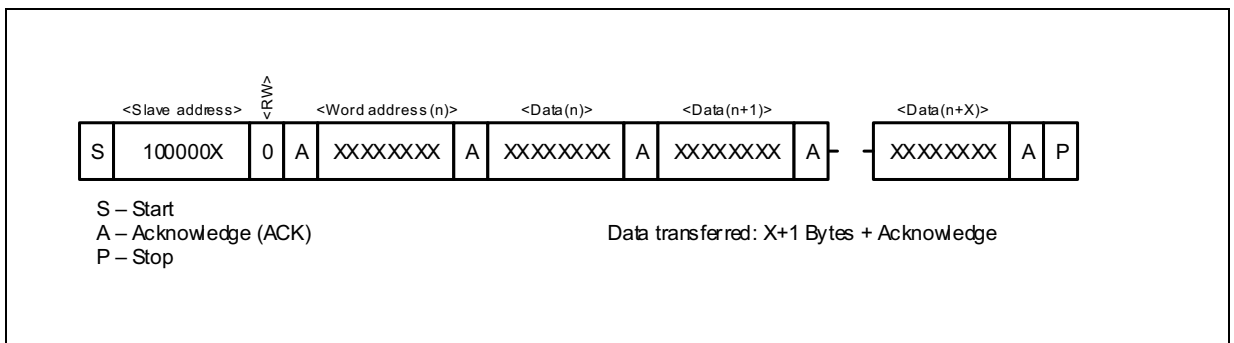
Slave receiver mode (Write Mode)

Serial data and clock are received through SDA and SCL. Each byte is followed by an acknowledge bit or by a not acknowledge depending on whether the address-pointer selects a valid address. START and STOP conditions are recognized as the beginning and end of a bus transaction. The slave address byte is the first byte received after the START condition.

The 7-bit slave address is followed by the direction bit (R/W), which, for a write, is 0 (low). After receiving and decoding the slave address byte the slave device drives an acknowledge on SDA. After the AS5200L acknowledges the slave address and write bit, the master transmits a register address (word address) to the AS5200L. This is loaded into the address pointer on the AS5200L. If the address is a valid readable address, the AS5200L answers by sending an

acknowledge (A bit low). If the address pointer selects an invalid address, a not acknowledge is sent (A bit high). The master may then transmit zero or more bytes of data. If the address pointer selects an invalid address, the received data are not stored. The address pointer will increment after each byte transferred whether or not the address is valid. If the address-pointer reaches a valid position again, the AS5200L answers with an acknowledge and stores the data. The master generates a STOP condition to terminate the write transaction.

Figure 6: Data write (Slave Receiver Mode)



Slave transmitter mode (Read Mode)

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the AS5200L will drive data on SDA. START and STOP conditions are recognized as the beginning and end of a bus transaction. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit AS5200L address. The 7-bit slave address is followed by the direction bit (R/W), which, for a read, is 1 (high). After receiving and decoding the slave address byte, the slave device drives an acknowledge on the SDA line. The AS5200L then begins to transmit data starting with the register address pointed to by the address pointer. If the address pointer is not written before the initiation of a read transaction, the first address that is read is the last one stored in the address pointer. The AS5200L must receive a not acknowledge (NACK) to end a read transaction.

Figure 7: Data read (Slave Transmitter Mode)

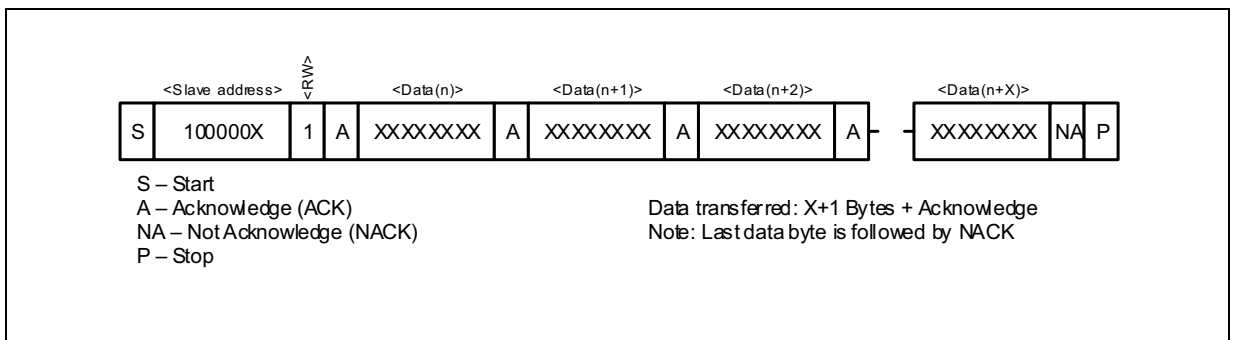
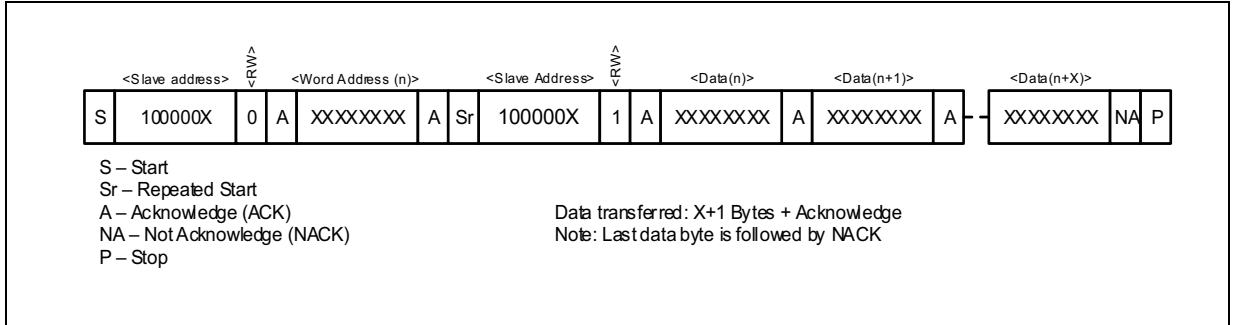


Figure 8: Data read with address pointer reload (Slave Transmitter Mode)



9.4.9 SDA and SCL input filters

Input filters for SDA and SCL inputs are included to suppress noise spikes of less than 50 ns.

10 Register description

The following registers are accessible over the serial I²C interface. The 7-bit device address of the slaves are 40h (1000000 in binary) for the bottom die and 41h (1000001 in binary) for the top die. To permanently program a configuration, a non-volatile memory (OTP) is provided.

Table 12: Register map

Address	Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration registers⁽¹⁾⁽²⁾										
0x01	ZPOS	R/W/P						ZPOS(11:8)		
0x02			ZPOS(7:0)							
0x03	MPOS	R/W/P						MPOS(11:8)		
0x04			MPOS(7:0)							
0x07	CONF	R/W/P			ALPM		FTH(2:0)		SF(1:0)	
0x08			PWMF(1:0)	OUTS(1:0)	HYST(1:0)	PM(1:0)				
Output registers										
0x0C	RAW ANGLE	R	RAWFF	SFBUSY				RAW ANGLE(11:8)		
0x0D		R	RAW ANGLE(7:0)							
0x0E	ANGLE	R					ANGLE(11:8)			
0x0F		R	ANGLE(7:0)							
Status registers										
0x0B	STATUS	R		ADCOF	MD	ML	MH	AGCF	OCF1	OCF0
0x1A	AGC	R	AGC(7:0)							
0x1B	MAGNITUDE	R					MAGNITUDE (11:8)			
0x1C		R	MAGNITUDE(7:0)							
Burn commands										
0xFF	BURN	W	Burn_Angle = 0x80; Burn_Setting = 0x40							

- (1) To change a configuration, read out the register, modify only the desired bits and write the new configuration. Blank fields may contain factory settings.
- (2) During power-up, configuration registers are reset to the permanently programmed value. Not programmed bits are zero.

10.1 ZPOS/MPOS registers

These registers are used to configure the start position (ZPOS) and a stop position (MPOS) for a narrower angular range. The angular range must be greater than 18 degrees. In case of narrowed angular range, the resolution is not scaled to narrowed range (e.g. 0°-360°(full-turn) → 4096dec; 0°-180° → 2048dec).

To configure the angular range, see Angle programming.

10.2 CONF register

The CONF register supports customizing the AS5200L. Table 13 shows the mapping of the CONF register.

Table 13: CONF register

Name	Bit position	Description
PM(1:0)	1:0	Power mode 00 = NOM, 01 = LPM1, 10 = LPM2, 11 = LPM3
HYST(1:0)	3:2	Hysteresis 00 = OFF, 01 = 1 LSB, 10 = 2 LSBs, 11 = 3 LSBs
OUTS(1:0)	5:4	Output stage 00 = OUT set to VDD, 01 = OUT set to VDD, 10 = digital PWM
PWMF(1:0)	7:6	PWM frequency 00 = 115 Hz; 01 = 230 Hz; 10 = 460 Hz; 11 = 920 Hz
SF(1:0)	9:8	Slow filter 00 = 16x [*] ; 01 = 8x; 10 = 4x; 11 = 2x
FTH(2:0)	12:10	Fast filter threshold 000 = slow filter only, 001 = 6 LSBs, 010 = 7 LSBs, 011 = 9 LSBs, 100 = 18 LSBs, 101 = 21 LSBs, 110 = 24 LSBs, 111 = 10 LSBs
ALPM	13	Automatic low power mode timer 0 = OFF, 1 = ON

(1) Forced in Low Power Mode (LPM)

10.3 ANGLE/RAW ANGLE register

The RAW ANGLE register contains the unscaled and unmodified angle. The scaled output value is available in the ANGLE register.

The ANGLE register has a 10-LSB hysteresis at the limit of the 360 degree range to avoid discontinuity points or toggling of the output within one rotation.

Table 14: RAW ANGLE register

Name	Bit position	Description
RAW ANGLE	11:0	Raw angle value
SFBUSY	14	Slow Filter is busy
RAWFF	15	RAW ANGLE comes from Fast Filter

10.4 STATUS register

The STATUS register provides bits that indicate the current state of the AS5200L.

Table 15: STATUS register

Bit	Name	State when bit is high
0	OCF0	Offset compensation loop 0 finished
1	OCF1	Offset compensation loop 1 finished
2	AGCF	AGC loop finished
3	MH	AGC minimum gain overflow, magnet too strong
4	ML	AGC maximum gain overflow, magnet too weak
5	MD	Magnet was detected
6	ADCOF ⁽¹⁾	ADC or CORDIC overflow

(1) ADCOF is a sticky bit and remains active once an overflow has occurred. The bit is reset by writing 00h into the register.

10.5 AGC register

The AS5200L uses Automatic Gain Control in a closed loop to compensate for variations of the magnetic field strength due to changes of temperature, airgap between IC and magnet, and magnet degradation. The AGC register indicates the gain. For the most robust performance, the gain value should be in the center of its range. The airgap of the physical system can be adjusted to achieve this value. In 5V operation, the AGC range is 0-255 counts. The AGC range is reduced to 0-127 counts in 3.3V mode.

10.6 MAGNITUDE register

The MAGNITUDE register indicates the magnitude value of the internal CORDIC.

10.6.1 Non-volatile memory (OTP)

The non-volatile memory is used to permanently program the configuration. To program the non-volatile memory, the I²C interface is used. The programming can be either performed in the 5V supply mode or in the 3.3V operation mode but using a minimum supply voltage of 3.3V and a 10 µF capacitor at the VDD3V3 pin to ground. This 10 µF capacitor is needed only during the programming of the device. Two different commands are used to permanently program the device:

10.6.2 Burn_Angle command (ZPOS, MPOS)

The host microcontroller can perform a permanent programming of ZPOS and MPOS with a BURN_ANGLE command. To perform a BURN_ANGLE command, write the value 0x80 into register 0xFF. The BURN_ANGLE command can be executed only two times.

This command will only be executed if the presence of the magnet is detected (MD = 1).

10.6.3 Burn_Setting command (CONFIG)

The host microcontroller can perform a permanent writing of CONFIG with a BURN_SETTING command. Once a bit in those registers is permanently written to 1, it stays on 1 and cannot be changed to 0 anymore. A bit which is 0 can be programmed to 1.

To perform a BURN_SETTING command, write the value 0x40 into register 0xFF.

10.7 Angle programming

For applications which do not use the full 0 to 360 degree angular range. The angular range must be greater than 18 degrees. In case of narrowed angular range, the resolution is not scaled to narrowed range (e.g. 0°-360°(full-turn) → 4096dec; 0°-180° → 2048dec).

The range is specified by programming a start position (ZPOS) and either a stop position (MPOS).

The recommended method for programming the angular range is:

Table 16: Angle programming through the I²C interface

Use the correct hardware configuration shown in Figure 13.	
Step 1	Power up the AS5200L.
Step 2	Turn the magnet to the start position.
Step 3	Read the RAW ANGLE register. Write the RAW ANGLE value into the ZPOS register. Wait at least 1 ms.
Step 4	Rotate the magnet in the direction defined by the level on the DIR pin (GND for clockwise, VDD for counterclockwise) to the stop position. The amount of rotation must be greater than 18 degrees.
Step 5	Read the RAW ANGLE register. Write the RAW ANGLE value into the MPOS register. Wait at least 1 ms.
Proceed with Step 6 to permanently program the configuration.	
Step 6	Perform a BURN_ANGLE command to permanently program the device. Wait at least 1 ms.
Step 7	Verify the BURN_ANGLE command: Write the commands 0x01, 0x11 and 0x10 sequentially into the register 0xFF to load the actual OTP content. Read the ZPOS and MPOS registers to verify that the BURN_ANGLE command was successful.
Step 8	Read and verify the ZPOS and MPOS registers again after a new power-up cycle.

- (1) After each register command, the new setting is effective at the output at least 1 ms later.
- (2) It is highly recommended to perform a functional test after this procedure.

10.8 Output stage

Without regard to the PWM output, an external unit can read the angle from the ANGLE register through I²C interface at any time. The output stage is fixed to VDD default. To enable the PWM output configure the OUTS bits in the CONF register.

10.9 PWM output mode

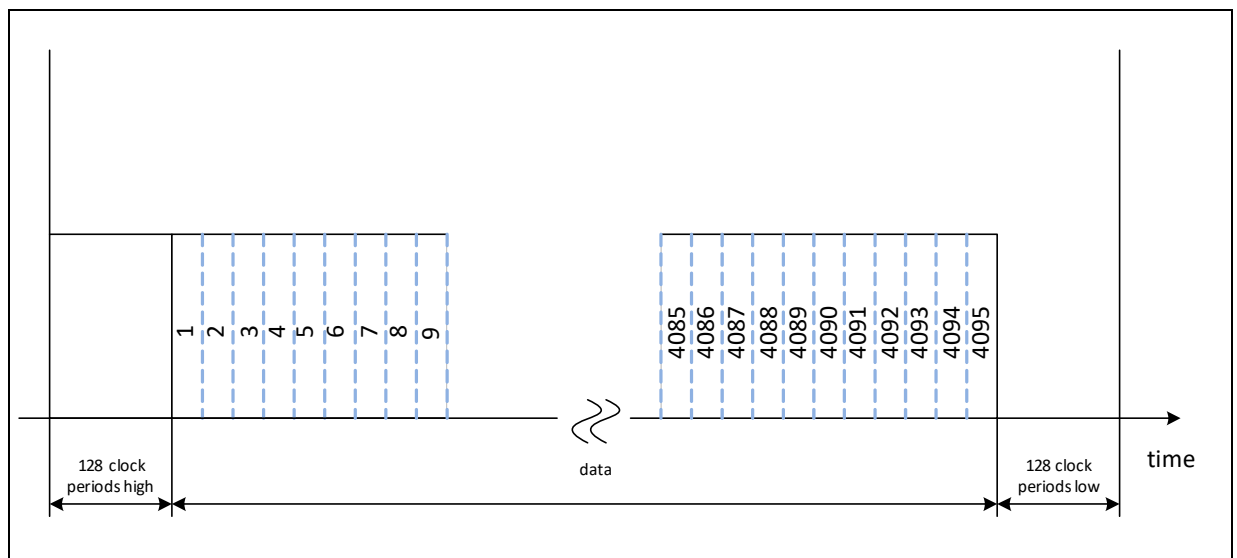
The OUT pin provides a digital PWM signal. The duty cycle of each pulse is proportional to the absolute angle of the rotating magnet.

The PWM signal consists of a frame of 4351 PWM clock periods as shown in Figure 9. This PWM frame is composed of the following sections:

- 128 PWM clock periods high
- 4095 PWM clock periods data
- 128 PWM clock periods low

The angle is represented in the data part of the frame, and one PWM clock period represents one 4096th of the full angular range. The PWM frequency is programmed with the PWMF bits in the CONF register.

Figure 9: Output characteristics in pulse width modulation mode



An angle of zero degrees is represented by 128 clock periods high and 4223 clock periods low, while a maximum angle consists of 4223 clock periods high and 128 clock periods low.

10.10 Step response and filter settings

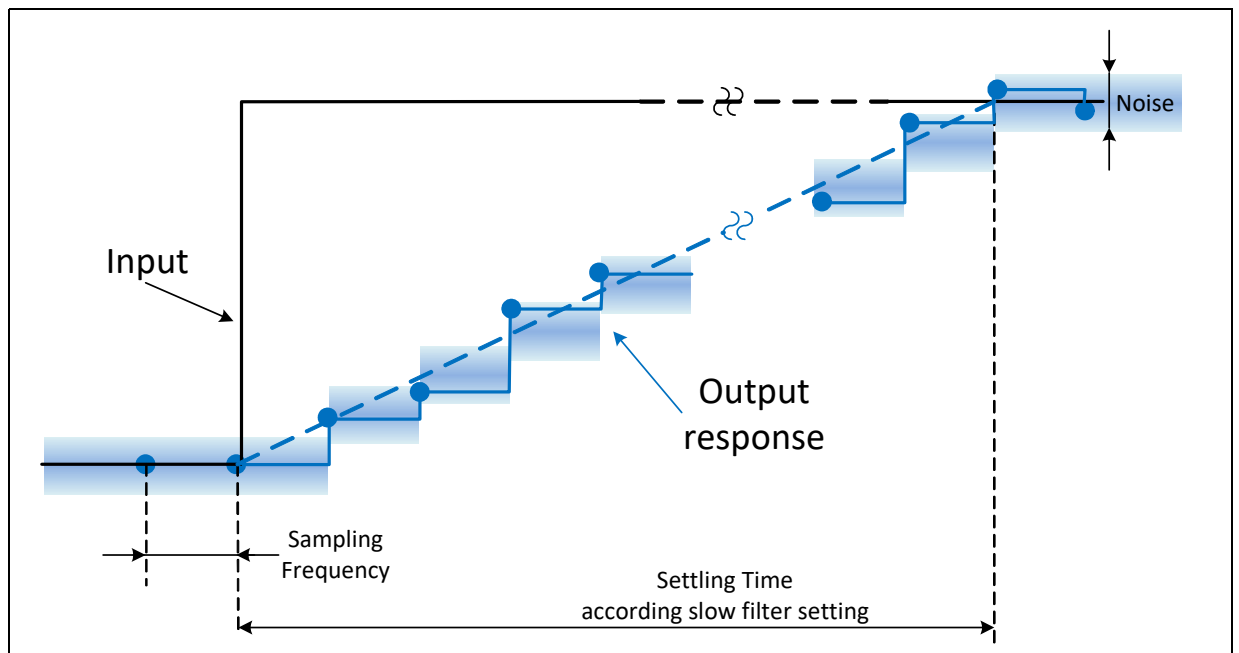
The AS5200L has a digital post-processing programmable filter which can be set in fast or slow modes. The fast filter mode can be enabled by setting a fast filter threshold in the FTH(2:0) bits of the CONF register.

If the fast filter is OFF, the step output response is controlled by the slow linear filter. The step response of the slow filter is programmable with the SF(1:0) bits in the CONF register. Figure 10 shows the tradeoff between delay and noise for the different SF bit settings.

Table 17: Step response delay vs. noise band

SF	Step response delay (ms)	Max. RMS output noise [1 Sigma] (Degree)	
		For normal magnetic range Bz	For extended magnetic range Bz_EXT
		5V	5V
00	2.2	0.015	0.060
01	1.1	0.021	0.085
10	0.55	0.030	0.120
11	0.286	0.043	0.170

Figure 10: Step response (fast filter OFF)

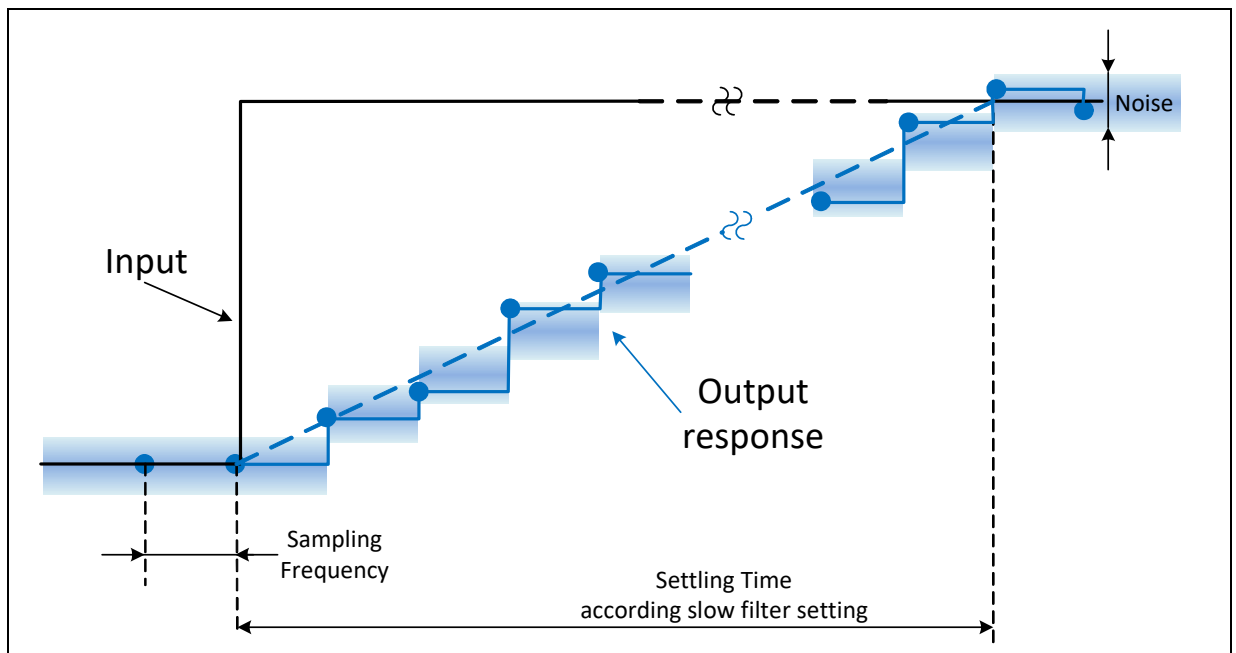


For a fast step response and low noise after settling, the fast filter can be enabled. The fast filter works only if the input variation is greater than the fast filter threshold, otherwise the output response is determined only by the slow filter. The fast filter threshold is programmed with the FTH(2:0) bits in the CONF register. As shown in Figure 11, the step response stays within an error band after two full sampling periods to settle to the final value determined by the slow filter.

Table 18: Fast filter threshold

FTH	Fast filter threshold (LSB)	
	Slow-to-fast filter	Fast-to-slow filter
000	Slow filter only	
001	6	1
010	7	1
011	9	1
100	18	2
101	21	2
110	24	2
111	10	4

Figure 11: Step response (fast filter ON)



10.11 Hysteresis

To avoid any toggling of the output when the magnet is not moving, a 1 to 3 LSB hysteresis of the 12-bit resolution can be enabled with the HYST(1:0) bits in the CONF register.

10.12 Magnet detection

As a safety and diagnostic feature, the AS5200L indicates the absence of the magnet. If the measured magnet field strength goes below the minimum specified level (Bz_ERROR), the MD bit in the STATUS register is set to 0 and if PWM mode is enabled, the output is driven low.

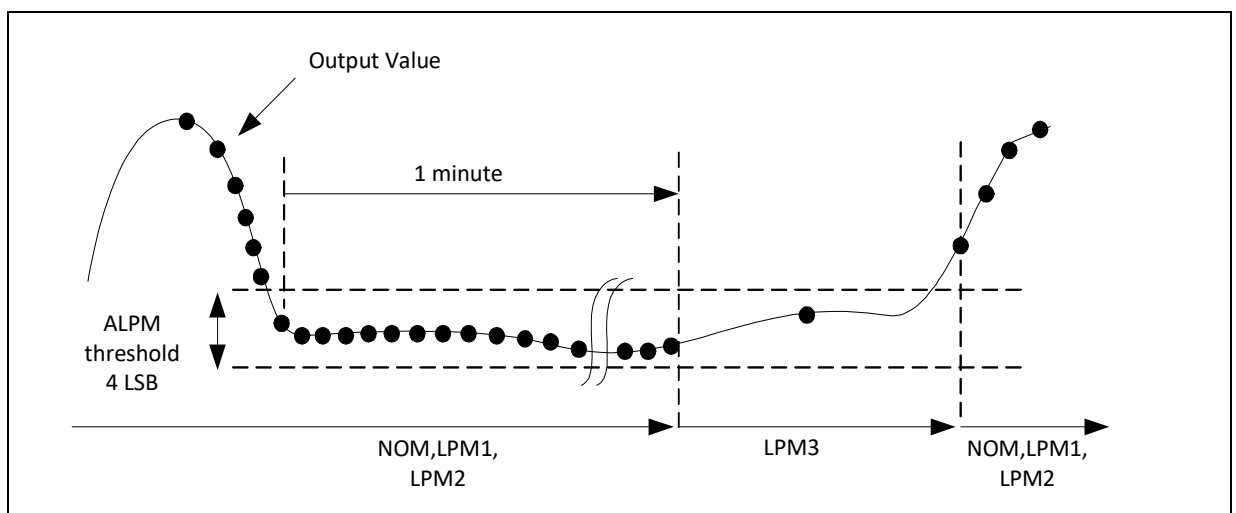
10.13 Low power modes

A digital state machine automatically manages the low power modes to reduce the average current consumption. Three low power modes are available and can be enabled with the PM(1:0) bits in the CONF register. Current consumption and polling times are shown in Table 4.

10.14 Automatic low power mode timer

The automatic LPM timer allows saving power by switching into LPM3 if the angle stays within the automatic LPM threshold of 4 LSB for at least one minute, as shown in Figure 12. The automatic LPM function can be enabled with the ALPM bit in the CONF register.

Figure 12: Automatic LPM timer function



11 Application information

11.1 Schematic

All required external components are shown below for the reference application diagram. To improve EMC and for remote applications, consider additional protection circuitry.

Figure 13: Application diagram for angle readout and programming with I²C

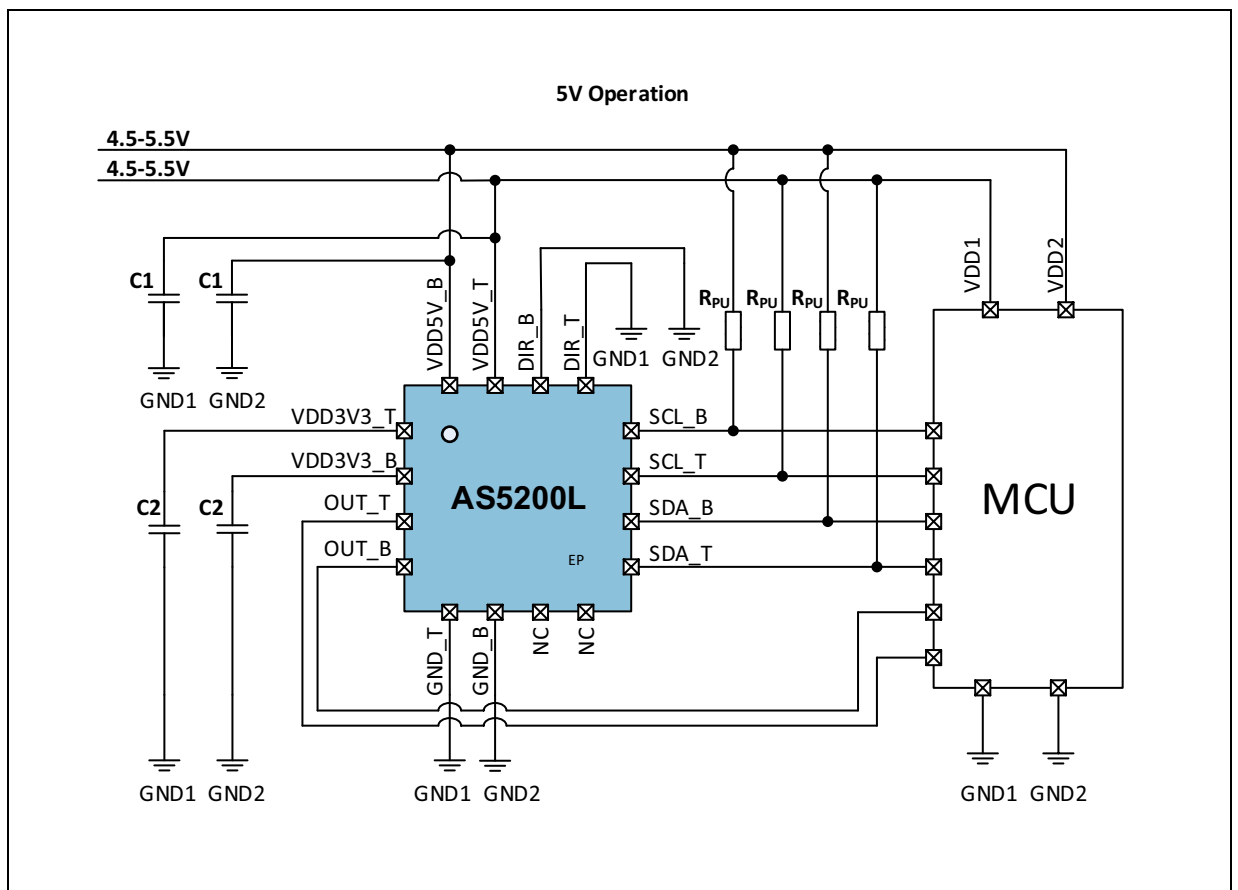


Table 19: Recommended external components

Component	Symbol	Value	Units	Notes
VDD5V buffer capacitor	C1	100	nF	20%
LDO regulator capacitor	C2	1	μ F	20%; < 100 m Ω ; Low ESR ceramic capacitor
Optional pull-up for I ² C bus	RPU	4.7	K Ω	Refer to UM10204 for RPU sizing

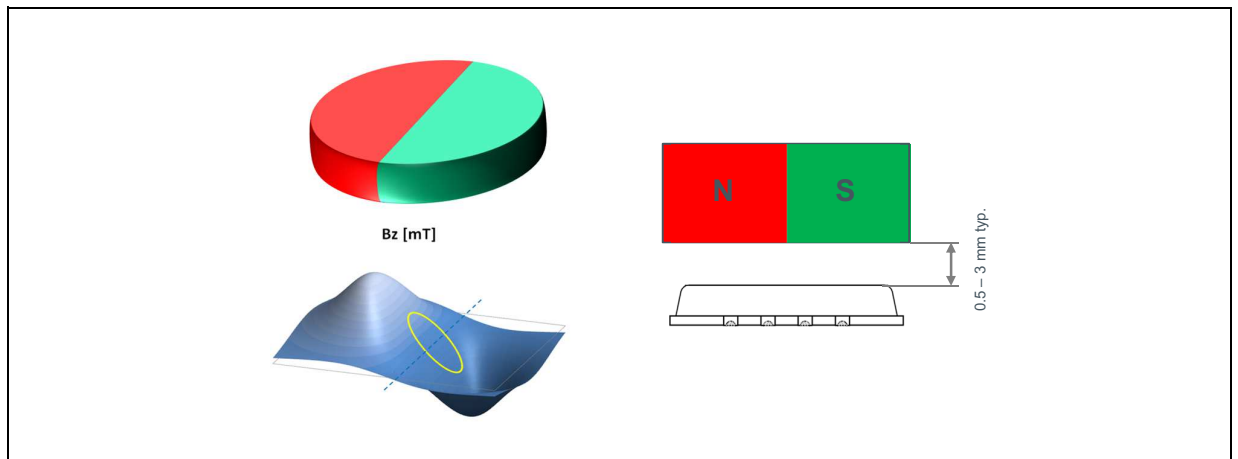
(1) To be fulfilled over temperature and lifetime

11.2 Magnetic requirements

The AS5200L requires the magnetic field component B_z perpendicular to the sensitive area on the chip.

Along the circumference of the Hall element circle the magnetic field B_z should be sine-shaped. The magnetic field gradient of B_z along the radius of the circle should be in the linear range of the magnet to eliminate displacement error by the differential measurement principle.

Figure 14: Magnetic field B_z and typical airgap

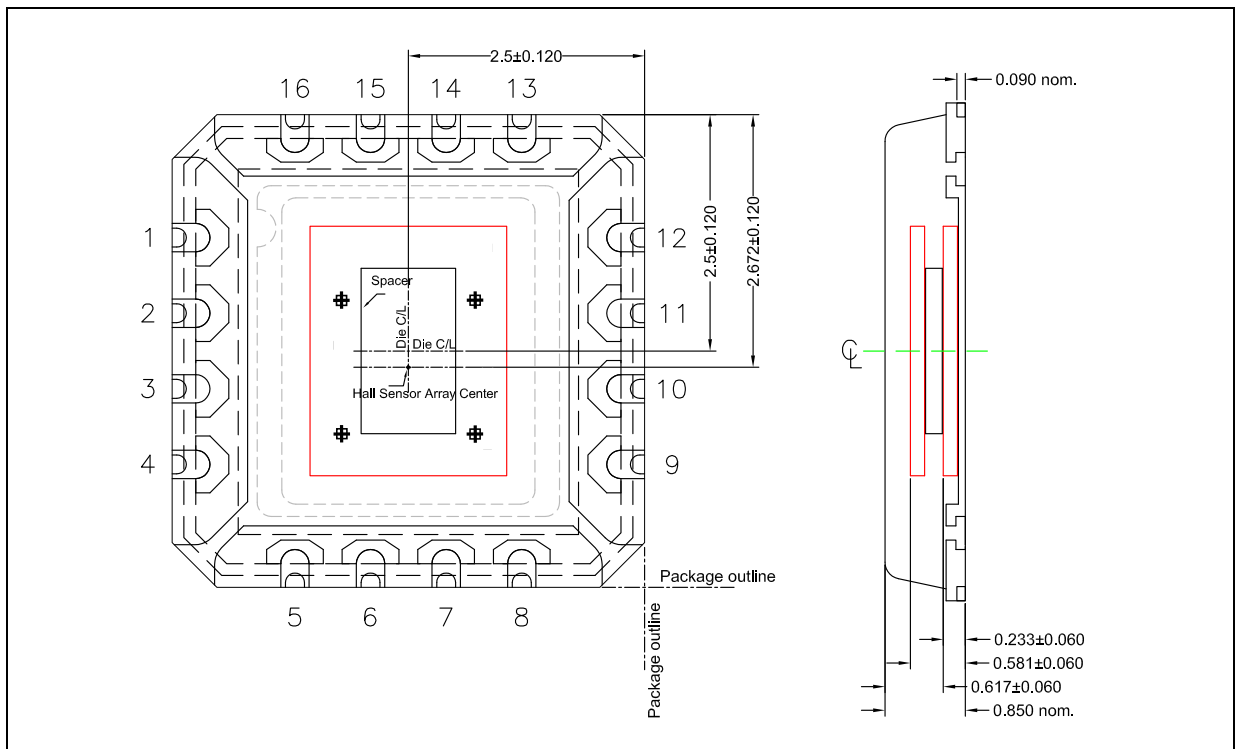


The typical airgap is between 0.5 mm and 3 mm, and it depends on the selected magnet. A larger and stronger magnet allows a larger airgap. Using the AGC value as a guide, the optimal airgap can be found by adjusting the distance between the magnet and the AS5200L so that the AGC value is in the center of its range. The maximum allowed displacement of the rotational axis of the reference magnet from the center of the package is 0.25 mm when using a magnet with a diameter of 6mm.

11.3 Mechanical data

The internal Hall elements are placed on a radius of 1 mm. The center of the internal hall array is NOT in the center of the package as shown below in Figure 15. The center of the magnet must be placed over the center of the Hall sensor array.

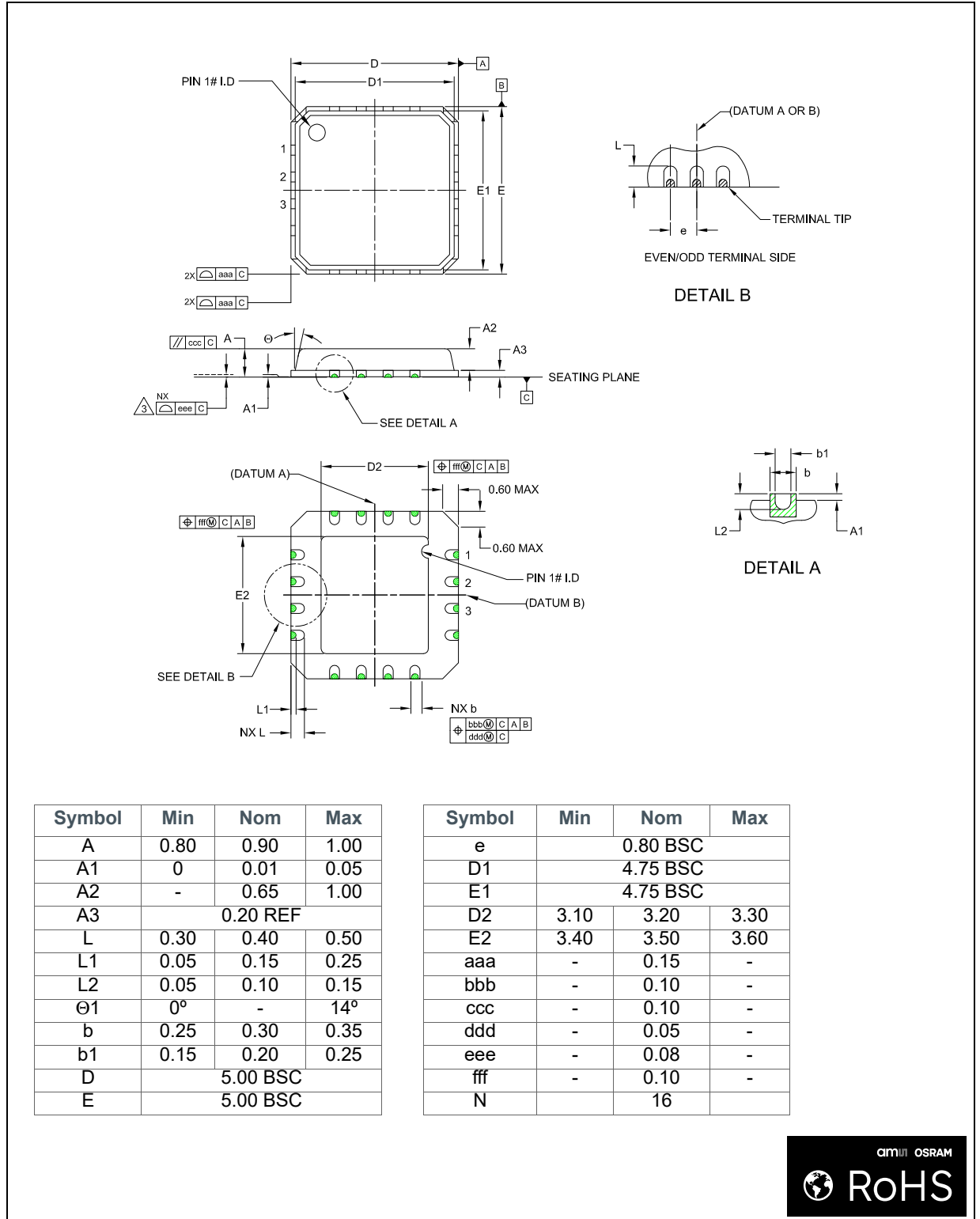
Figure 15: Hall element positions



- (1) All dimensions in mm.
- (2) Die thickness 150mm nom.
- (3) Adhesive thickness 12mm nom.
- (4) Spacer thickness: 178mm typ.

12 Package drawings & markings

Figure 16: MLF-16 package outline drawing



- (1) Dimensioning & tolerancing conform to ASME Y14.5M-1994.
- (2) All dimensions are in millimeters. Angles are in degrees.
- (3) N is the total number of terminals.
- (4) DATUMS A & B to be determined at DATUM H.
- (5) Do not solder the exposed pad. Remove the exposed pad from PCB land pattern.

Figure 17: Package marking

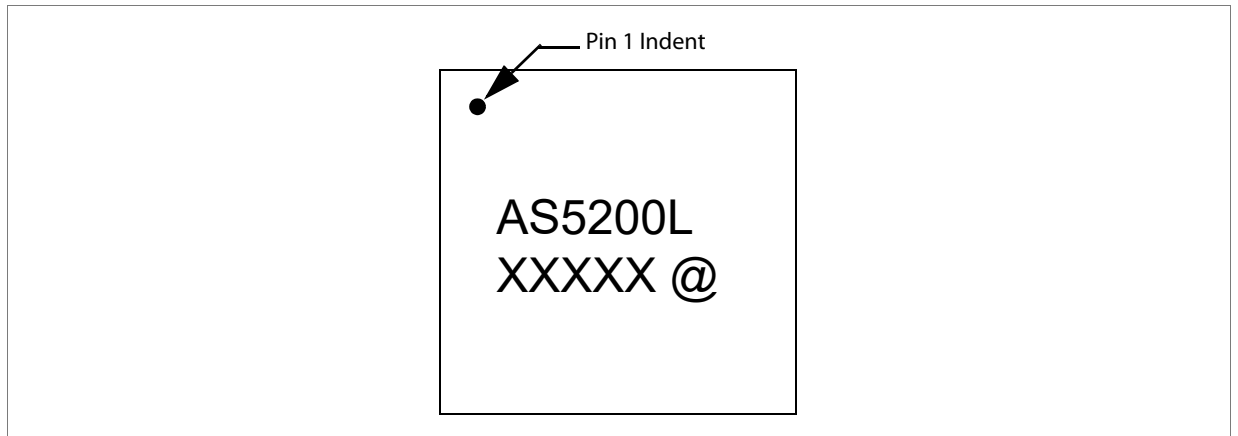


Table 20: Packaging code

XXXXX	@
Tracecode	Sublot identifier

13 Revision information

Document status	Product status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous released version to current revision v2-00	Page
Updated description under "AGC register"	27

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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Headquarters

ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

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