Product Document

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User Guide

UG001016

AS7050

Evaluation Kit

User Manual

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Content Guide

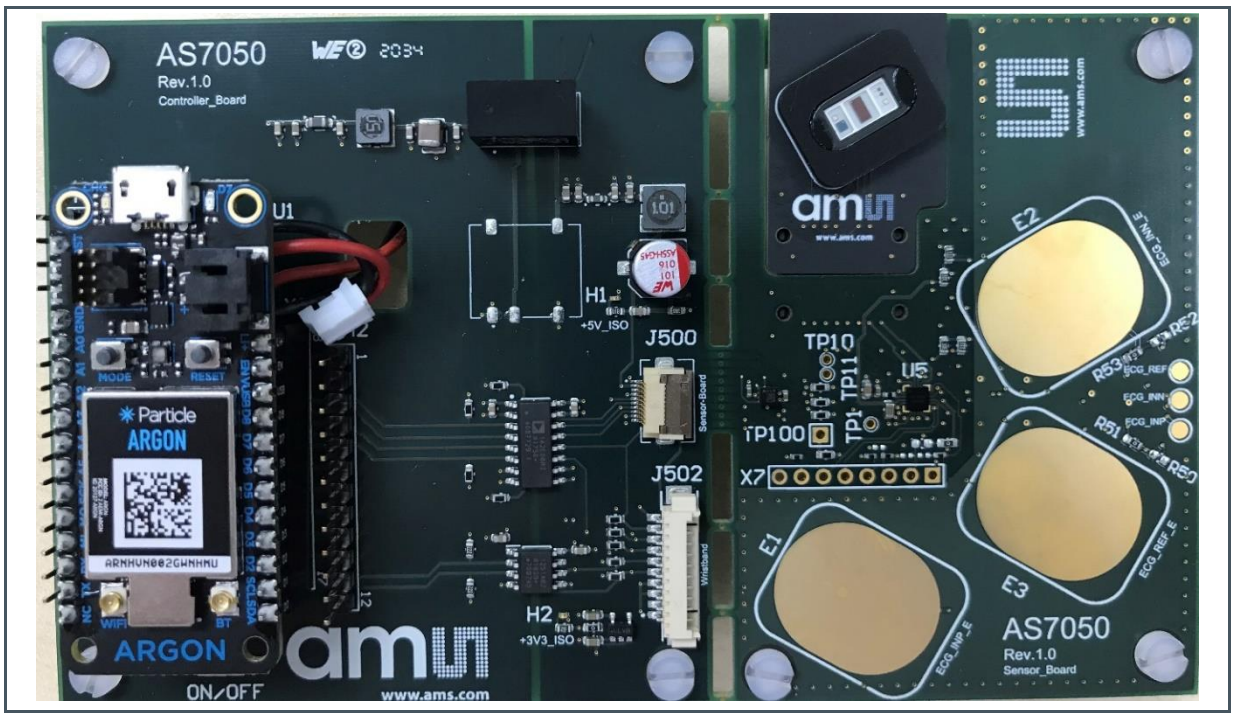
1 Introduction

The AS7050 Evaluation Kit allows for the evaluation of all the functions on the AS7050 Biosensors and tests them in various applications.

The initial Evaluation Kit works with a USB connection to the PC. It comes with a graphical user interface GUI which enables the user to perform measurements, change AS7050 register settings, and many more.

1.1 Kit Content

Figure 1:
AS7050 Evaluation Hardware Board



For full flexibility, the PCB of the evaluation kit has two parts: a Mainboard (Microcontroller part) and a Sensor board (Sensor part). The Sensor part has a vital signs sensor AFE (AS7050), an accelerometer, an LED-PD module (from ams OSRAM, part No.SFH7072), and three electrodes for ECG inputs. The Sensor board can be re-connected to the Mainboard via a Flexible Printed Circuit (FPC) cable if it is broken off. There is also an option to attach external electrodes as ECG inputs. If an optional Wristband evaluation kit is used, the AS7050 wristband is connected to the 10-pin Pico Blade connector on the Mainboard. Ensure that the sensor part of the kit is separated from the Mainboard before the Wristband is connected. Alternatively, ensure that the LED-PD module is disconnected.

The Evaluation Kit also contains firmware which can be updated by the user if necessary.

Any signals which are vital for development are accessible for probing at the pin headers.

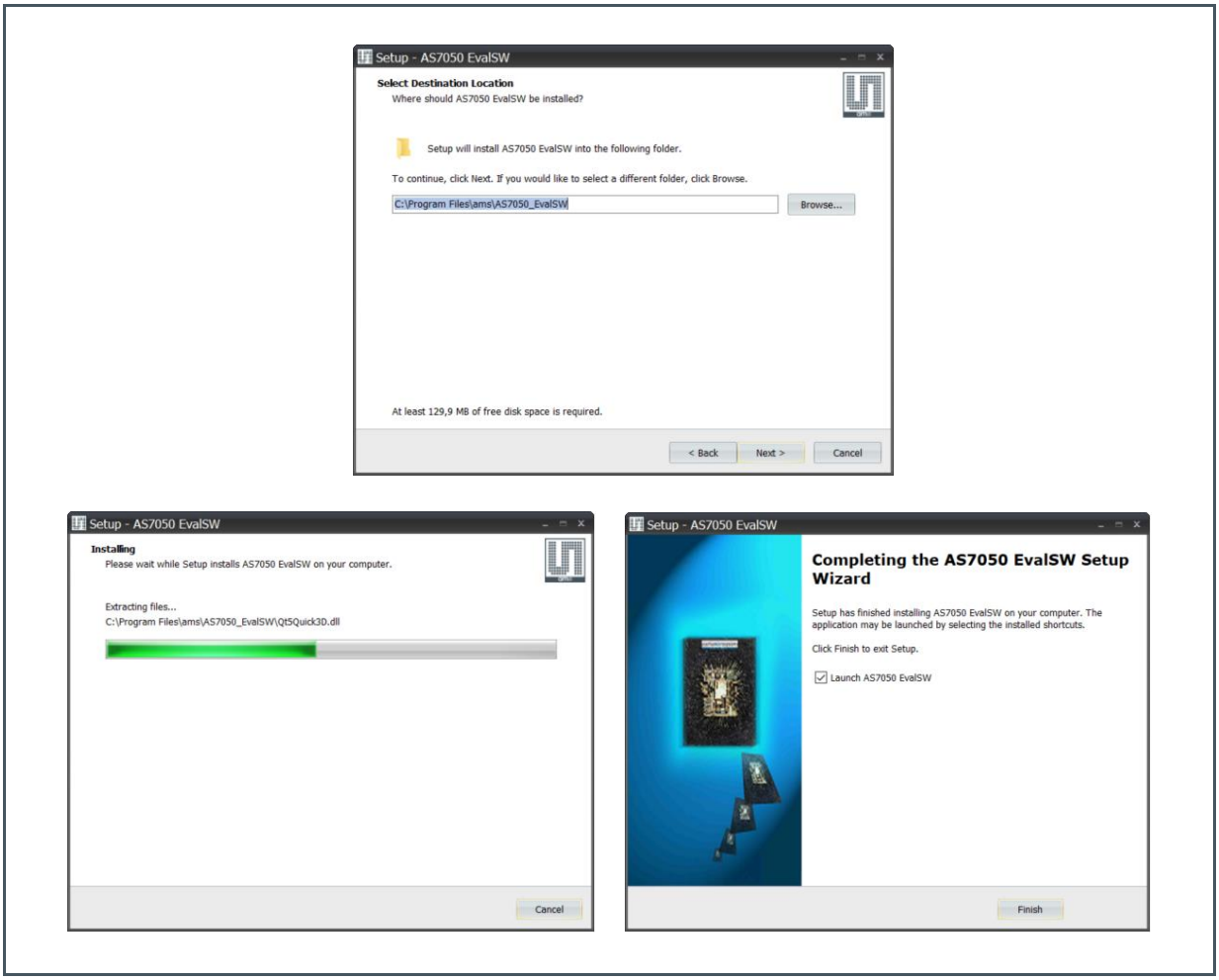
1.2 Ordering Information

Ordering Code	Description
AS7050_EVALKIT_BT	AS7050 USB Evaluation Kit

2 Getting Started

The latest version of the client software is available for download here. Alternatively, the software is also available on the USB stick as a part of the evaluation kit. To install, start the installer executable and follow the instructions as shown in Figure 2 (from left to right, top to bottom).

Figure 2:
AS7050 Evaluation Kit GUI Installation



3 Hardware Description

3.1 Hardware Architecture

Figure 3:
AS7050 Evaluation Hardware Board – Top View

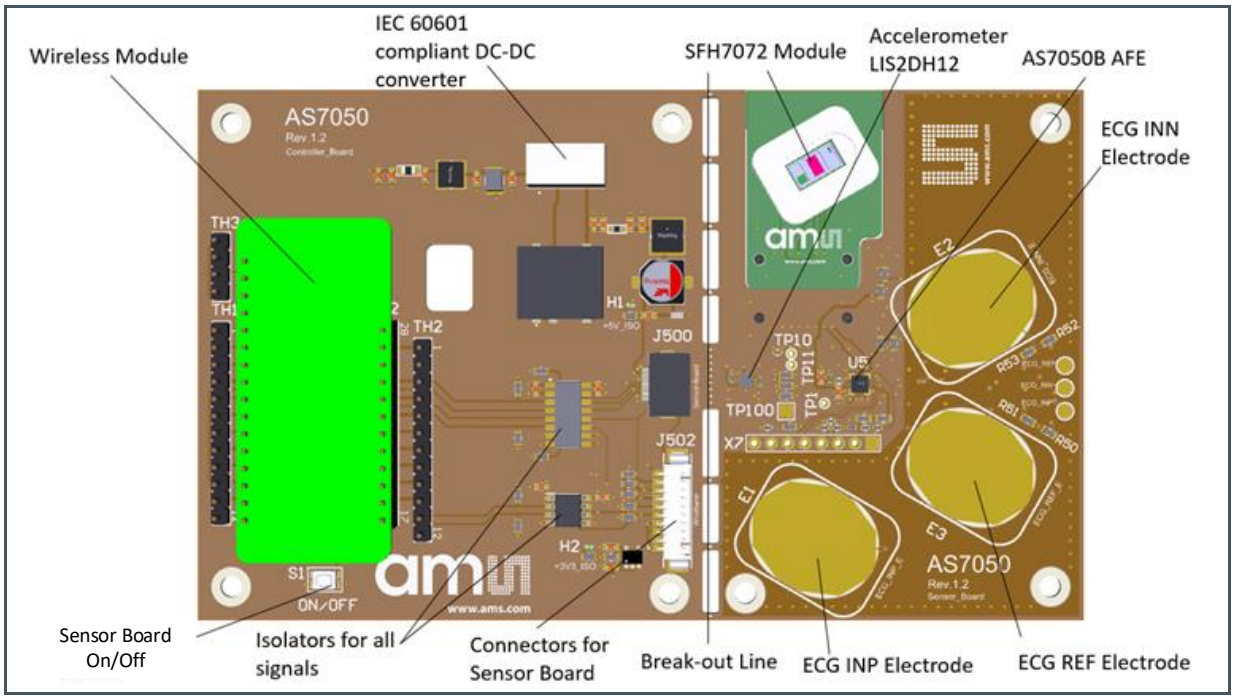
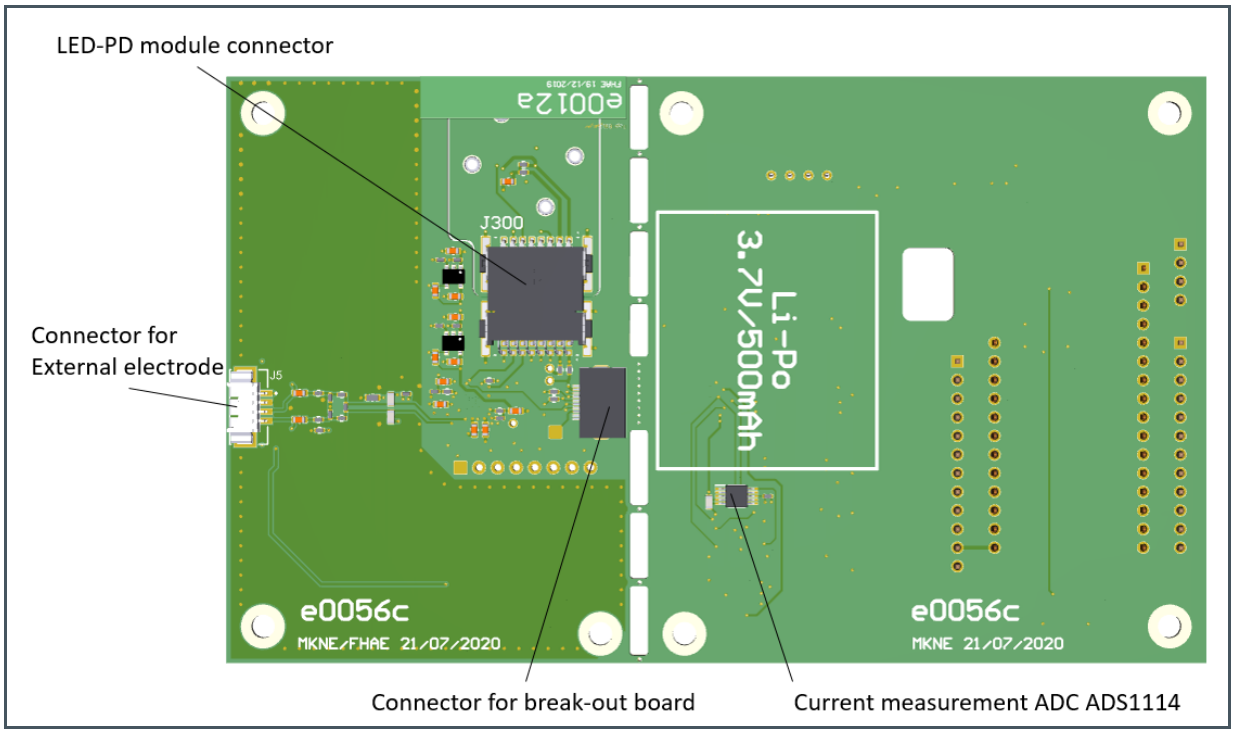


Figure 4:
AS7050 Evaluation Hardware Board – Bottom View



3.2 Power Supply

3.2.1 USB Connector

The source of power for the AS7050 Evaluation Kit is a USB connector on the wireless module. To avoid a direct connection from the electrodes to the power grid: an IEC 60601-1 compliant Traco Power DC/DC converter (TBA 1-0311) is assembled on the board, as well as isolator ICs, for all signals passing to the sensor board. Therefore, there is no galvanic connection between the sensor board and the power grid.

3.2.2 Battery Supply

A battery is provided for wireless use, and it needs to be connected to the wireless module. Also, the AS7050 EVK is to be connected to an Android/iOS device with a specific ams OSRAM application.

For further information, please refer to the following documents:

- ams-OSRAM AG, *ams OSRAM Vital Signs Mobile Application*, quick start guide.

The AS7050 EVK uses a Lithium-Ion battery.

Firstly, ensure that the battery is fully charged before connecting with the app. To charge the battery, plug in the micro USB connector and connect the AS7050 EVK to the computer. It can take up to 2 hours to charge the battery.

3.2.3 Technical Details

Figure 5:
Technical Details

Type	Rechargeable
Technology	Li-ion
Voltage	3.7 V
Capacitance	500 mAh
Nominal energy	1.85 Wh
Category	Cell

Do not use the product in humid, wet, and/or a corrosive environment. Do not put, store, or leave it in or near a heat source, a high temperature location, direct sunlight, a microwave oven, or a pressurized container, and do not expose it to temperatures over 60°C (140°F). Failure to follow these guidelines may cause the battery to leak acid, become hot, explode, or ignite and cause injury and/or damage. Do not pierce, open, or disassemble the battery. If the battery leaks and you come into contact with the leaked fluids, rinse thoroughly with water and immediately seek medical attention. For safety reasons, and to prolong the lifetime of the battery, charging will not occur at low (below 0°C/32°F) or high (over 45°C/113°F) temperatures.

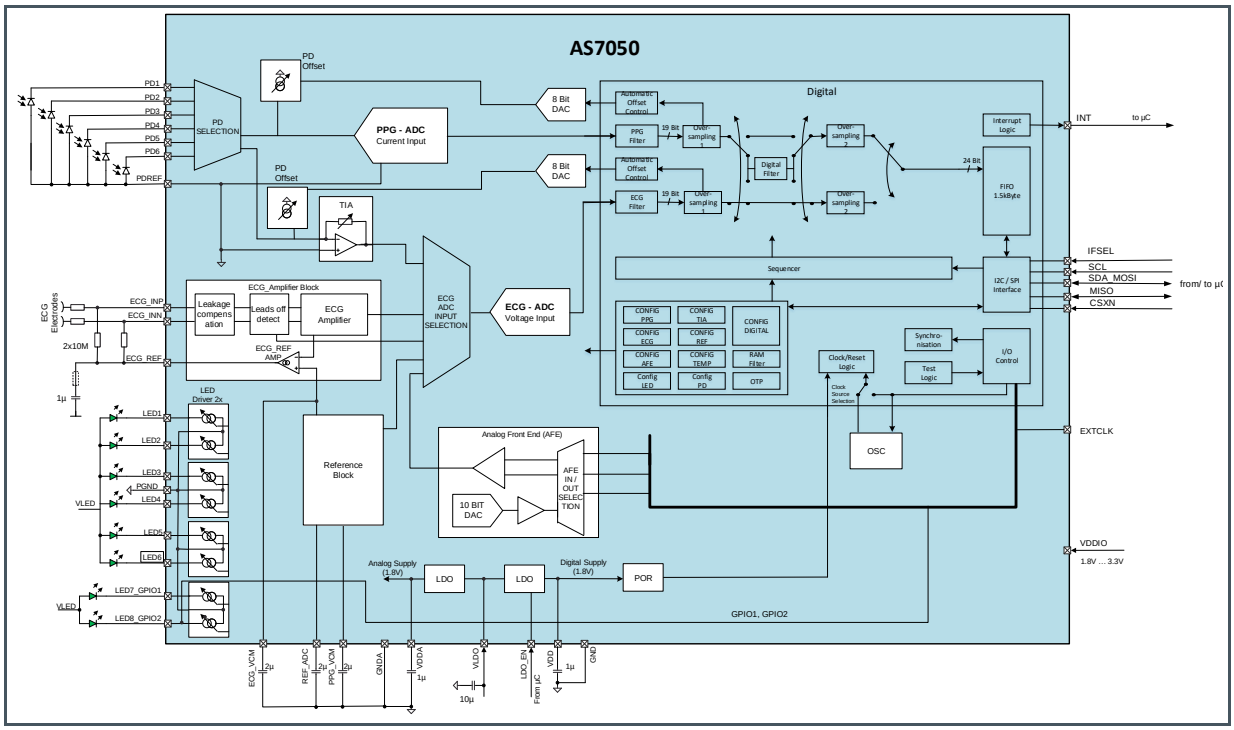
4 AS7050 Overview

The AS7050 is an analog frontend (AFE) that enables the measurement of photoplethysmography (PPG) electrocardiography (ECG) signals. PPG is the most used heart rate measurement (HRM) method. It is an optical technique that measures the heart rate by shining light on the skin, and sampling light, modulated by the blood vessels, which expand and contract as blood pulses through them. ECG, on the other hand, is an electrical technique for measuring the biopotential generated by the heart; by placing electrodes on the body parts.

Algorithms that convert the PPG signals into digital HRM and SpO2 support the AS7050. These can be further utilized to estimate other vital sign parameters such as heart/pulse rate variability, blood pressure, etc. The AS7050 can drive external LEDs and support additional photodiodes and electrodes. In addition to the vital signs, the device can also enable skin temperature and skin resistivity measurements with internal analog blocks.

All the functions of the AS7050 are controlled via an I²C/SPI interface. When using the internal LDO, the AS7050 wakes up via the LDO_EN pin. If the AS7050 switches to active mode, all the functions can be controlled using an external MCU via the I²C/SPI interface.

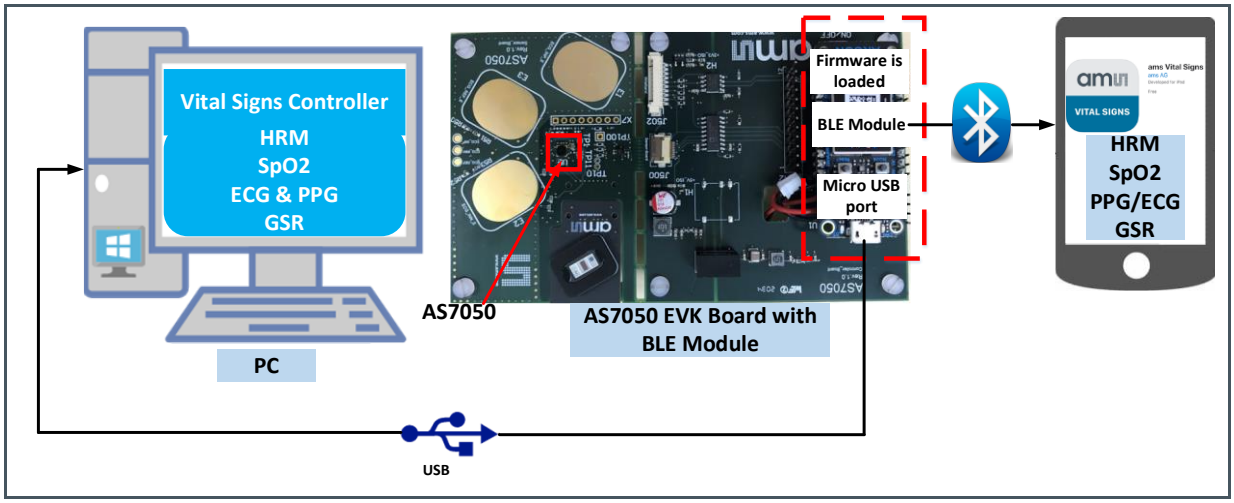
Figure 6:
AS7050 Block Diagram



5 Software Description

The chapter describes the essential workability of the AS7050 AFE. The software module provides software components, which enable a user to rapidly prototype their solutions.

Figure 7:
System Overview



The following software components are provided:

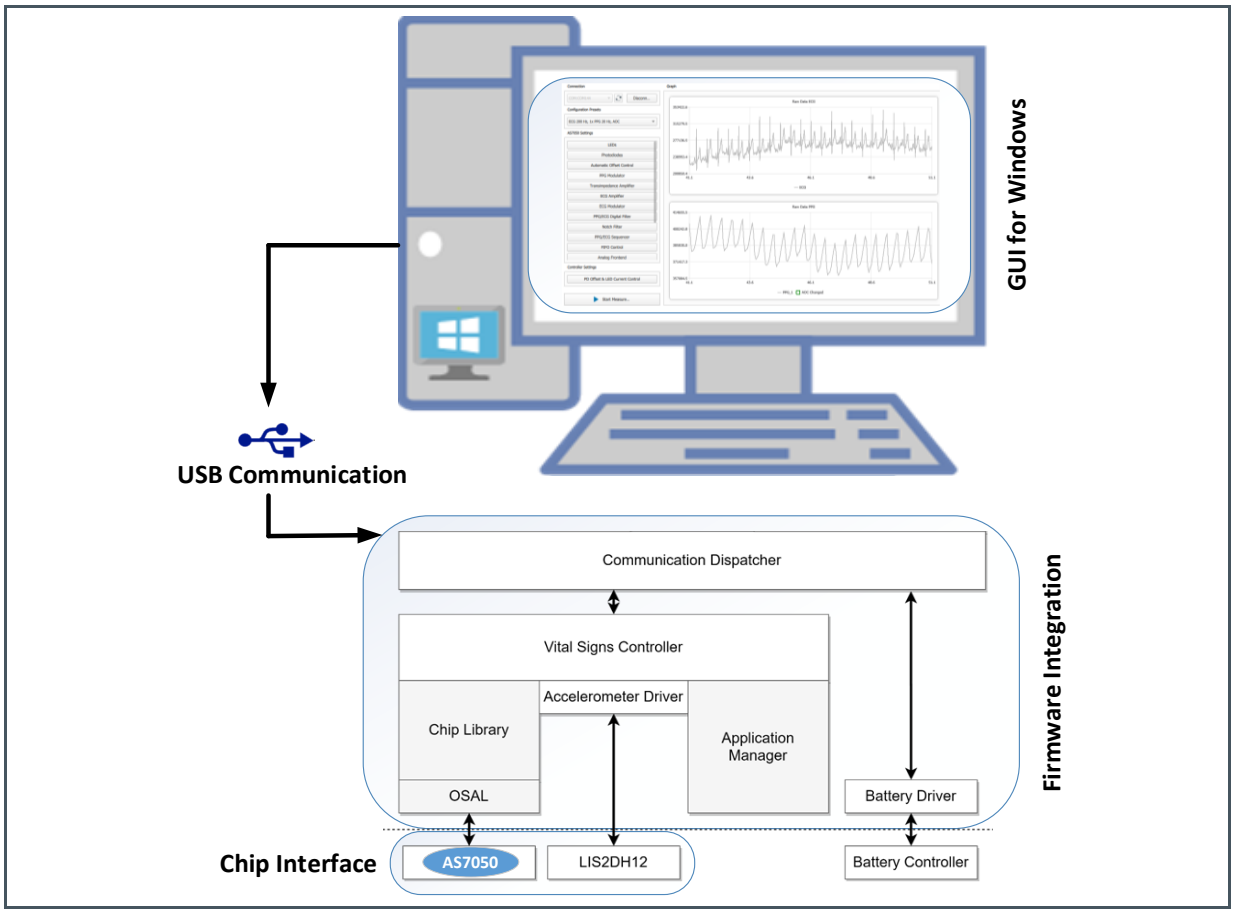
- Chip Library: Configures and controls the AS7050 sensor. It also delivers the output data from the sensor and the AGC status information.
- Application Manager: Configures and controls the Vital Signs Application.
- Vital Signs Application: Processes the measurement data from the Chip Library, and outputs the vital parameters below.
  - HRM/PRV Application: Heart rate and heart rate variability monitoring.
  - SpO2 Application: Blood oxygen saturation monitoring.
  - RAW Data Application: This is not a real Vital Signs Application. This application streams the raw ADC, accelerometer, and AGC status data (e.g. for recording or displaying).
  - GSR Application: Galvanic Skin Resistance with terminal resistance

For further information, please refer to the following documents:

- ams-OSRAM AG, *AS7050 Software Support Package*, user guide.
- ams-OSRAM AG, *ams OSRAM Vital Signs Mobile Application*, quick start guide.

5.1 Software Architecture

Figure 8:
SW Architecture for Windows GUI



5.2 Graphical User Interface

This section describes the Graphical User Interface (GUI) of the AS7050 Vital Sign Sensor application. The application is designed to be used with AS7050 vital sign sensor evaluation kit.

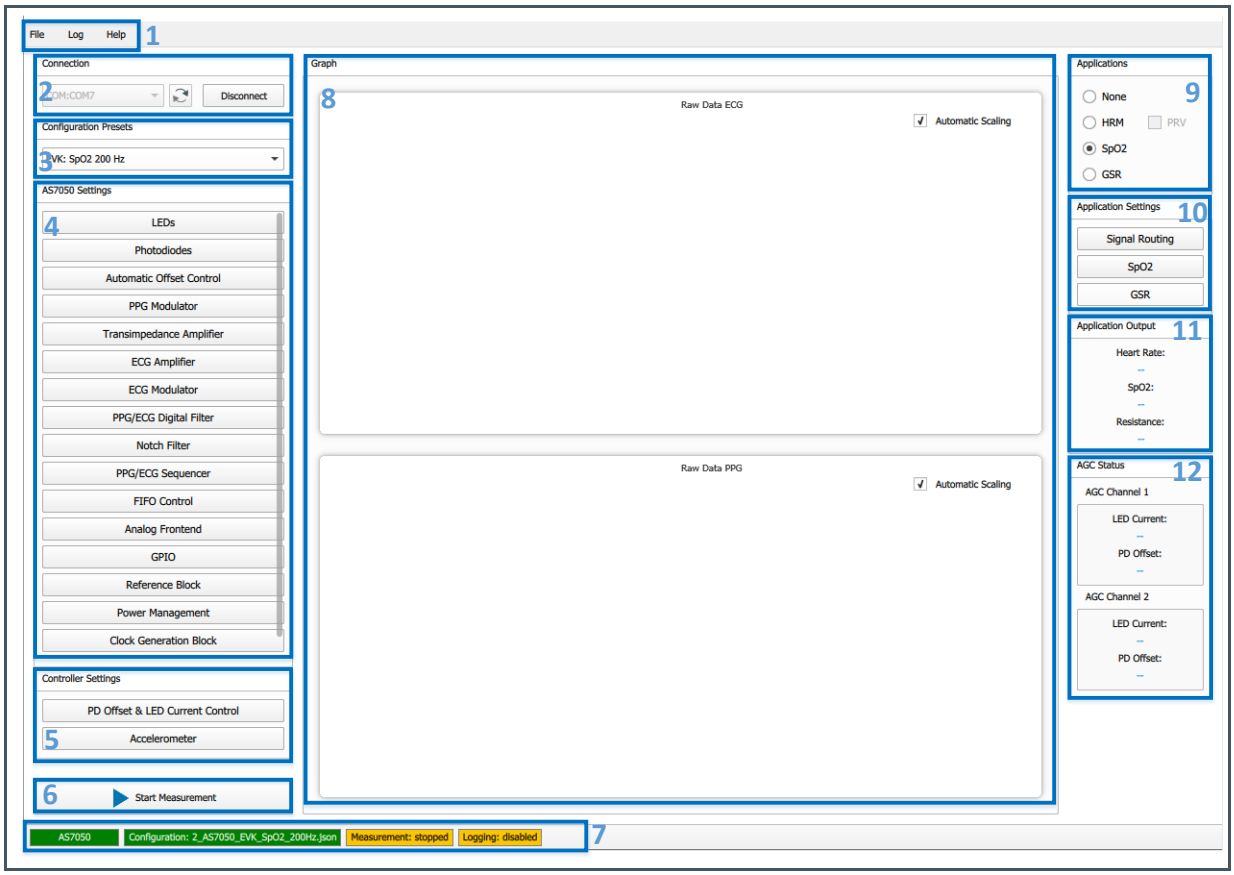
Information

- User Guide Version 1
- Valid for the following software version - AS7050 Vital Signs Sensor
- Supported hardware - Evalboard AS7050 Rev.1.0
- Download – Go here to download the latest version.

5.2.1 Overview

Figure 9 shows the main window of the GUI with different segments marked with numbered boxes. To connect to the board, the connection control elements are used (2, 3, and 4). The measured data is displayed in the main section of the application (8). Additional information about the set LED current, and the PD offset current by the software AGC are displayed in (12). Output data of the application algorithms, such as HRM and SpO2, data are displayed in (11).

Figure 9:
AS7050 Vital Signs Sensor – Graphical User Interface



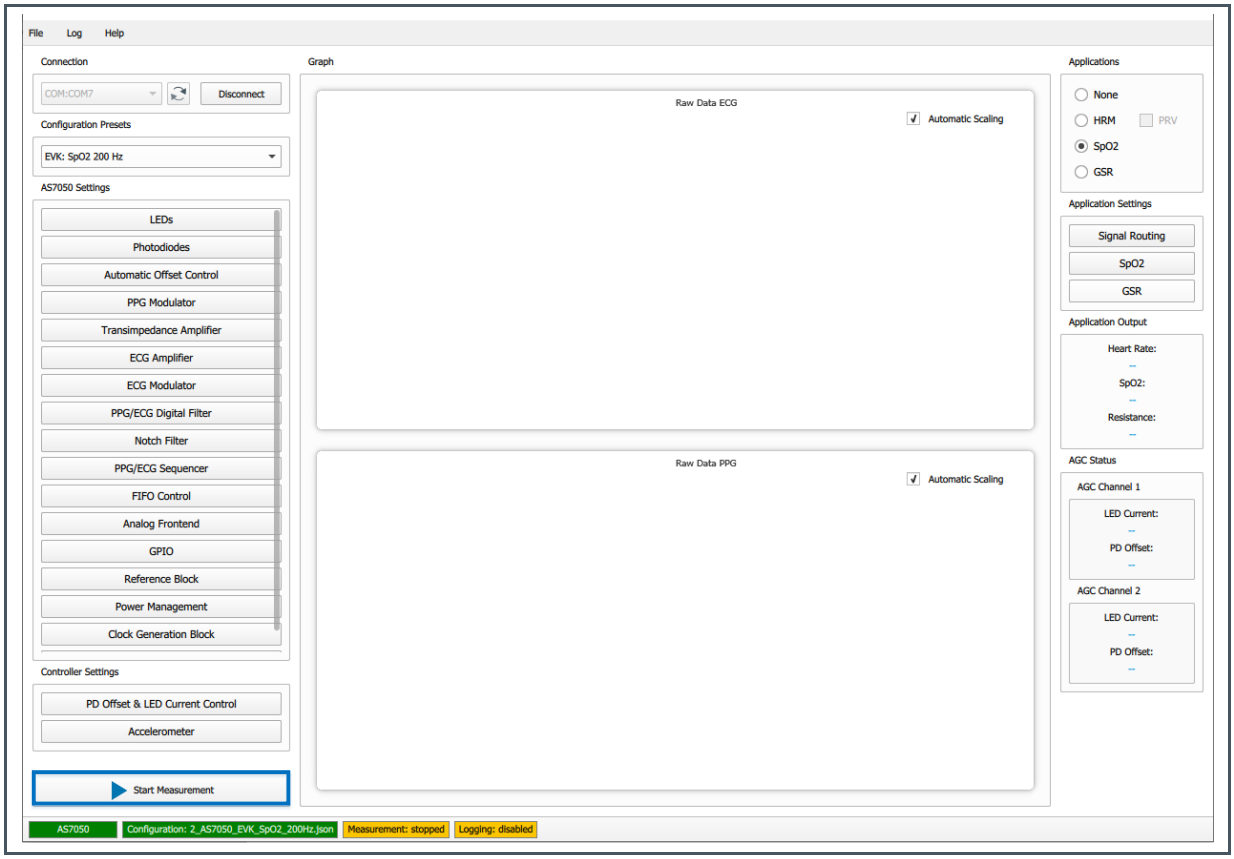
1	Main Menu	**7**	Status Window
2	Connection Window	**8**	Raw Data of PPG/ECG Signal
3	Configuration Presets	**9**	Measurement Type
4	Settings Window	**10**	Application Settings
5	PD & LED (AGC) Configuration with Accelerometer	**11**	Application Outputs
6	Start Measurements	**12**	AGC Status

5.2.2 Powering Up and Starting a Measurement

Powering Up

1. If you have broken the board, connect the sensor board and the mainboard via the 10-pin Pico blade cable. Otherwise, you can skip this step.
2. Connect the micro USB to USB-A cable to the mainboard, and plug it into your computer.
3. Afterwards, press the S1 button for three seconds to turn on the sensor board.
4. The green LED on the Bluetooth Microcontroller module will light up as soon as the board is powered.
5. Start the EVK GUI software.
6. Select the appropriate COM port number or BLE number from the drop-down menu.
7. Click the connect button, which subsequently changes the connection button to a disconnect button.
8. Select the right configuration file from the configuration presets.

Figure 10:
Starting a Measurement



Starting a Measurement

1. Select one of the configuration presets. Optionally, check and change the AS7050 AGC settings and other block settings.
2. To start measurement with the current settings, click on the button labeled “Start Measurement”.
3. Based on the selection of the configuration file:
   - Place a finger on the LED/PD module, or you will see the raw PPG data plot in the Graph window.
   - Place your fingers on the ECG electrodes, and subsequently, you will see the raw ECG data plot in the Graph window.
   - Place your fingers on the ECG electrodes & LED/PD module, and subsequently, you will see raw PPG & ECG data plots in the Graph window.

For further information, please refer to the following documents:

- ams-OSRAM AG, *AS7050 Eval Kit* (QG000166), quick start guide.

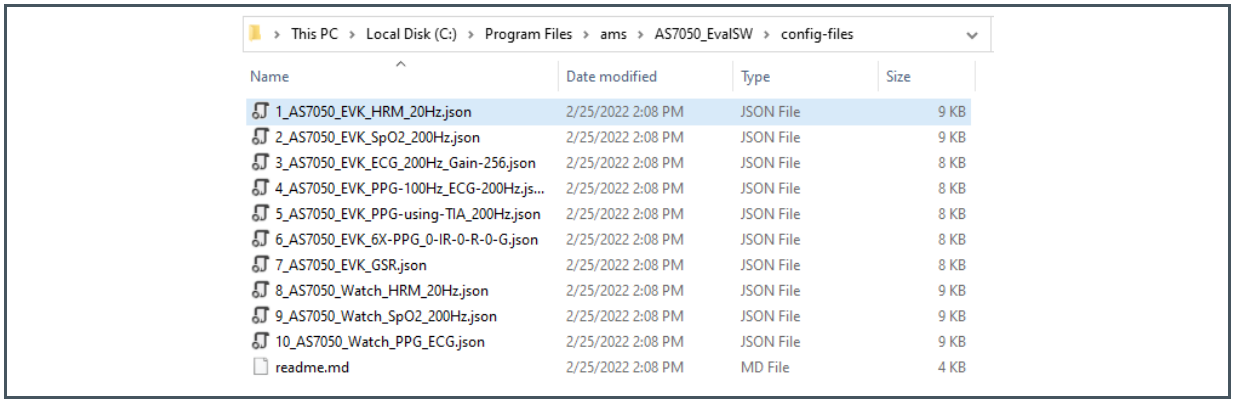
5.3 AS7050 Configuration Settings

The AS7050 configuration preset settings are located in the configuration JSON files of the latest release.

The individual settings of each of the AS7050 blocks can be found in a JSON file, and new settings can be saved in the JSON file.

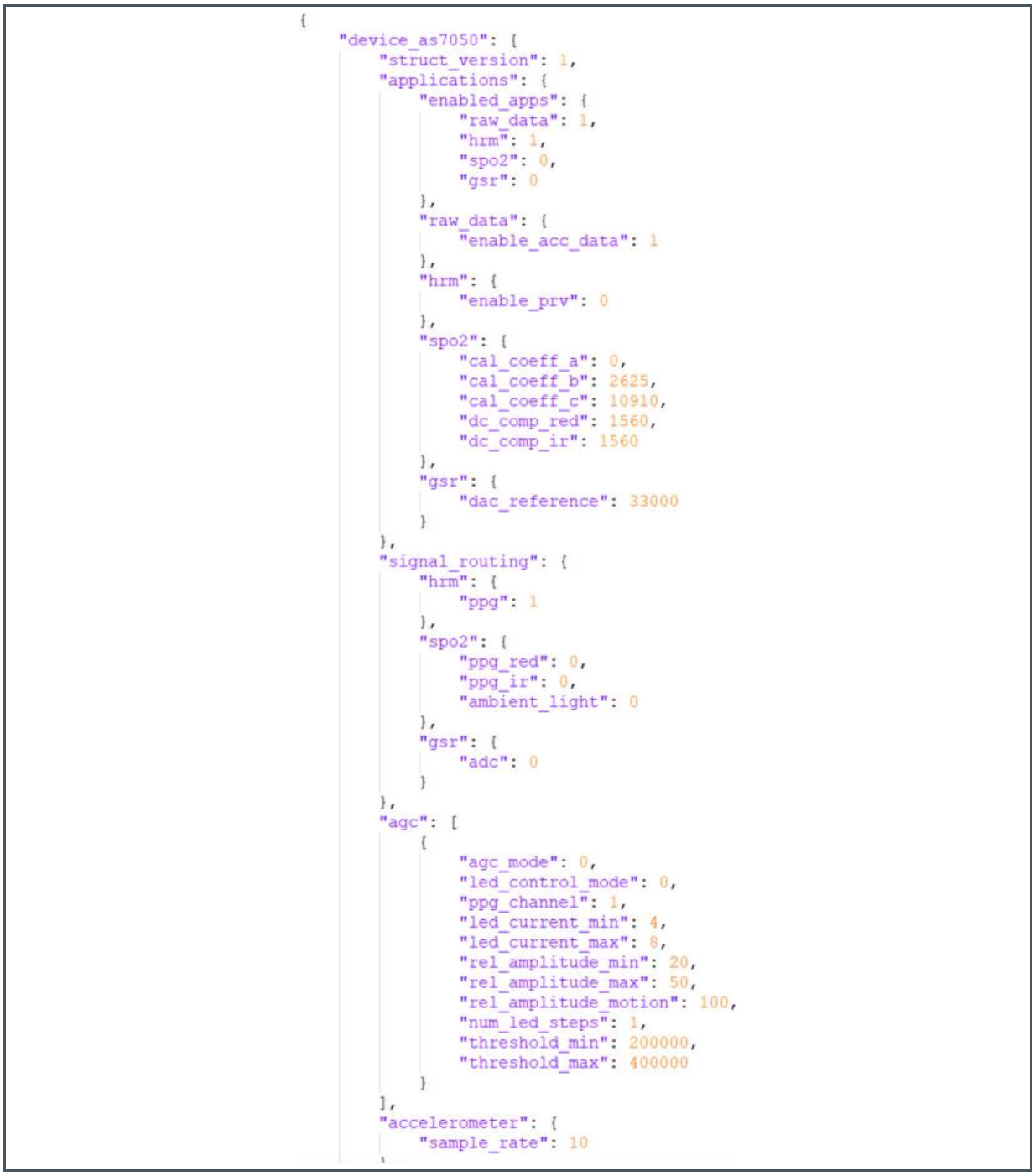
By default, the configuration presets are located in the folder “*C:\Program Files\ams\AS7050_EvalSW\config-files*” after the AS7050 software installation. Alternatively, they can be found in the user directory, depending on the installation folder.

Figure 11:
Default Preset Configuration Files



Application-specific default preset configuration JSON files store almost all the register information for the AS7050 AFE that are easy to read, as shown in Figure 11.

Figure 12:
AS7050 Configuration File(1)




```
{
    "device_as7050": {
        "struct_version": 1,
        "applications": {
            "enabled_apps": {
                "raw_data": 1,
                "hrm": 1,
                "spo2": 0,
                "gsr": 0
            },
            "raw_data": {
                "enable_acc_data": 1
            },
            "hrm": {
                "enable_prv": 0
            },
            "spo2": {
                "cal_coeff_a": 0,
                "cal_coeff_b": 2625,
                "cal_coeff_c": 10910,
                "dc_comp_red": 1560,
                "dc_comp_ir": 1560
            },
            "gsr": {
                "dac_reference": 33000
            }
        },
        "signal_routing": {
            "hrm": {
                "ppg": 1
            },
            "spo2": {
                "ppg_red": 0,
                "ppg_ir": 0,
                "ambient_light": 0
            },
            "gsr": {
                "adc": 0
            }
        },
        "agc": [
            {
                "agc_mode": 0,
                "led_control_mode": 0,
                "ppg_channel": 1,
                "led_current_min": 4,
                "led_current_max": 8,
                "rel_amplitude_min": 20,
                "rel_amplitude_max": 50,
                "rel_amplitude_motion": 100,
                "num_led_steps": 1,
                "threshold_min": 200000,
                "threshold_max": 400000
            }
        ],
        "accelerometer": {
            "sample_rate": 10
```


(1) All the register values displayed here are in decimals. However hexadecimals are also supported (0-255), without quotation marks.

5.3.1 LED Driver Configuration

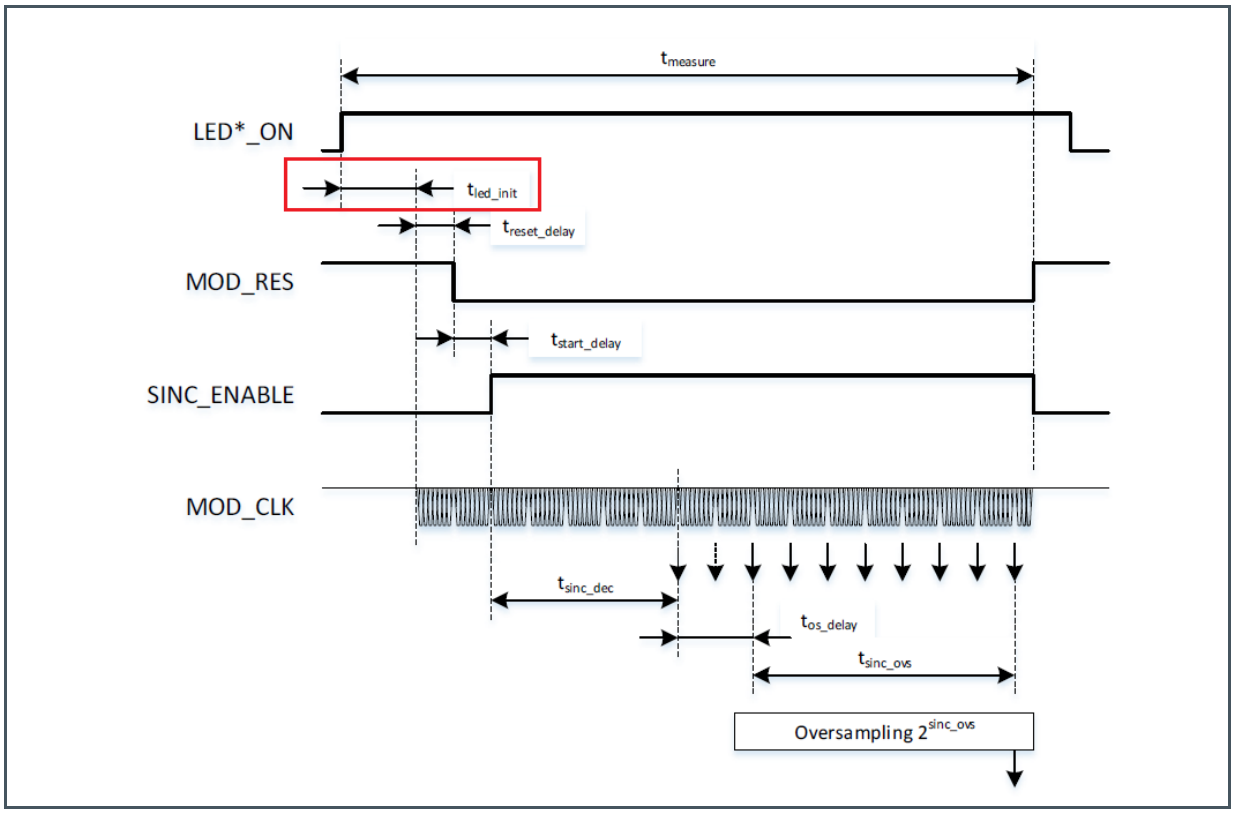
Figure 13:
LED Driver Configuration in the JSON File

- **lowvds_wait** (Address 0x27):
  Defines the time between switching on an LED and the start of voltage monitoring.

  $\mathrm{Time}=\mathrm{lowvds\_wait}*1\mu s$

  LED on detection: The LED driver compares the voltage at the LEDn pad against 0.3V (DROP). If the LED is on and the voltage at the LEDn pad is below the DROP voltage, then the output low_vds is set and assumed that the expected output current was not reached.
- **led1_ictrl-led6_ictrl** (Address 0x28 — Address 0x2D):
  The maximum output current is 300 mA.
  Bit0-6 selection LED current, Bit 7 selection current range.
  If Bit 6 = 0, step size = 1.17 mA.
  If Bit 7 = 1, step size = 2.34 mA.
- **led7_ictrl – led8_ictrl** (Address 0x2E — Address 0x2F):
  The maximum output current is 50mA.
  Bit0-6 selection LED current, Bit 7 has no function.
  Step size = 0.39mA.
- **led_init** (Address 0x4C):
  The configuration register for LED initialization time, $t\_LED\_INIT = N * 1\mu s$ with $N = 0 \ldots 255$.

Figure 14:
LED_INIT Time



- **led_ppg1 – led_ppg8** (Address 0x4D – 0x54):
  A combination of the LEDs for each PPG subsample (PPG1 to PPG8).
  Each PPG subsample has 8 bits, and each bit enables/disables the corresponding LED driver outputs.

Figure 15:
LED_PPGn Register Description

Address	Reg. Name	Sub-Sample	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x4D	LED_PPG1	1	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1
0x4E	LED_PPG2	2	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1
…	…	…	…	…	…	…	…	…	…	…
0x54	LED_PPG8	8	LED8	LED7	LED6	LED5	LED4	LED3	LED4	LED1

- **led_tia** (Address 0x55):
  A combination of the LEDs for the TIA sample if no PPG subsample is active.
  Same as LED_PPGn for enabling or disabling LED drivers.
- **led_mode** (Address 0x56):

The configuration register for LED sample modes.

Figure 16:
LED Mode Configuration for PPG and ECG Samples

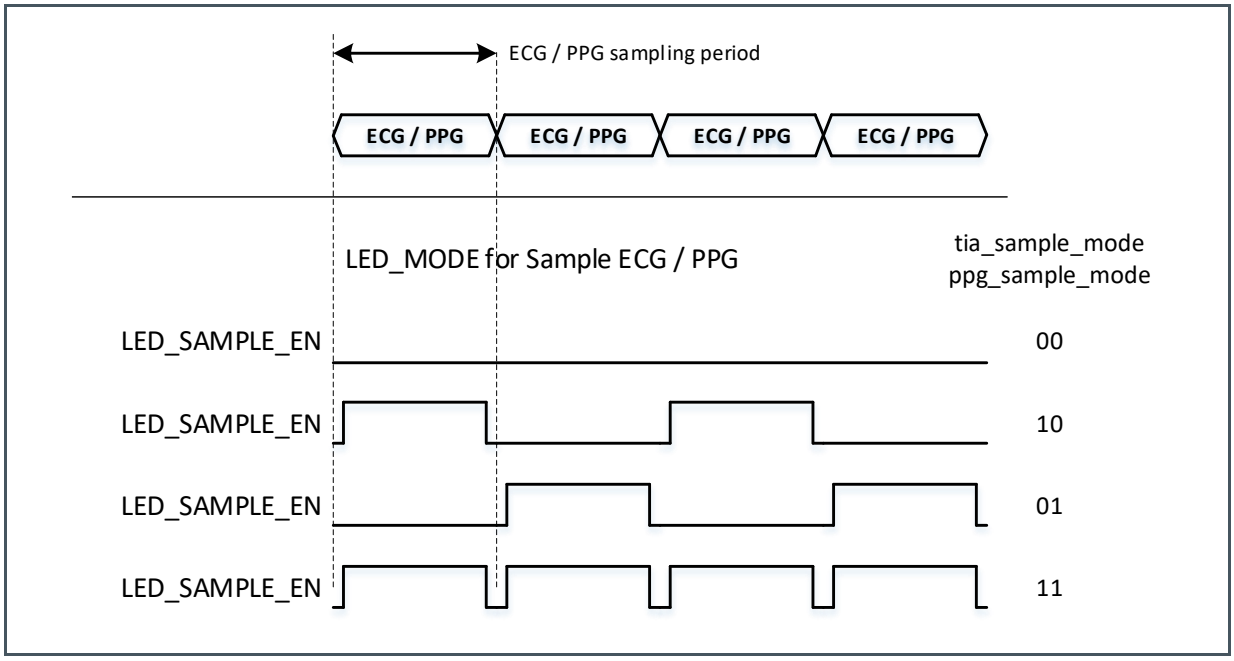
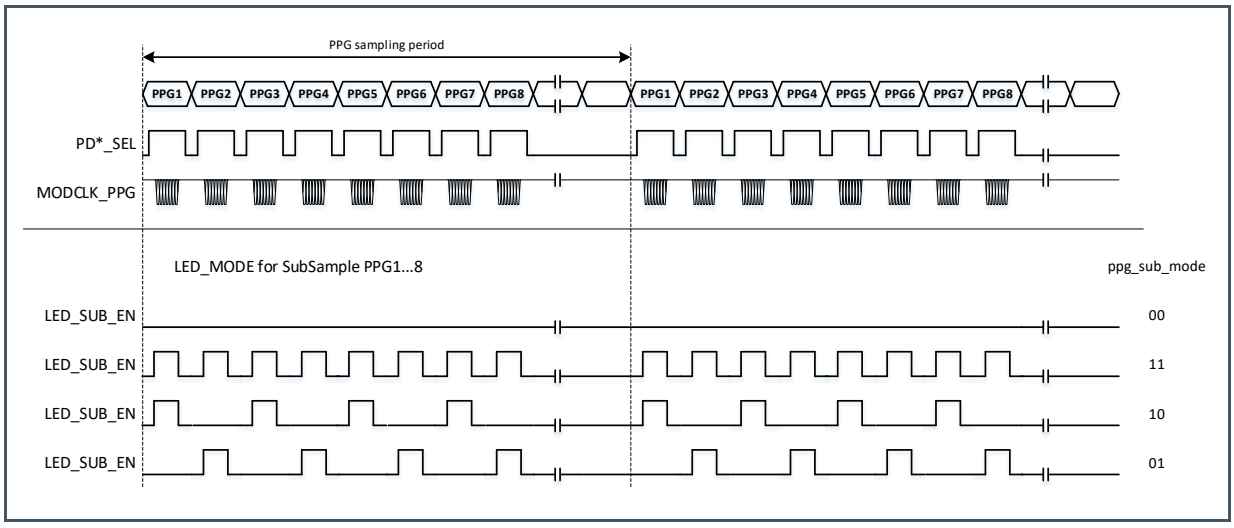
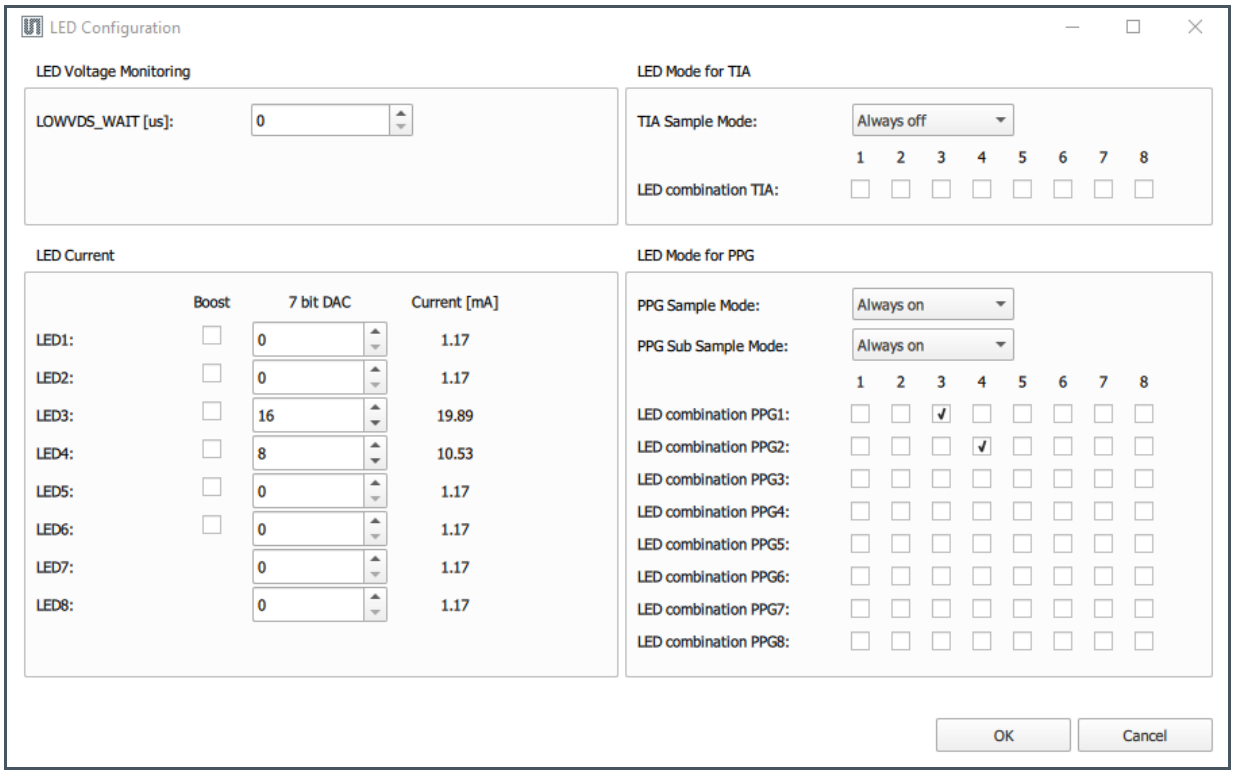


Figure 17:
LED Mode Configuration for PPG Subsamples



These LED configurations can be found in the GUI, under the “LEDs” submenu.

Figure 18:
LED Configuration Submenu



For further information, please refer to the following documents:

- ams-OSRAM AG, *AS7050 Biosignal Converting Unit* (DS000725), datasheet.

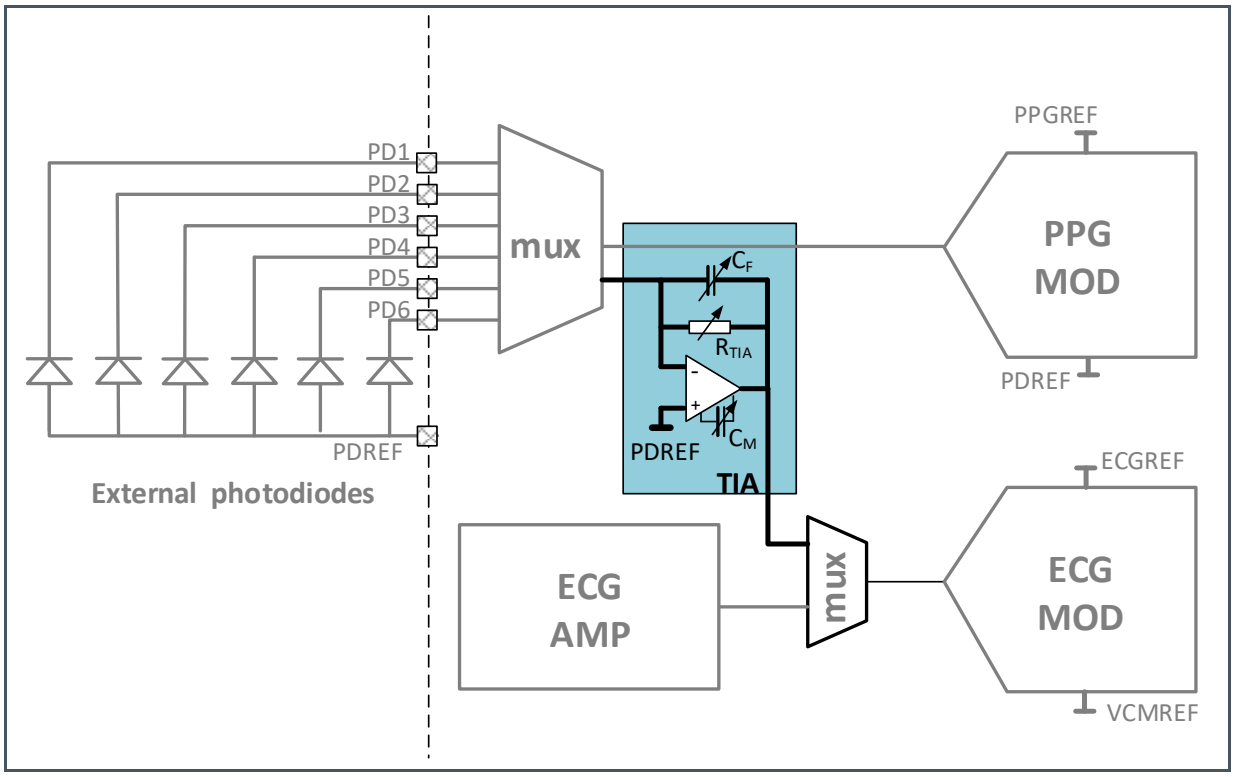
5.3.2 Photodiodes Configuration

Figure 19:
PD Configuration in the Configuration File

```
"pd": {
    "PDSEL_CFG": "0x00",
    "PD_PPG1": "0x01",
    "PD_PPG2": "0x01",
    "PD_PPG3": "0x01",
    "PD_PPG4": "0x00",
    "PD_PPG5": "0x00",
    "PD_PPG6": "0x00",
    "PD_PPG7": "0x00",
    "PD_PPG8": "0x00",
    "PD_TIA": "0x00"
},
```

- **pdsel_cfg** (Address 0x23):
  The configuration for the photodiode reference voltage connection – set it to 0 by default.

Figure 20:
PD_REF Connection



- **pd_ppg1 – pd_ppg8** (Address 0x43 – 0x4A):
  A combination of the PDs for each PPG subsample (PPG1 to PPG8).

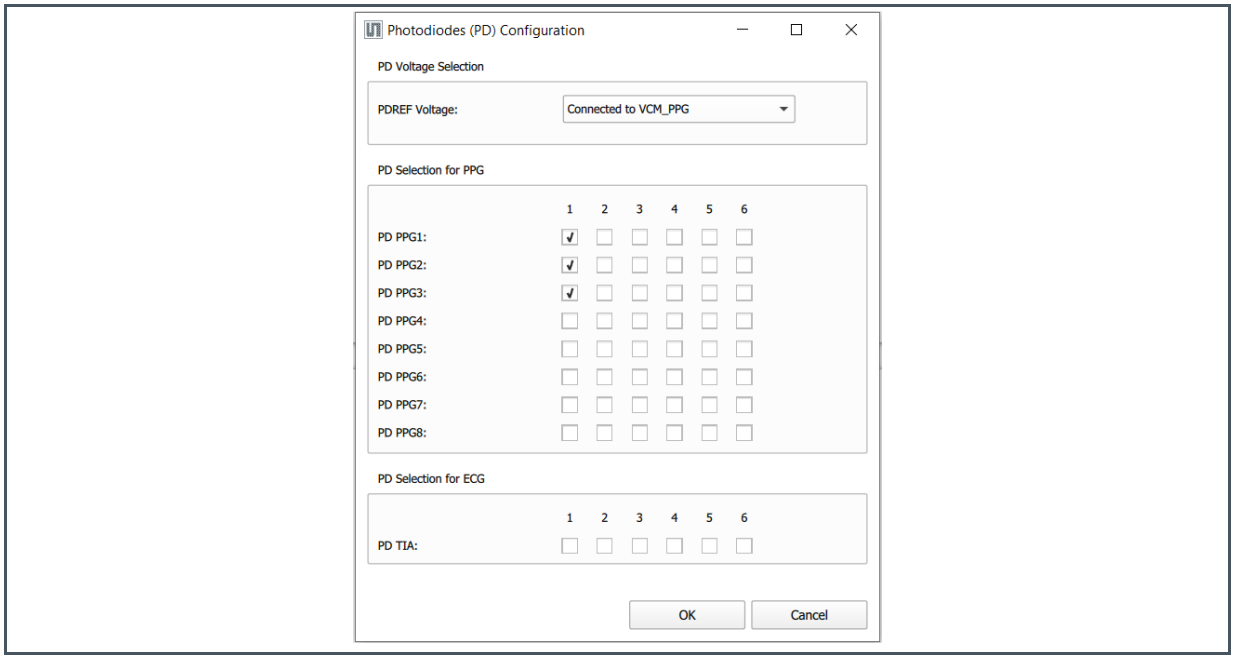
Figure 21:
PPG Subsample PD Configuration

Address	Reg. Name	Sub-Sample	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x43	PD_PPG1	1			PD6	PD5	PD4	PD3	PD2	PD1
0x44	PD_PPG2	2			PD6	PD5	PD4	PD3	PD2	PD1
…	…	…			…	…	…	…	…	…
0x4A	PD_PPG8	8			PD6	PD5	PD4	PD3	PD2	PD1

- **pd_tia** (Address 0x4B):
  A combination of the PDs for each TIA sample with ECG. It is the same as the PD_PPGn configuration. A PD used for TIA must not be used in a PPG subsample (PPG1 to PPG8).

These PD configurations can be found in the GUI, under the “Photodiodes” submenu.

Figure 22:
PD Configuration Submenu



For further information, please refer to the following documents:

- ams-OSRAM AG, *AS7050 Biosignal Converting Unit* (DS000725), datasheet.

5.3.3 PPG ADC Configuration

Figure 23:
PPG ADC Configuration in the Configuration File

```
"ppg": {
    "PPG_MOD_CFGA": "0xC6",
    "PPG_MOD_CFGB": "0x00",
    "PPG_MOD_CFGC": "0x07",
    "PPG_MOD_CFGD": "0x04",
    "PPG_MOD_CFGE": "0x0F"
},
```

The PPG ADC has six input full-scale ranges. To keep the ADC in stable operation, you need to follow the recommended settings below in Figure 24.

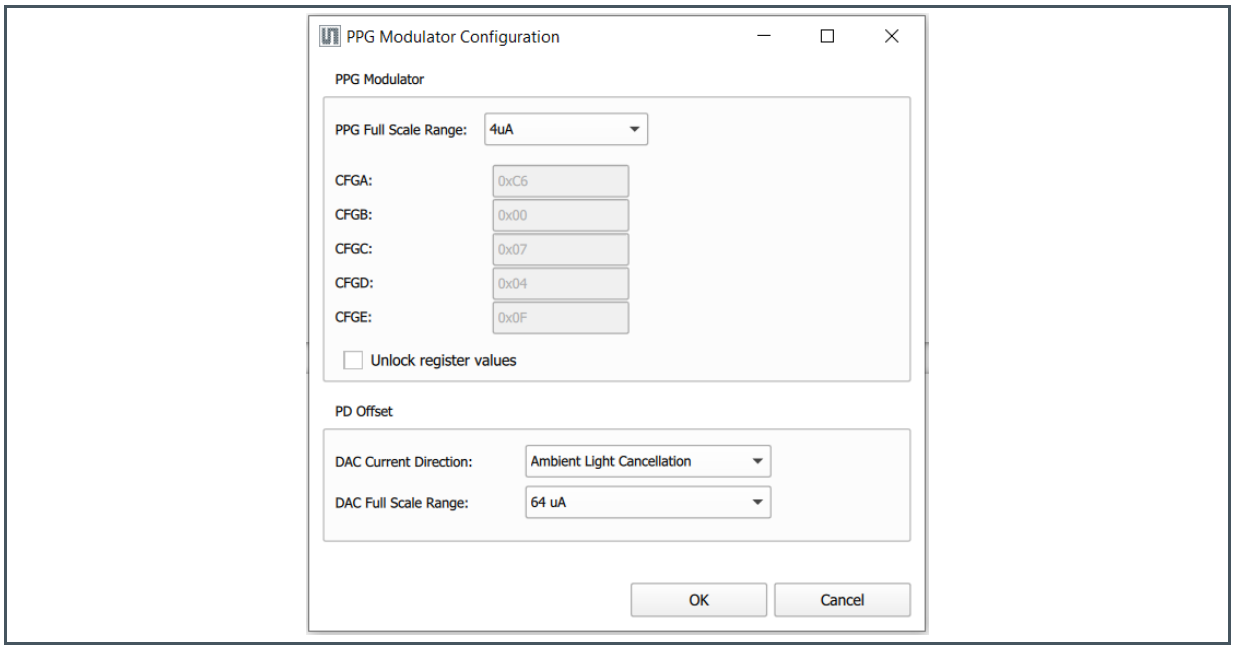
Figure 24:
PPG_MOD_CFGx Settings

ppg_mod_cfg	AGAIN	1µA	2µA	4µA	8µA	16µA	32µA
Register Name	Address	0	1	2	3	4(1)	5
PPG_MOD_CFGA	0x19	0xCX	0xCX	0xCX	0xCX	0xCX	0x8X
PPG_MOD_CFGB	0x1A	0x00	0x00	0x00	0x00	0x00	0x00
PPG_MOD_CFGC	0x1B	0x07	0x07	0x07	0x07	0x0F	0x1F
PPG_MOD_CFGD	0x1C	0x04	0x04	0x04	0x04	0x04	0x04
PPG_MOD_CFGE	0x1D	0x03	0x07	0x0F	0x1F	0x3F	0x7F

(1) Default setting, X = 0...7, see more details in the PD offset chapter

These PPG modulator settings can be found in the GUI, under the “PPG Modulator” submenu.

Figure 25:
PPG Modulator Configuration Submenu



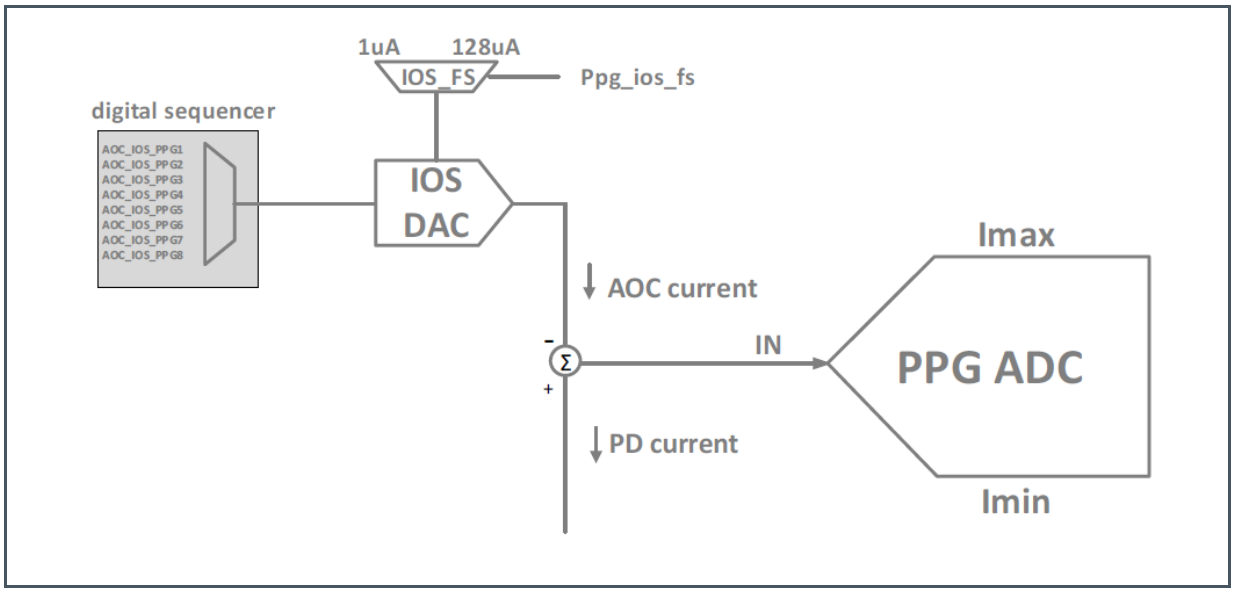
5.3.4 PPG PD Offset Configuration

Figure 26:
PD Offset Configuration

```
"aoc": {
    "AOC_IOS_PPG1": "0xFF",
    "AOC_IOS_PPG2": "0xFF",
    "AOC_IOS_PPG3": "0xFF",
    "AOC_IOS_PPG4": "0xFF",
    "AOC_IOS_PPG5": "0xFF",
    "AOC_IOS_PPG6": "0xFF",
    "AOC_IOS_PPG7": "0xFF",
    "AOC_IOS_PPG8": "0xFF",
    "AOC_PPG_THH": "0xB4",
    "AOC_PPG_THL": "0x82",
    "AOC_PPG_CFG": "0x81",
    "AOC_IOS_ECG": "0xFF",
    "AOC_ECG_THH": "0xB4",
    "AOC_ECG_THL": "0x82",
    "AOC_ECG_CFG": "0x01",
    "AOC_IOS_LEDOFF": "0xFA"
},
```

A programmable DC offset flows in the opposite direction of the photodiode current and reduces the effective signal coming into the ADC. This result enables the use of a more sensitive ADC signal range, resulting in a large number of PPG signal counts and better SNR compared to the case without offset correction.

Figure 27:
PD Offset



Ambient light can be compensated for each subsequence, either directly by writing a value from 0...255 to AOC_IOS_PPGi digital register values, or by a digital regulation loop.

Figure 28:
AOC Settings

Address	Register Name	Description
0x65	AOC_IOS_PPG1	AOC current value for subsample1
0x66	AOC_IOS_PPG2	AOC current value for subsample2
0x67	AOC_IOS_PPG3	AOC current value for subsample3
0x68	AOC_IOS_PPG4	AOC current value for subsample4
0x69	AOC_IOS_PPG5	AOC current value for subsample5
0x6A	AOC_IOS_PPG6	AOC current value for subsample6
0x6B	AOC_IOS_PPG7	AOC current value for subsample7
0x6C	AOC_IOS_PPG8	AOC current value for subsample8

Besides that, we can change the IOS DAC full-scale range from 1µA-128µA in the register PPG_MOD_CFGA (Address 0x41) bit [2:0].

Figure 29:
AOC Current

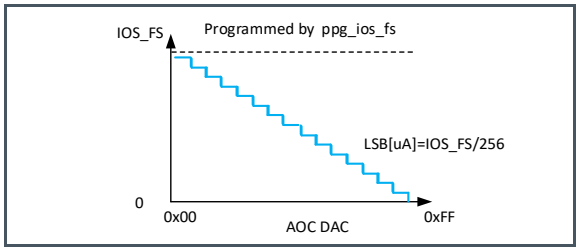


Figure 30:
IOS DAS Full-Scale Range

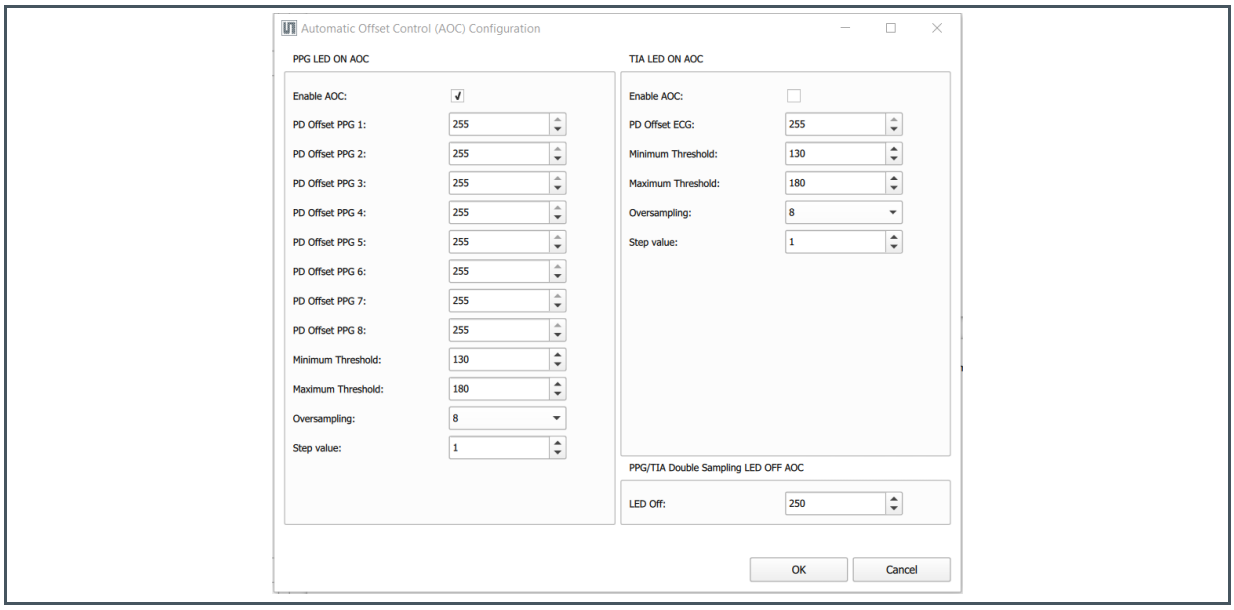
PPG_IOS_FS

reg. Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PPG_MOD_CFGA	x	x	x	x	x	0	1uA	
	x	x	x	x	x	1	2uA	
	x	x	x	x	x	2	4uA	
	x	x	x	x	x	3	8uA	
	x	x	x	x	x	4	16uA	
	x	x	x	x	x	5	32uA	
	x	x	x	x	x	6	64uA	
	x	x	x	x	x	7	128uA	

- **aoc_ppg_thh** (Address 0x6D):
  The threshold for decreasing the PD_OFFSET for all PPG subsamples. The maximum value for aoc_ppg_thh is “0xBF”.
- **aoc_ppg_th1** (Address 0x6E):
  The threshold for increasing the PD_OFFSET for all PPG subsamples. The minimum value for aoc_ppg_th1 is “0x80”.

The AOC configurations can be found in the GUI, under the “Automatic Offset Control” submenu.

Figure 31:
AOC Configuration Settings Submenu



5.3.5 ECG Amplifier Configuration

The ECG (electrocardiogram) amplifier is a high-impedance, low-noise, instrumentation amplifier, with analog circuitry to a bandpass filter and amplify the signal.

Figure 32:
ECG Amplifier Configuration

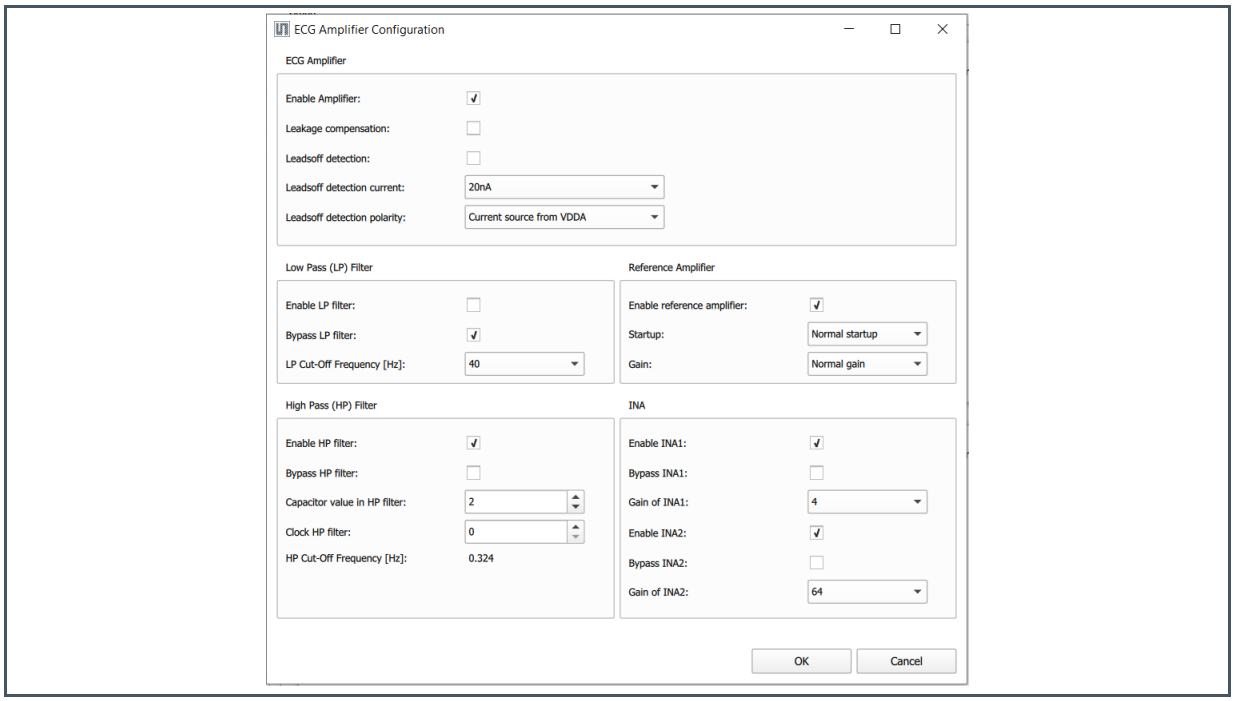
```
"amp": {
    "ECG_AMP_CFGA": "0x81",
    "ECG_AMP_CFGB": "0xAB",
    "ECG_AMP_CFGC": "0xB4",
    "ECG_AMP_CFGE": "0x44"
},
```

- **ECG_AMP_CFGA** (Address 0x20)
- The ECG amplifier is controlled via several signals from the sequencer and I²C registers. The ECG leadoff detection and leakage compensation are part of the ECG amplifier. The result of a Leadoff/ECG electrode off detection is a converted result from the ADC. The ECG leakage compensation can be enabled for ECG input pads and the current source from VDDA (positive analog supply), or the current sink to VSSA (analog ground) can be selected for the leadoff detection polarity.**ECG_AMP_CFGA** (Address 0x20) & **ECG_AMP_CFGE** (Address 0x39)

- The Low Pass (LP) is part of the ECG amplifier. The filter employs a fully differential second-order low-pass filter structure. The internal supply voltage of 1.9 V powers it. The cut-off frequency can be set from 40Hz to 320Hz by changing the clock frequency of the filter. The LP filter can be enabled, and with the bypass LP filter option, the LP filter can be bypassed (IN=OUT).**ECG_AMP_CFGB** (Address 0x21) & **ECG_AMP_CFGE** (Address 0x39)
- The High Pass (HP) filter is part of the ECG amplifier. The filter employs a fully-differential first-order high-pass filter topology. The internal supply voltage of 1.9 V powers it. The cut-off frequency can be set from 0.17 Hz to 10.56 Hz by changing the clock frequency and the capacitor size of the filter. The HP filter can be enabled, and with the bypass HP filter option, the HP filter can be bypassed (IN=OUT).**ECG_AMP_CFGC** (Address 0x22)
- The reference amplifier supports two modes for the external load conditions. In the normal operational mode, the reference block is limited to a low range. This mode is called Normal startup mode. On the other hand, when the reference block reaches a relatively higher value than the standard value, the mode is called fast startup mode. Normal or high gain can be selected for the ECG reference amplifier gain.**ECG_AMP_CFGB** (Address 0x21) & **ECG_AMP_CFGC** (Address 0x22)

  The ECG measurement uses an instrumentation amplifier, which helps to suppress any unwanted common-mode signals. It is also a high gain voltage amplifier. The INA can be enabled, and with the bypass INA option, the INA can be bypassed.

Figure 33:
ECG Amplifier Configuration Submenu



5.3.6 ECG Modulator

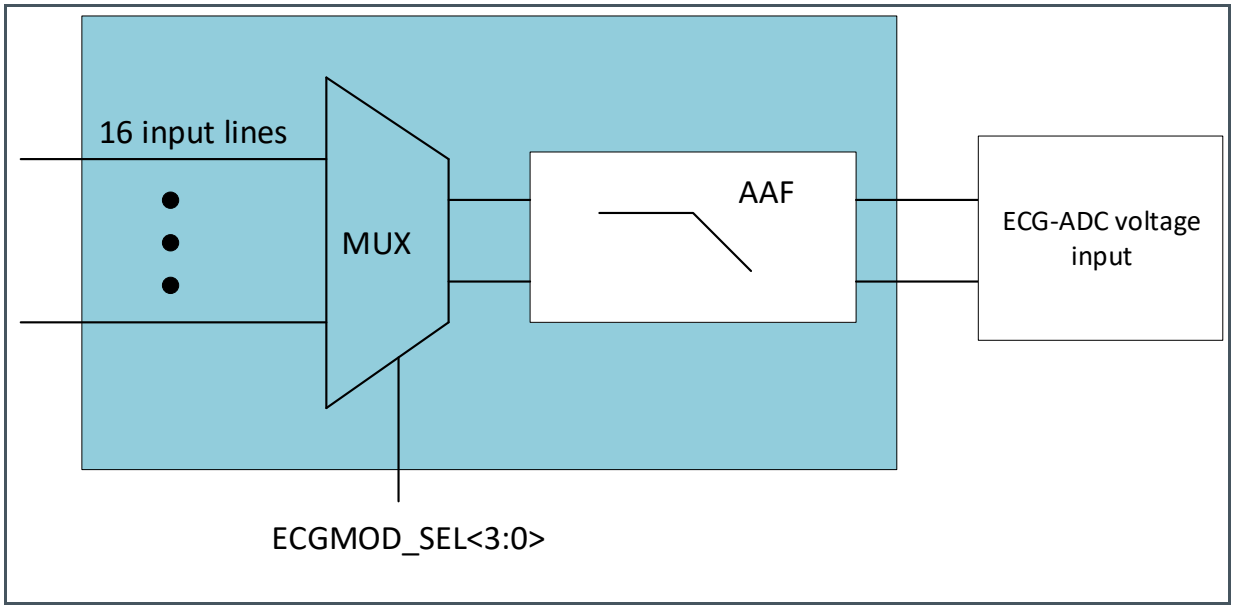
Electrodes capture the voltage difference, filter out noise, and amplify the signal. The ECG modulator modulates the amplitude of the ECG signal.

Figure 34:
ECG Modulator

```
"ecg": {
    "ECG_SOURCE": "0x40",
    "ECG_MOD_CFGA": "0x90"
},
```

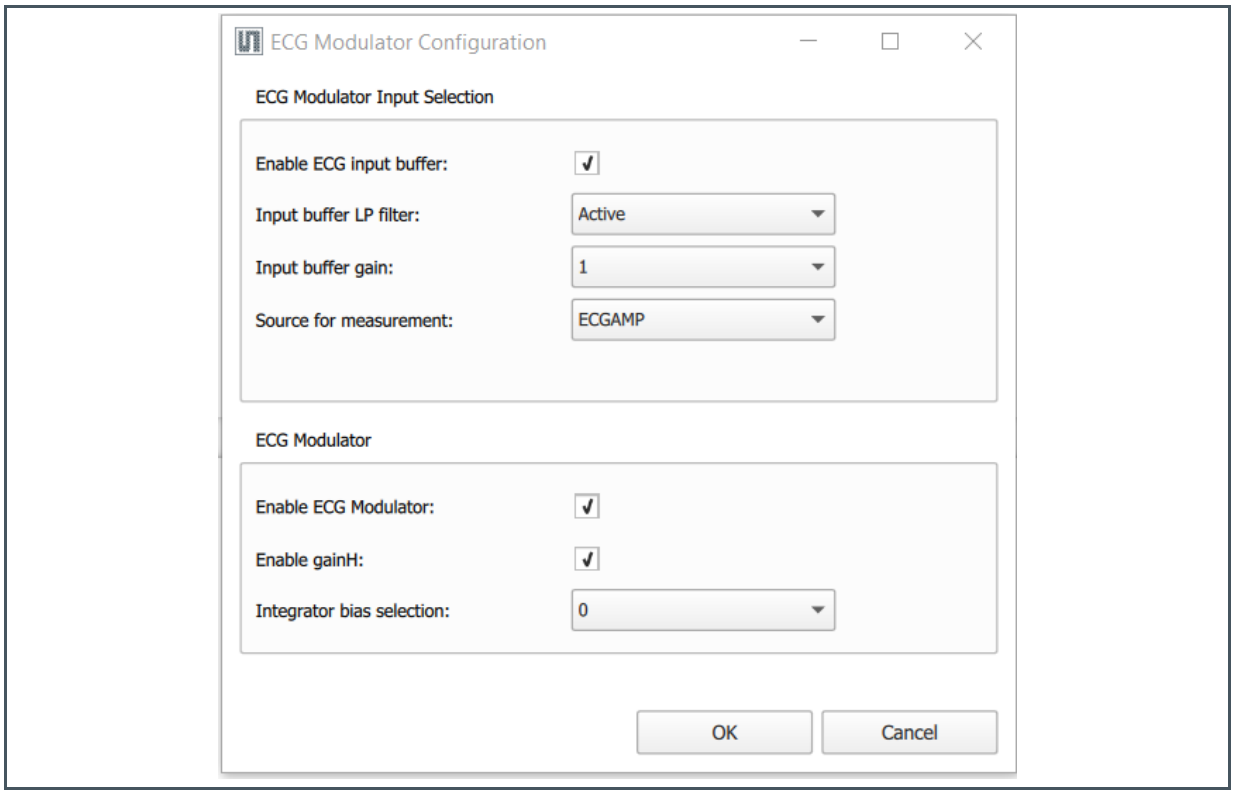
The ECG modulation input buffer can be enabled to provide a high input impedance. It is possible to activate or bypass the high impedance LP buffer filter and change the gain stage of the buffer input. With the ECG-ADC input selection, it is possible to read out more input signals via the ECG channel. It can be chosen between six different input sources, such as PD-TIA, ECG-AMP, AFE, ECG lead detection, temperature, or an external voltage source. However, selection of source for measurement via the ECG channel cannot be changed during the active ECG measurement.

Figure 35:
ECG-ADC Input Selection



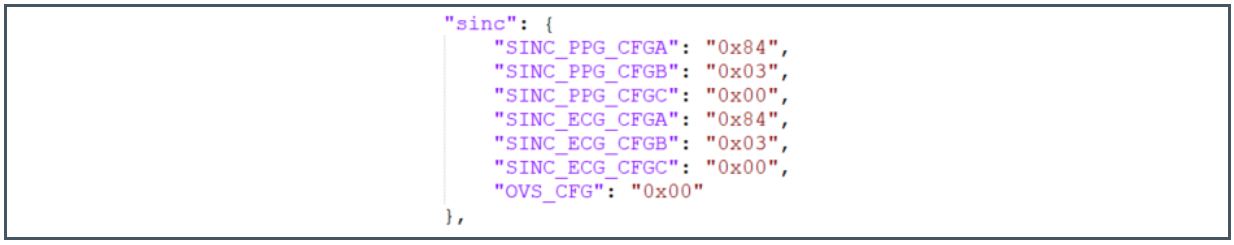
ECG modulation can be enabled to modulate the ECG signal. DSM gain can also be enabled. An anti-aliasing filter (AAF) is used in the ECG-ADC input selection before the signal sampler or ECG-ADC voltage input to restrict the bandwidth of a signal and satisfy the band over the band of interest.

Figure 36:
ECG Modulator Submenu



5.3.7 PPG/ECG ADC Digital Filter

Figure 37:
ADC Digital Filter Configuration



```
"sinc": {
    "SINC_PPG_CFGA": "0x84",
    "SINC_PPG_CFGB": "0x03",
    "SINC_PPG_CFGC": "0x00",
    "SINC_ECG_CFGA": "0x84",
    "SINC_ECG_CFGB": "0x03",
    "SINC_ECG_CFGC": "0x00",
    "OVS_CFG": "0x00"
},
```

With the digital filter, it is flexible to configure the following: filter type, filter order, filter decimation rate, and PPG modulator frequency.

The digital filter's configuration results in a different ADC conversion time (ADC) and the effective number of bits of the ADC (ENOBs). Therefore, we highly recommend that you follow the settings below to get the best ADC performance combinations.

Figure 38:
PPG Sinc Filter

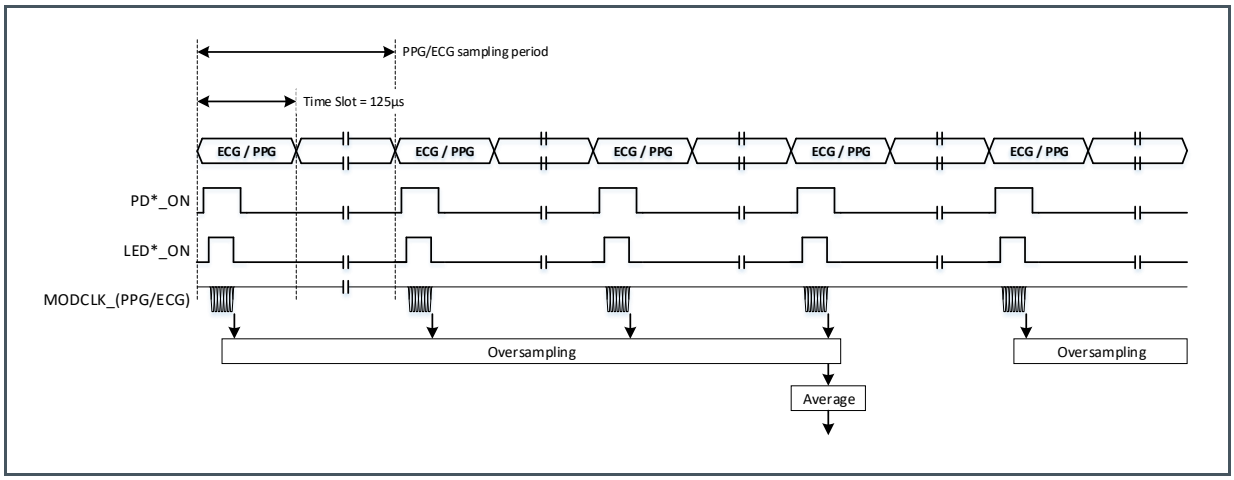
Combination	sinc_ppg_cfga (0x5B)	sinc_ppg_cfgb (0x5C)	ADC Conversion Time (µs)
1	0x00	0x00	5.7
2	0x04	0x00	7.3
3	0x08	0x02	10.6
4	0x10	0x02	29.8
5	0x08	0x01	35.7
6	0x08	0x03	42.1

Figure 39:
ECG Sinc Filter

Combinaton	sinc_ecg_cfga (0x5E)	sinc_ecg_cfgb (0x5F)	ADC Conversion Time (µs)
1	0x00	0x00	5.7
2	0x04	0x00	7.3
3	0x08	0x02	10.6
4	0x10	0x02	29.8
5	0x08	0x01	35.7
6	0x08	0x03	42.1

- **ovs_cfg** (Address 0x64):
  This is the configuration register for oversampling ECG and PPG.
  The AS7050 allows you to average up to 16 output samples, which is done by the internal hardware blocks.

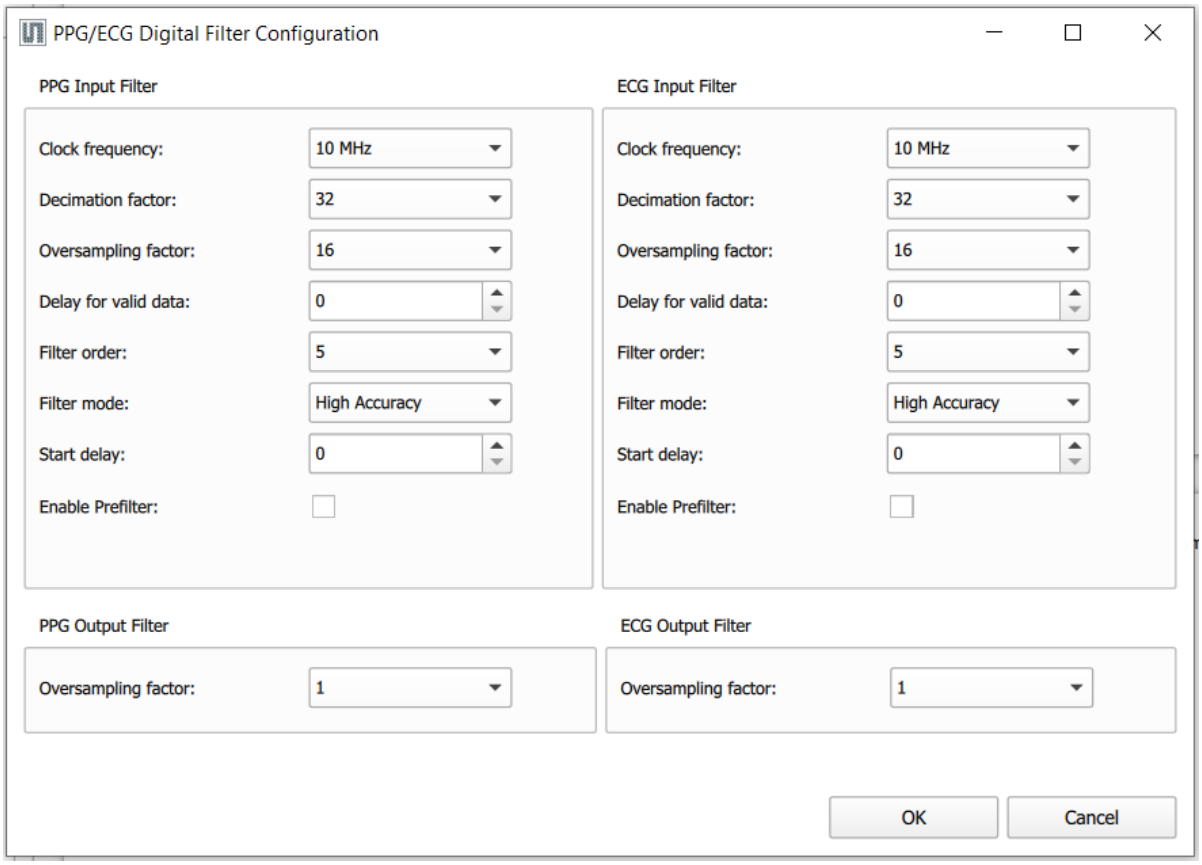
Figure 40:
Sample Averaging Oversampling for PPG/ECG



These PPG ADC digital filter configurations, or ECG ADC digital filter configurations, can be found in the GUI, under the “PPG/ECG Digital Filter Configuration” submenu.

There are two types of Oversampling. One for the Input Filter and the other for the Output Filter. Figure 40 shows the Oversampling of the Output Filter. This results in a reduction of the effective sampling frequency. The oversampling of the input does not affect the PPG sampling frequency. However, it results in an increased conversion time (T_ON). This oversampling output filter is called downsampling.

Figure 41:
PPG/ECG Digital Filter Configuration Submenu



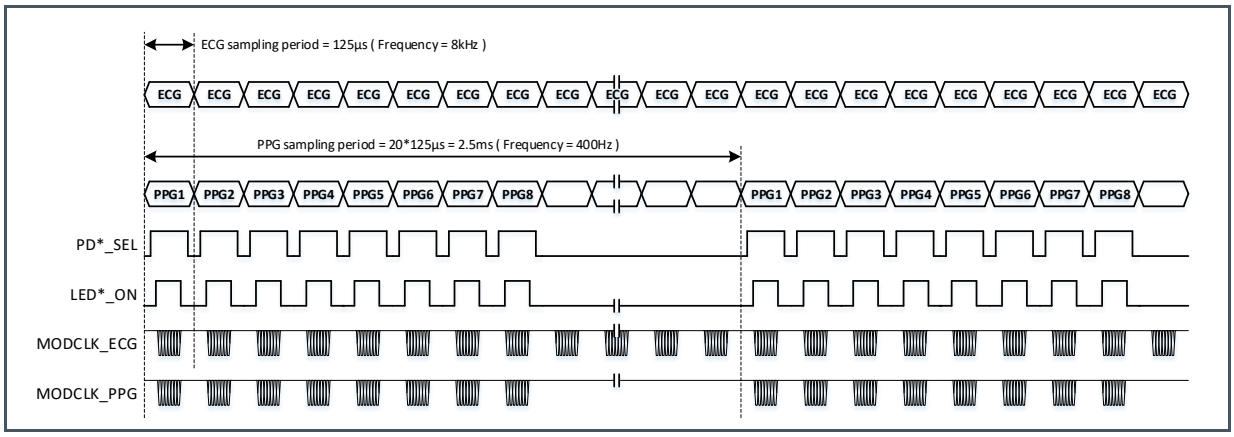
5.3.8 PPG/ECG Sequencer Configuration

Figure 42:
PPG Sequencer Settings

```
"seq": {
    "CGB_CFG": "0x07",
    "SEQ_SAMPLE": "0x64",
    "SEQ_PPGA": "0x02",
    "SEQ_PPGB": "0x00",
    "SEQ_MODE": "0x80"
},
```

- **cgb_cfg** (Address 0x38):
  A configuration for the internal clock generation block.
- **seq_sample** (Address 0x40):
  Configures the PPG and ECG sampling rate.

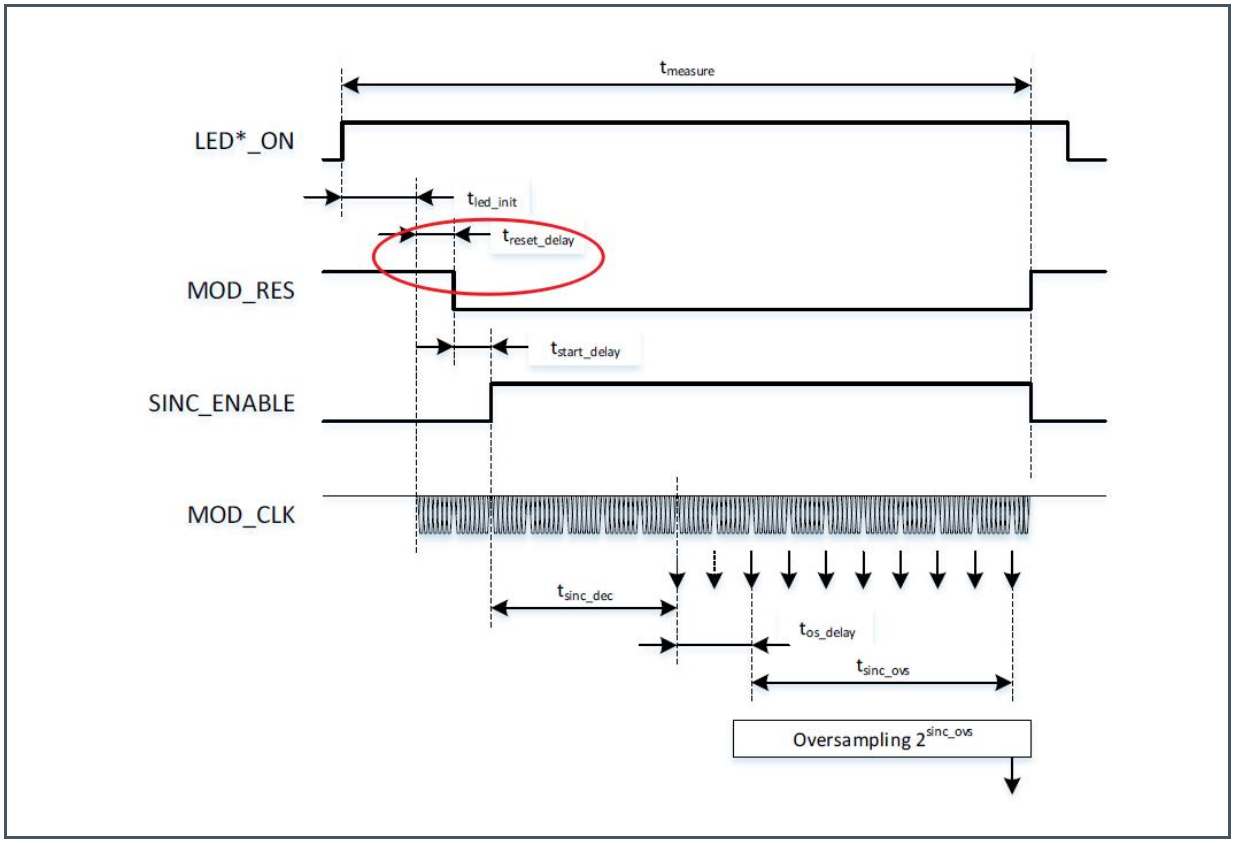
Figure 43:
ECG and PPG Sampling Rate



For more details please see the datasheet [1].

- **seq_ppga** (Address 0x41):
  Set the PPG/ECG reset delay.

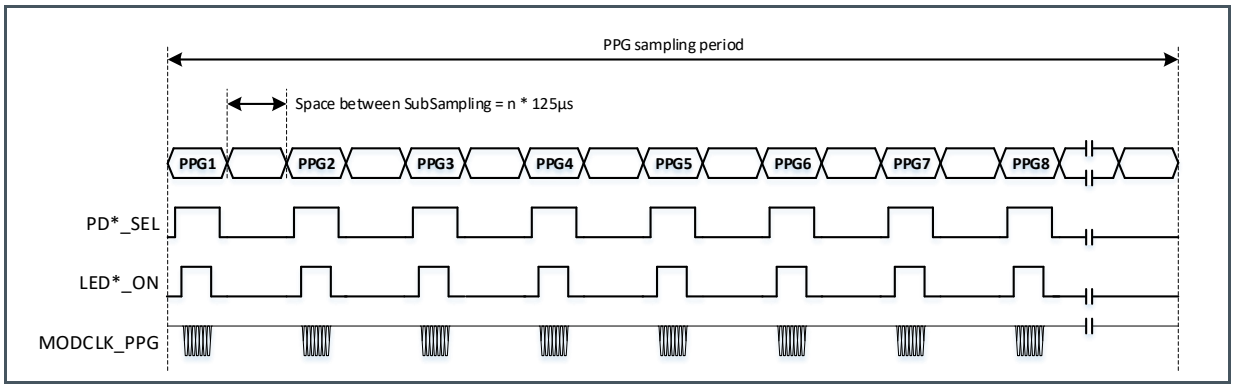
Figure 44:
Time of Reset Delay in One Measurement



ppg_sub_samples: Set the number of PPG subsamples = N+1.

- **seq_ppgb** (Address 0x42):
  Configures the distance between the PPG subsequences; N * 125µs

Figure 45:
Distance Between PPG Subsamples



- **seq_mode** (Address 0x59):
  A sequencer configuration register for PPG and ECG sampling modes.
  ppg_en: PPG enable. 1 = enable, 0 = disable.
  ppg_continous: 1 = continuously measure PPG, 0 = disable.
  ppg_after_ecg: set PPG and ECG to start at the same time or set PPG after ECG.

Figure 46:
ECG and PPG Simultaneous Sample Period

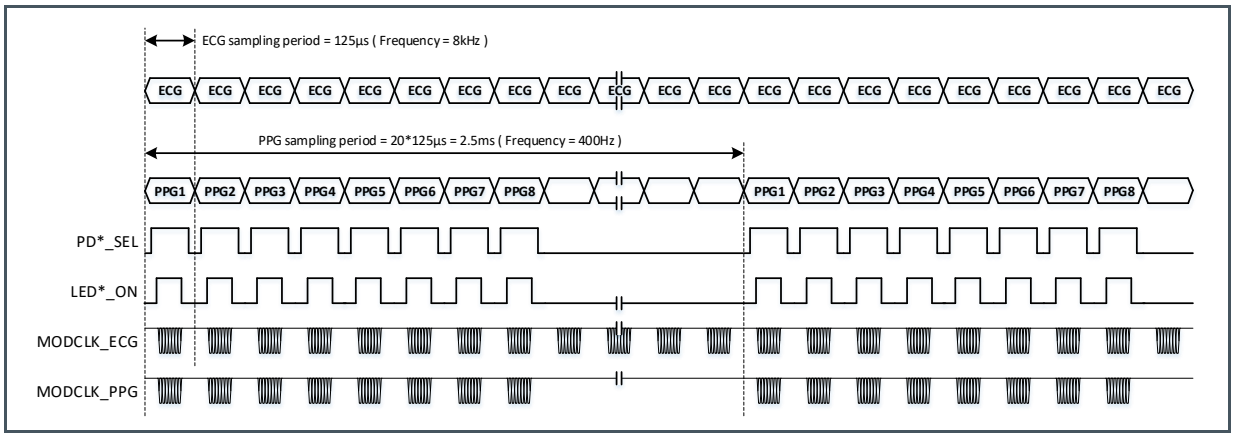


Figure 47:
ECG and PPG Shifted Sample Period

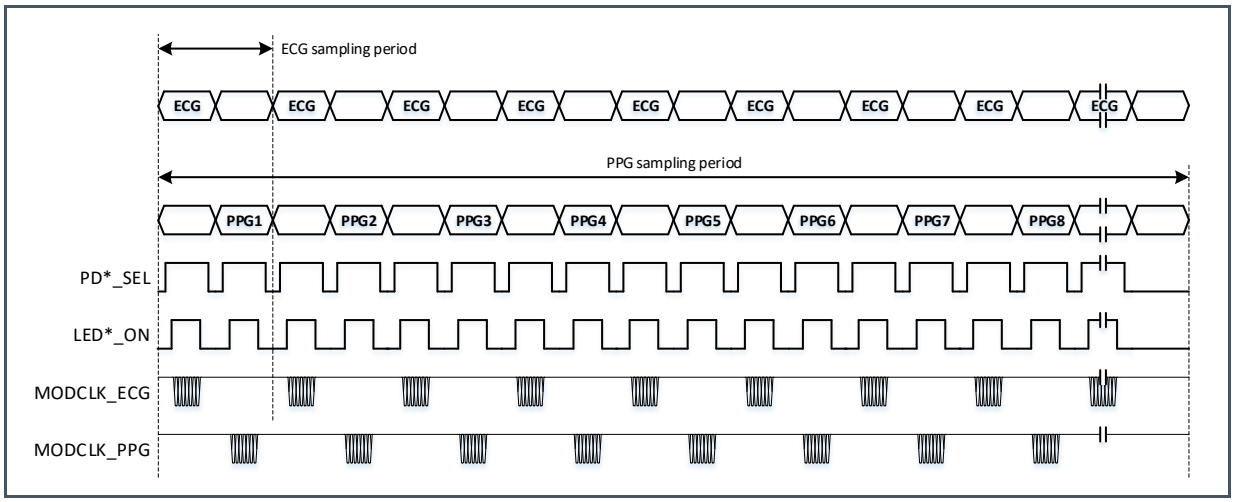
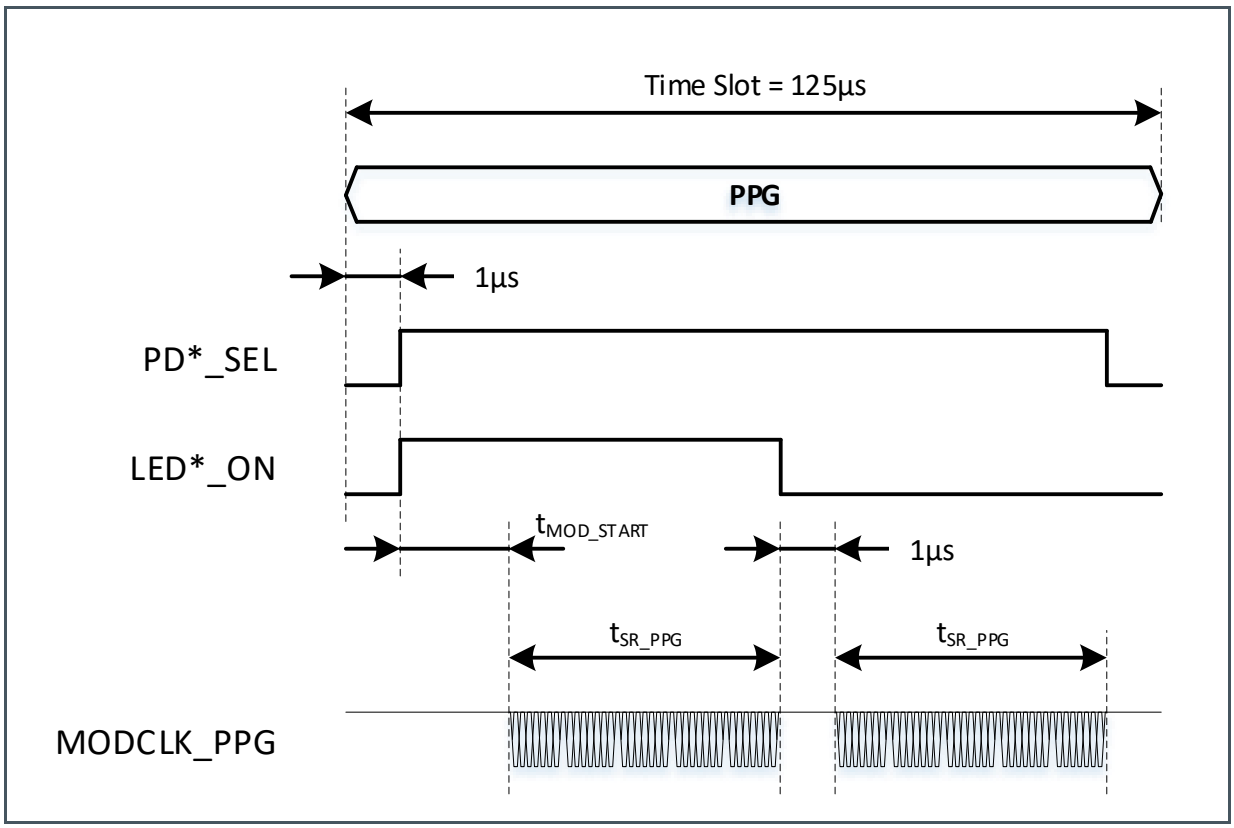


Figure 48:
PPG Double Sampling



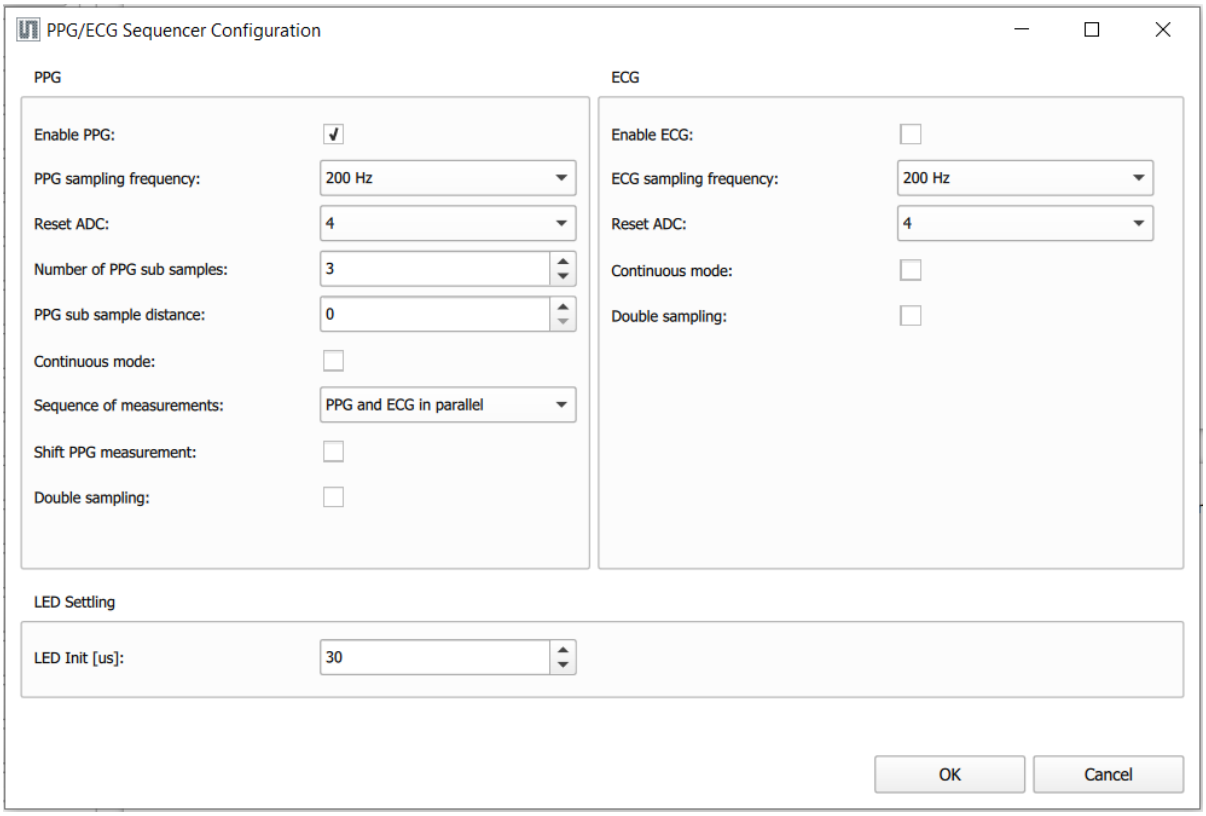
ppg_double: 1 = enable double measurements; 0 = single measurement

Double measurements will measure LED_ON and LED_OFF. Get the difference between these two measurements, and push to FIFO. This is used to cancel ambient light during the measurements.

Single measurements only measure one LED_ON.

These PPG sequencer settings can be found in the GUI under the “PPG/ECG sequencer” sub-menu.

Figure 49:
PPG ECG Sequencer Configuration Submenu



5.3.9 Notch Filter

Figure 50:
Notch Filter Configuration in the JSON File

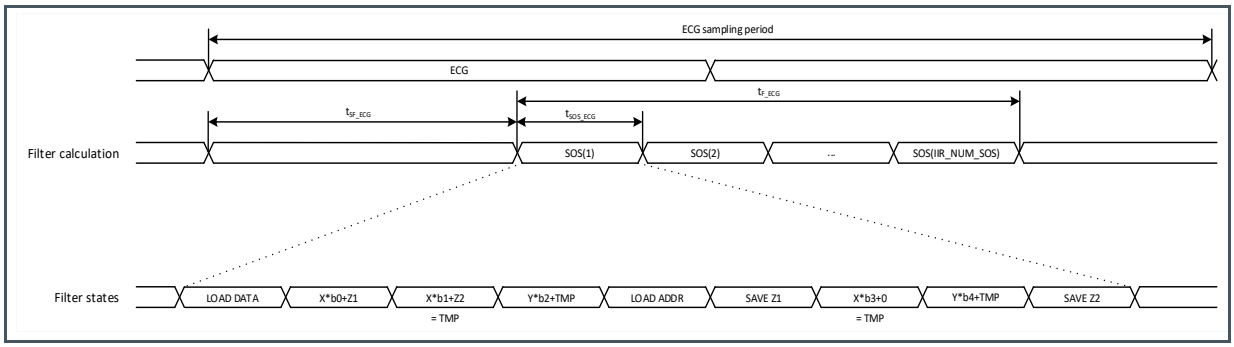
An Infinite Impulse Response (IIR) filter, with the parameter in Figure 51, is used to realize the notch filter functionality. The IIR filter is implemented sequentially as a second-order transposed Direct-Form-II (DF-II) structure (SOS). The IIR filter can be configured as a higher-order filter up to 24th order, based on an SOS structure (maximum 12th cascaded SOS structures). It is possible to implement other filters by reprogramming the filter coefficients. It uses two's complement for math operations.

The clock frequency should be 10 MHz.

Figure 51:
IIR Filter Parameter

Parameter	Value
MAX_NUM_OF_SOS =	12
SAMPLE_BIT_WIDTH =	21
COEFF_BIT_WIDTH =	16
SCALE_SHIFT =	14
RAM_WIDTH =	8

Figure 52:
Notch Filter Timing Diagram

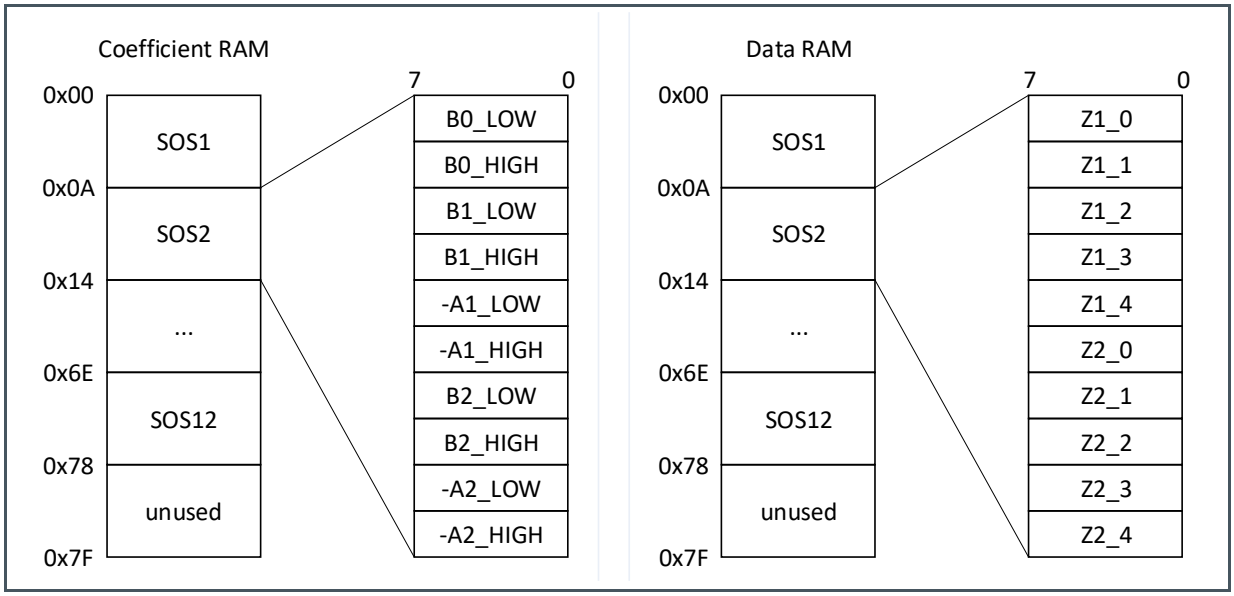


$t_{SF\_ECG} = t_{SD\_ECG} + t_{DV\_ECG} + t_{OS\_ECG}$

$t_{SOS\_ECG} = t_{MODCLK\_ECG} * 51$

$t_{F\_ECG} = IIR\_NUM\_SOS * t_{SOS\_ECG}$

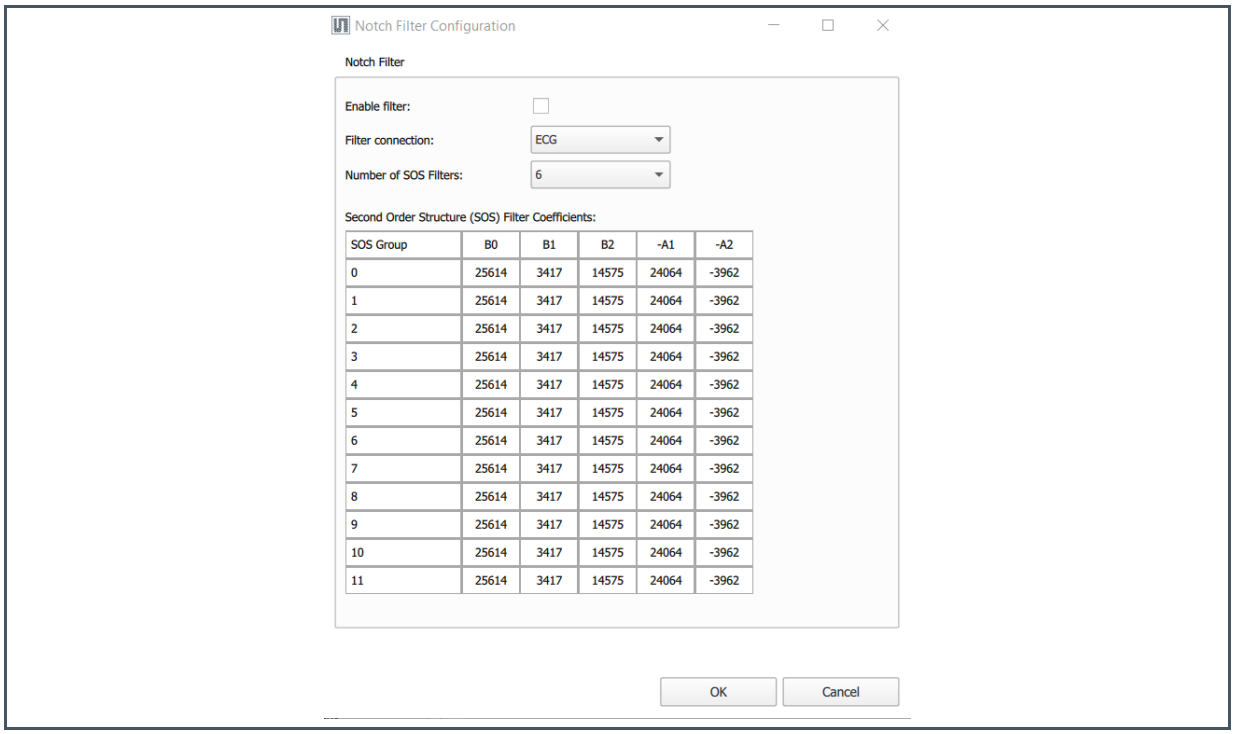
Figure 53:
Memory Map of Filter Parameters and Data



IIR_CFG (Address 0x61):

- Enable Notch Filter or IIR filter.
- IIR filter connection – PPG or ECG.
- IIR filter number of cascaded SOS structures.

Figure 54:
Notch Filter Configuration



SOS Group	B0	B1	B2	-A1	-A2
0	25614	3417	14575	24064	-3962
1	25614	3417	14575	24064	-3962
2	25614	3417	14575	24064	-3962
3	25614	3417	14575	24064	-3962
4	25614	3417	14575	24064	-3962
5	25614	3417	14575	24064	-3962
6	25614	3417	14575	24064	-3962
7	25614	3417	14575	24064	-3962
8	25614	3417	14575	24064	-3962
9	25614	3417	14575	24064	-3962
10	25614	3417	14575	24064	-3962
11	25614	3417	14575	24064	-3962

5.3.10 FIFO Control

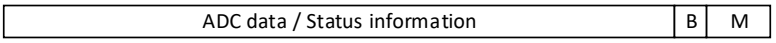
Figure 55:
FIFO Control in the JSON File

```
"fifo": {
    "FIFO_CTRL": "0x00",
    "FIFO_THRESHOLD": "0x17"
},
```

Figure 56:
FIFO Data Structure and Organization

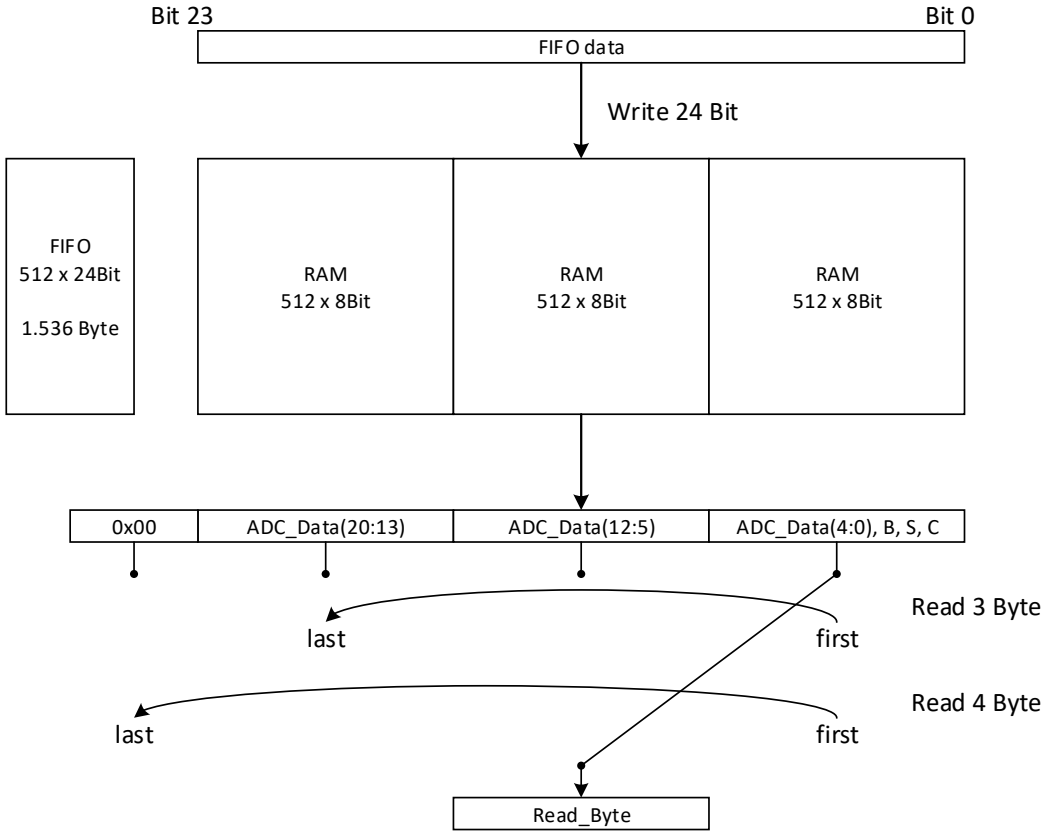
Format FIFO data when programming sample frequency

Block frame	1 Bit
Data marker	2 Bit
ADC data	21 Bit



Data marker 2 Bits

00 – ADC data PPG2...8
01 – ADC data ECG
10 – ADC data PPG1
11 – additional Status information (Sub addressing possible)



FIFO RAM Structure

RAM block	Number of RAMs	Number N	FIFO size
128 x 8 Bit	12	512	1.536 Byte

The AS7050 FIFO is 1536 bytes long. ADC samples are 3/4 bytes, which means the FIFO can hold up to 512 samples. There is a FIFO length register, which indicates how many samples are currently available in the FIFO. The FIFO can send an interrupt when the number of available samples reaches a certain configurable threshold.

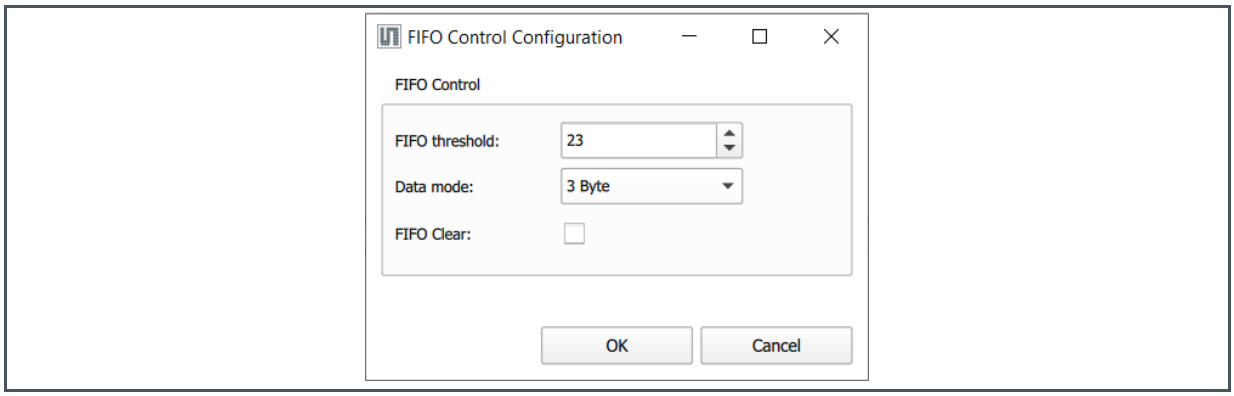
FIFO_CTRL (Address 0x75):

- FIFO Threshold configuration.
- FIFO Burst Length can be set.
- FIFO clear.

FIFO_THRESHOLD (Address 0x76):

- FIFO Threshold configuration.

Figure 57:
FIFO Control Configuration Submodule



5.3.11 Analog Frontend

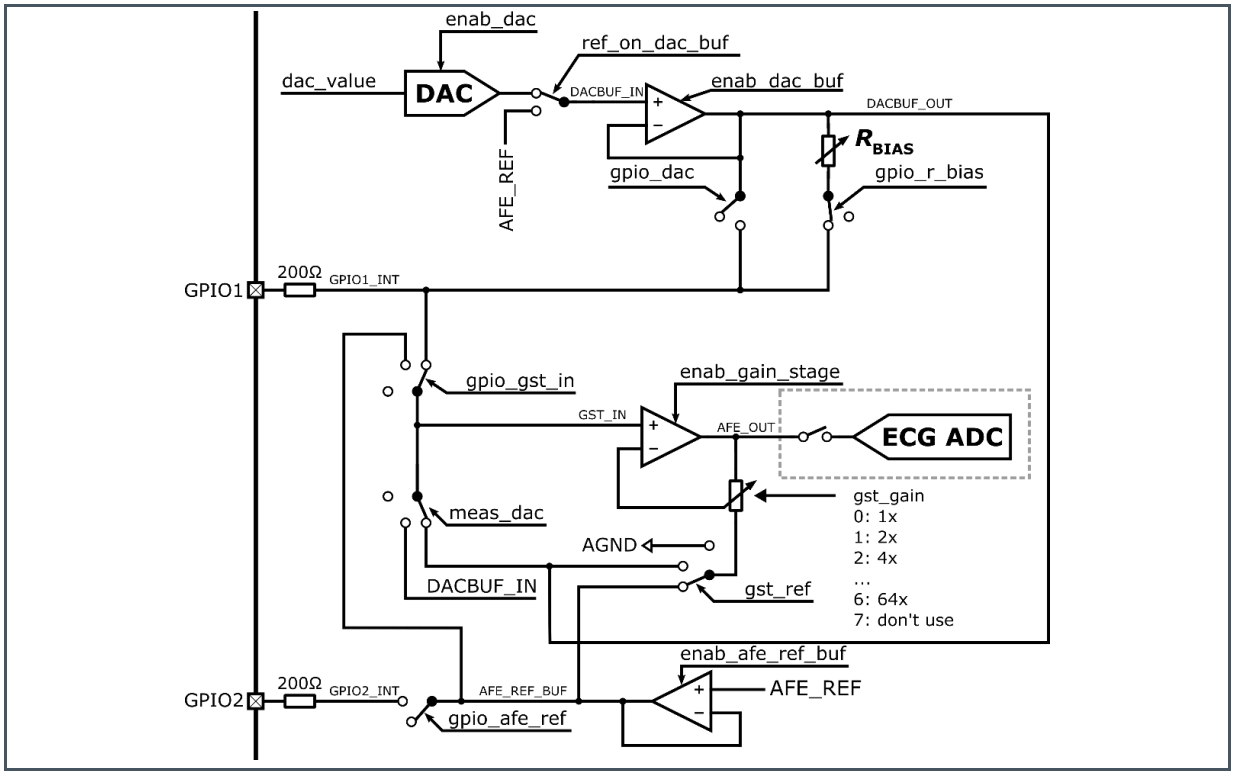
Figure 58:
Analog Frontend Configuration

```
"afe": {
    "AFE_DAC0L": "0x00",
    "AFE_DAC1L": "0x00",
    "AFE_DACH": "0x00",
    "AFE_CFGA": "0x00",
    "AFE_CFGB": "0x00",
    "AFE_GSR": "0x00"
},
```

The main purpose of the AFE is to measure the galvanic skin resistivity (GSR) via the two GPIOs. The two general-purpose pins, GPIO1 and GPIO2, can be used either as configurable GPIO pins or as analog input pins for the analog frontend beside the LED driver function. The electrical analog frontend

consists of two signal paths with dedicated functions. The analog inputs can be configured to set up different amplifier topologies. All the AFE functions are controlled by the digital part and work independently from each other.

Figure 59:
Analog Frontend



AFE_DAC0L (Address 0x32): Set the DAC0 value (0 - 1023).

AFE_DAC1L (Address 0x33): Set the DAC1 value (0 - 1023).

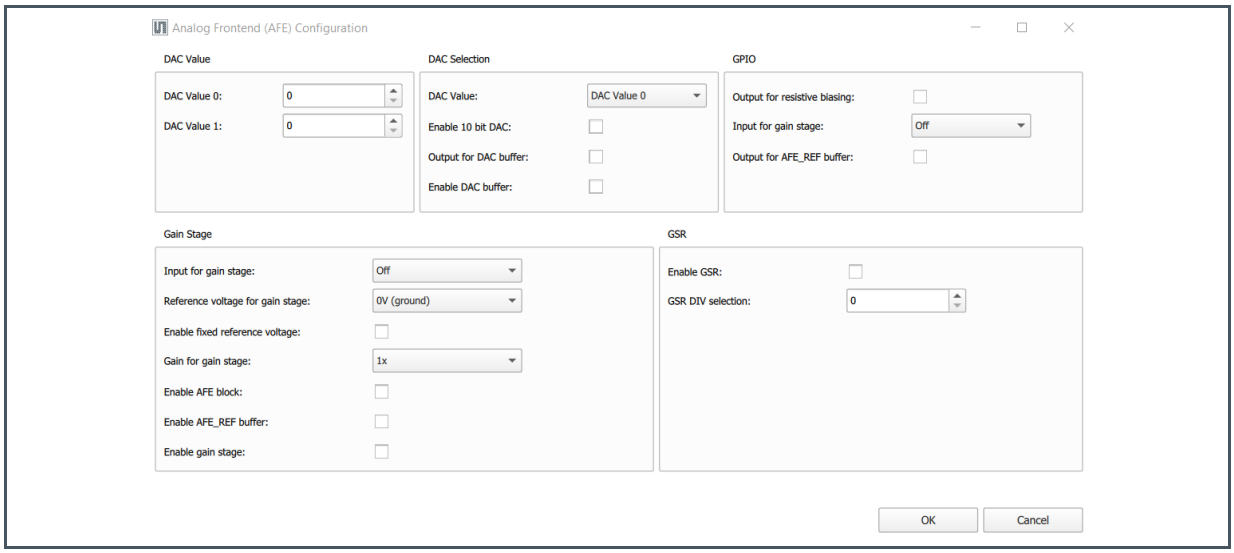
AFE_DACH (Address 0x34): Select the DAC0/1, enable the signal for 10bit, and enable the DAC buffer.

AFE_DACH (Address 0x3A): Enable the GSR and GSR DAC divider factor for switching between DAC1 and DAC2 values.

AFE_DACH (Address 0x35): Select the input gain stage and the DAC output as an input gain stage. Select the reference voltage at the gain stage, and select the output resistor biasing.

AFE_DACH (Address 0x36): Enable a fixed reference voltage on the DAC buffer, select the gain of the gain stage, enable the signal for the AFE block, AFE reference block, and the gain stage.

Figure 60:
AFE Configuration Submenu



5.3.12 GPIO

GPIO pins can be digitally controlled and have pull up/down enabled. They can also be used as analog input/output pins for the LED driver and GSR.

Figure 61:
GPIO Pin Configuration in the JSON File

```
"gpio": {
    "GPIO1_CFG": "0x00",
    "GPIO2_CFG": "0x00",
    "GPIO1_CFGB": "0x00",
    "GPIO2_CFGB": "0x00",
    "GPIO_IO": "0x00"
},
```

GPIO1_CFG (Address 0x10)/**GPIO2_CFG** (Address 0x11):

- Enable E2: Set the output driver strength to 2x (in the range of VDD to GND).
- Enable E4: Set the output driver strength to 4x (in the range of VDD to GND).
- Enable SR: Slightly adapt the output driver's slew rate to a better value (in the range of VDD to GND).
- Enable pull-up: Activate the pull-up current at the IO pin (pull-up in the range of VDD to GND).
- Enable pull-down: Activate the pull-down current at the IO pin (pull-down in the range of VDD to GND).

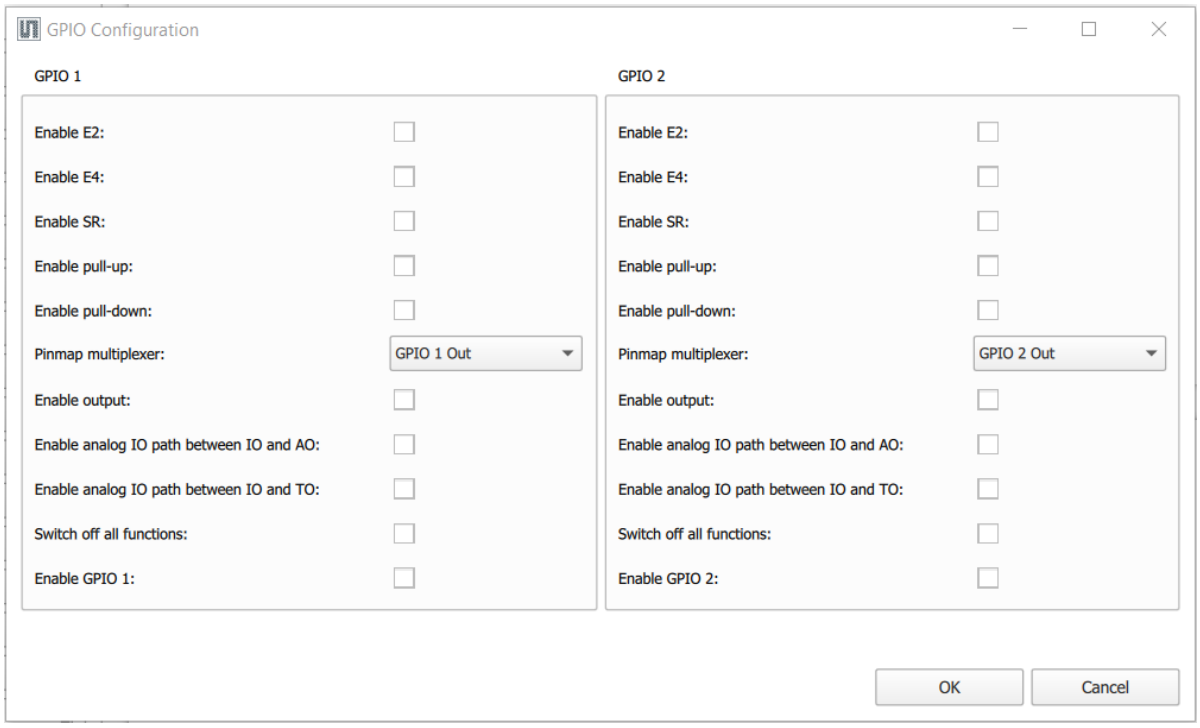
GPIO1_CFGB (Address 0x15)/**GPIO2_CFGB** (Address 0x16):

- Pinmap Multiplexer: Select GPIO1/2 as the output.
- Enable Output: 1 = enable output; 0 = disable output.

- Enable analog IO path between IO and AO: Switch on the analog IO path between IO and AO, and is in the range of VDD to GND.
- Enable analog IO path between IO and TO: Switch on the analog IO path between IO and TO, and is in the range of VDD to GND.
- Switch off all functions: To switch off input Schmitt-Trigger in case the LDE driver is on. (It is recommended to disable other apart as well).

GPIO_IO (Address 0x8F): `Bit 0 = GPIO1 Enable, Bit 1 = GPIO2 Enable`

Figure 62:
GPIO Configuration Submenu



5.3.13 Reference Block

Figure 63:
Reference Block in the JSON File

```
"ref": {
    "REF_CFGA": "0xAC",
    "REF_CFGB": "0x02"
},
```

This reference block supports two modes for the external load conditions. In the normal operational mode, the external capacitors on the reference voltage pads are set up to 2.2 µF. Thus, the bandwidth

of the reference block is limited to a low frequency range, due to the external capacitor. In the following subsections, this mode is called “slow mode”. The signal path of this mode is called “slow path”. In another newly developed testing mode, those voltage pads are completely open. With no external capacitors, the bandwidth of the reference block reaches a relatively high frequency. Thus, this mode is called “fast mode” with a signal path called “fast path”. For these two modes, the buffer utilizes two different operational amplifiers (OpAmps) and switches.

The reference block generates two types of bias currents (1 µA and 10 µA) with a light positive temperature coefficient. Please note that the bias current (1 µA) is designed exclusively for the PPG channel and other blocks since the PPG channel requires isolation from other noise-sensitive blocks.

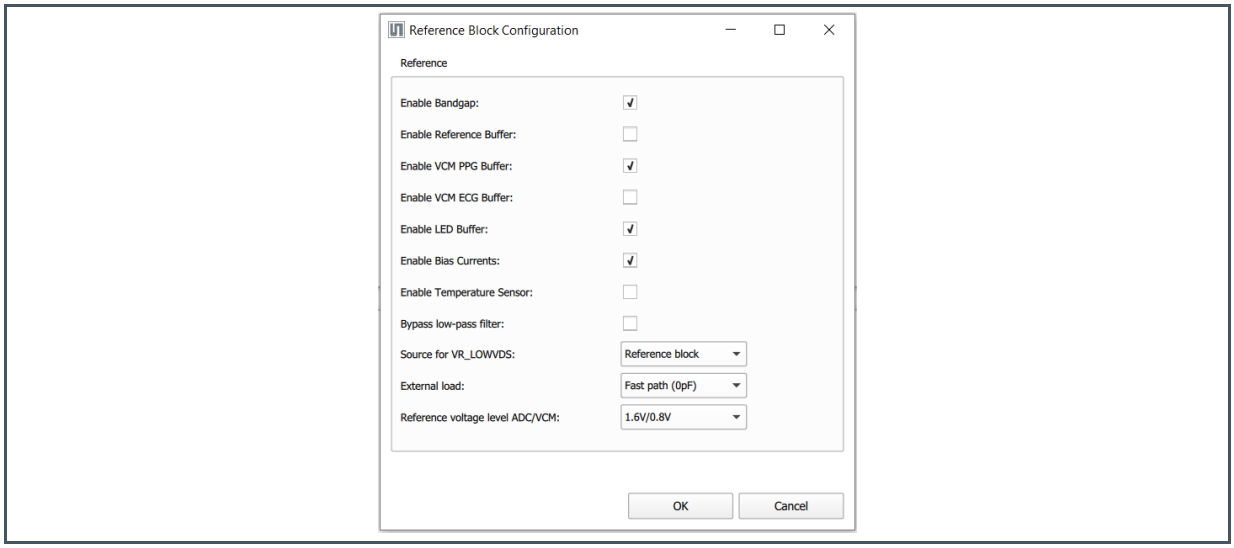
REF_CFGA (Address 0x30):

- Enable Bandgap: Digital input interface to enable the bandgap.
- Enable Reference Buffer: Enable the reference ADC buffer.
- Enable VCM PPG Buffer: Enable the common mode voltage reference (VCM) of the PPG buffer.
- Enable VCM ECG Buffer: Enable the common mode voltage reference (VCM) of the ECG buffer.
- Enable LED Buffer: Digital input interface to enable the LED buffer.
- Enable Bias Currents: Digital input interface to enable the bias currents.
- Enable Temperature Sensor: Digital input interface to enable the temperature sensor.
- Bypass Low-pass filter: Bypass of the low-pass filter for the bandgap voltage.

REF_CFGB (Address 0x31):

- Source for VR_LOWVDS: 0=use from reference block; 1=use external load.
- External Load: 0= external load 2.2 pF (slow path); 1=external load 0pF (fast path).
- Reference voltage level ADC/VCM: Select - 0= 1.6 V/0.8 V; 1=1.5 V/0.75 V.

Figure 64:
Reference Block Configuration Submenu



5.3.14 Power Management

Figure 65:
Power Management in the JSON File

```
"standby": {
    "STANDBY_CFGA": "0x35",
    "STANDBY_CFGB": "0x01"
},
```

Power Management aims to minimize power consumption. The standby registers are part of the AS7050 power management to reduce the power consumption of the AS7050 and the measurement system itself. Also, during continuous measurements, blocks such as modulators, clock generation, reference block, or ECG can switch to standby mode between the several PPG and/or ECG sample slots if they are inactive. For usage of the standby functionality, the dedicated registers have to be activated. In the standard default setting, the automatic standby is disabled. That means all the blocks are always active as long as no standby is activated. Depending on the programmed sequences, the blocks automatically switch on standby.

It is recommended to only use this feature for PPG and TIA + ECG Modulator measurements.

For all measurements with the ECG amplifier and AFE, this feature should not be used.

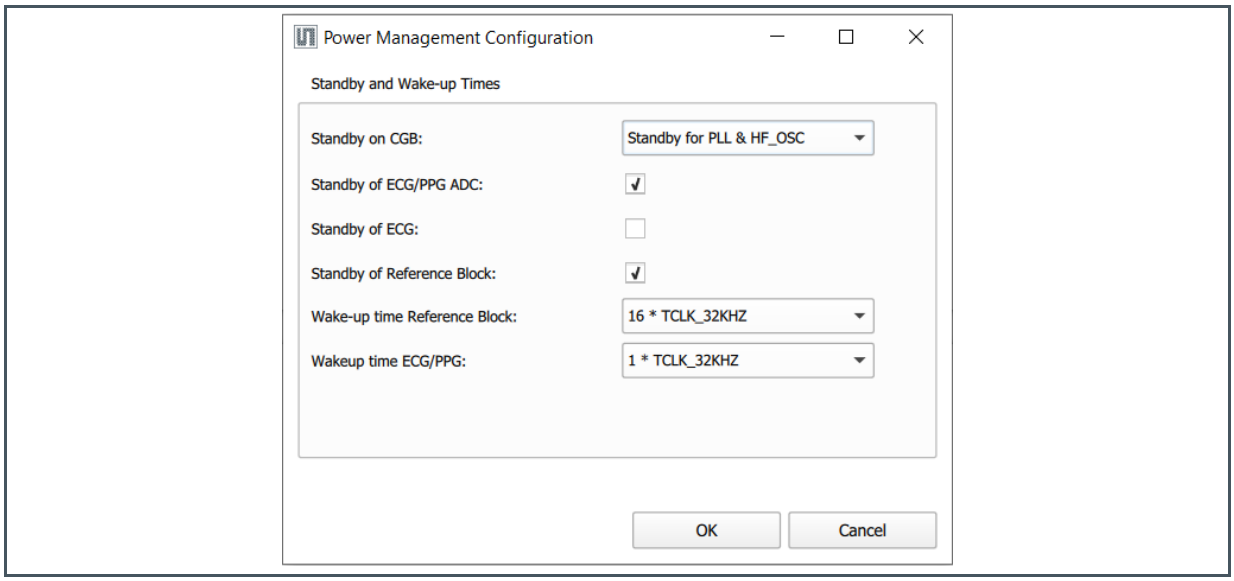
STANDBY_CFGA (Address 0xB0):

- Standby on CGB (Clock Generation Block): Select standby on CGB
  - Standby for PLL
  - Standby for HR_OSC
- Standby of ECG/PPG ADC: Select standby for ECG/PPG Modulator.
- Standby of ECG: Enables standby for ECG.
- Standby of Reference Block: Enables standby for the Reference block.

STANDBY_CFGB (Address 0xB1):

- Wake-up up time Reference Block: Select wake-up time Reference Block.
- Wakeup time ECG/PPG: Select wake-up time for ECG/PPG modulator.

Figure 66:
Power Management Configuration Submodule



5.3.15 Clock Generation Block

Figure 67:
Clock Generation Configuration in the JSON File

```
"seq": {
    "CGB_CFG": "0x07",
```

The clock reference block provides three clock frequencies needed for the system. They are 32 kHz, 2 MHz, and 20 MHz. The 32 kHz is always active, whilst the 2 MHz and 20 MHz are active when needed.

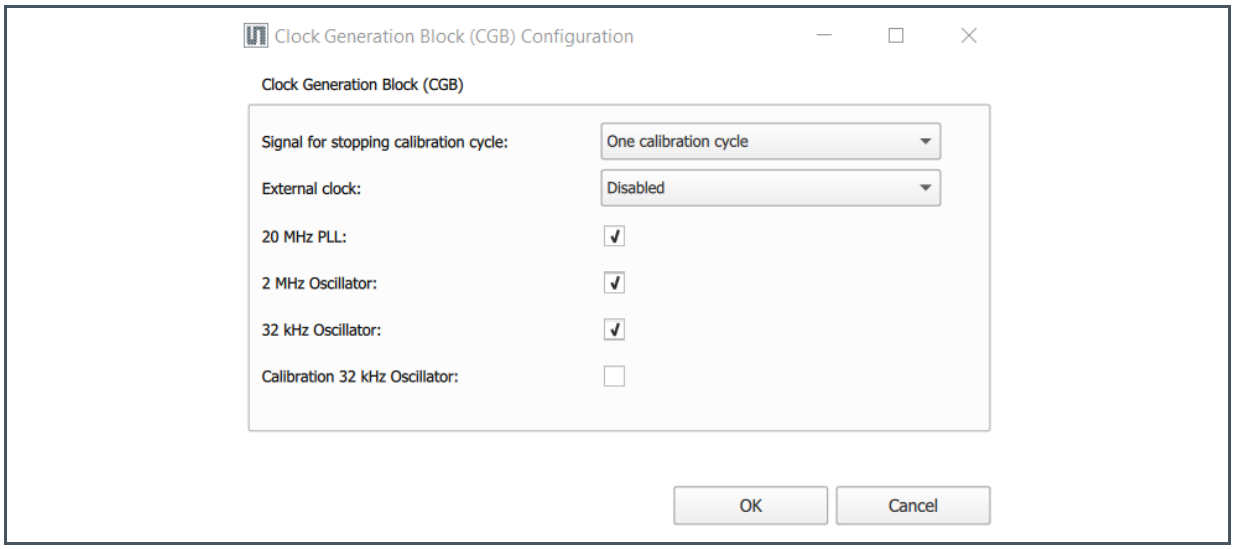
The 32 kHz low frequency clock is always active to enable low power consumption over the whole time. It is needed by the digital part to generate the time basis for the sampling windows.

The low frequency clock is recalibrated from time to time to achieve the needed accuracy. The calibration is done in the clock generation block (CGB).

The 2 MHz high-frequency oscillator is used as a clock basis for the PLL and recalibration of the low frequency clock. The activity is controlled by the digital core.

The 20 MHz PLL clock is used for the modulators and is the highest frequency available in the system. It runs together with the high-frequency oscillator and is enabled on demand by the digital core.

Figure 68:
Clock Generation Block Configuration Submenu



5.3.16 LDO and I²C

Figure 69:
JSON File for the LDO and I²C Configuration

```
"ctrl": {
    "CONTROL": "0x01"
},
```

LDO for VDDA:

The integrated LDO generates the 1.8 V power supply for all internal blocks from an external voltage. It uses an external blocking capacitor typically of 1 µF. For digital and analog supply voltage generation, two independent LDOs are used.

The LDO for VDD (digital power supply) is switchable by the pin LDO_EN (LDO Enable). The LDO for VDDA (analog power supply) is switchable only by the internal register value and only if the LDO for VDD is active.

Information

If a valid internal LDO should be used, $V_{LDO} = V_{DD}$ = 2.3 V…5.5 V (typ. 3.3 V); LDO_EN > 1.26 V

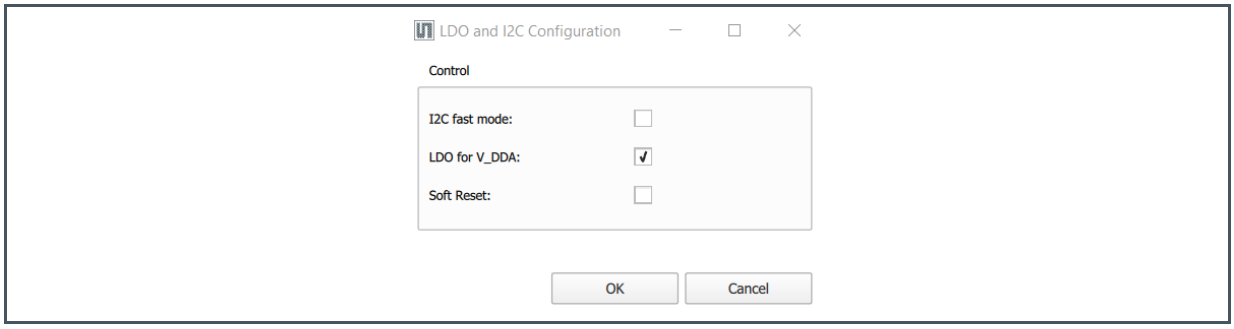
If a valid external LDO power supply should be used, $V_{LDO} = V_{DD}$ = 1.8 V; LDO_EN < 0.56 V

I²C Fast Mode:

Enable I²C fast mode with 1 MHz. By enabling this function, the internal clock will be switched to 1 MHz from the standard 100 kHz or 400 KHz in the fast mode.

Soft Reset: Resets the software. The reset has the same effect as power on reset.

Figure 70:
LDO and I²C Configuration Submenu



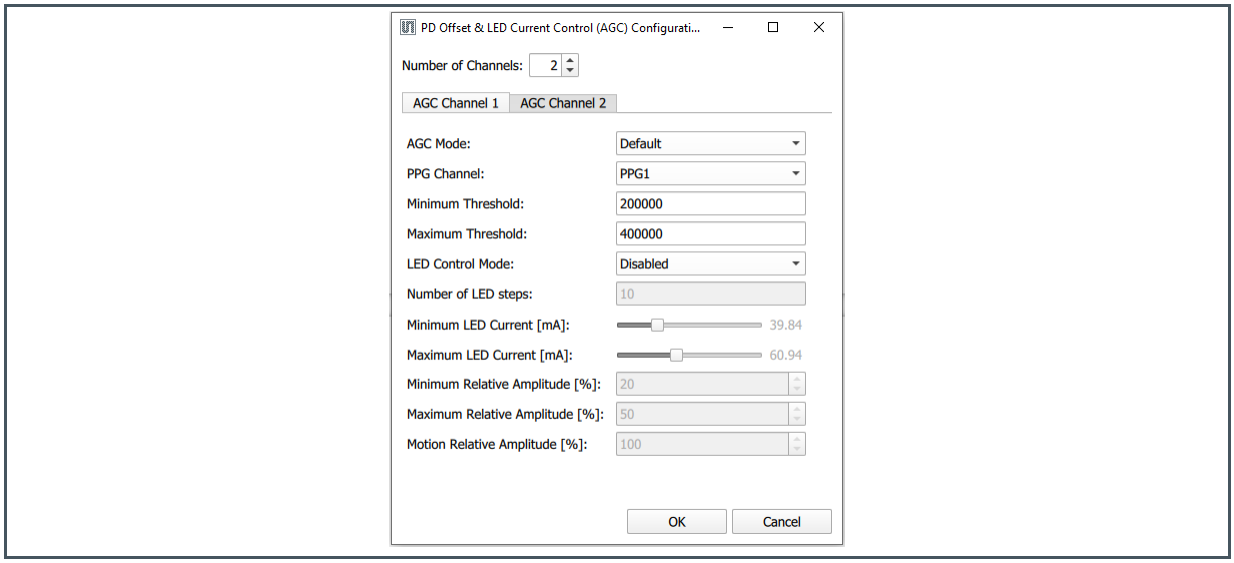
5.3.17 PD Offset & LED Current Control

Figure 71:
AGC Configuration JSON File


```
"agc": [
    {
        "agc_mode": 0,
        "led_control_mode": 0,
        "ppg_channel": 1,
        "led_current_min": 33,
        "led_current_max": 51,
        "rel_amplitude_min": 20,
        "rel_amplitude_max": 50,
        "rel_amplitude_motion": 100,
        "num_led_steps": 10,
        "threshold_min": 200000,
        "threshold_max": 400000
    },
    {
        "agc_mode": 0,
        "led_control_mode": 0,
        "ppg_channel": 2,
        "led_current_min": 20,
        "led_current_max": 34,
        "rel_amplitude_min": 20,
        "rel_amplitude_max": 50,
        "rel_amplitude_motion": 100,
        "num_led_steps": 10,
        "threshold_min": 200000,
        "threshold_max": 400000
    }
```

The PD offset and LED current control is an algorithmic approach to increase the signal quality of the PPG signals. The algorithm continuously monitors the ADC outputs and, if necessary, reconfigures the AS7050 while measuring to ensure ideal conditions.

Figure 72:
PD Offset & LED Current Control Submenu



The firmware supports up to four AGC instances, each running independently. Thus each AGC instance controls a single PPG channel, up to eight different PPG channels can be controlled by the AGC.

The AGC attempts to keep the PPG signal within a configured range by only controlling the PD offset. It is also possible to enable the control mode of the PPG amplitude. When enabled, the AGC attempts to keep the PPG amplitude within a configured range by controlling the current of the LEDs assigned to that PPG channel.

Automatic Gain Control (AGC) Mode: Enables the AGC algorithm for the channel.

PPG Channel: The PPG Signal is assigned to the AGC channel and is required when the channel is enabled.

Minimum/Maximum Threshold: The minimum or maximum threshold specifies the range in ADC counts to keep the PPG signal within.

LED Control Mode: PPG amplitude control can be disabled or enabled in automatic or external mode via the LED control mode. In Auto mode, amplitude control is performed by the AGC itself. In external mode, the LED current can be increased or decreased by an external algorithm, but this mode is not implemented yet.

Number of LED Steps: The number of LED steps specifies the number of LED current increments to step through the configured LED current range. This parameter determines the granularity/speed of the amplitude control. When the AGC algorithm determines that the LED current needs to be

increased or decreased, and the bounds of the LED current range are not yet reached, the LED current is adjusted by one step.

Minimum/Maximum LED Current [mA]: The minimum or maximum LED current limits the LED current output by the PPG amplitude control.

Configuration Notes - The minimum current should be low enough to keep the PPG amplitude within the configured amplitude range for high perfusion/bright skin tones. The maximum current should be high enough to keep the PPG amplitude within the configured amplitude range for low perfusion/dark skin tones.

Minimum/Maximum Relative Amplitude [%]: The minimum or maximum relative amplitude specifies the target PPG amplitude range, relative to the configured PPG range, in percent (in the example shown in Figure 72, the minimum PPG amplitude would be 200000 ADC counts and the maximum PPG amplitude would be 400000 ADC counts).

Configuration Notes - Consider the dynamic range of the use case signal and the PPG signal requirements of the vital sign algorithm being used. For use cases with strong motion artifacts, the PPG amplitude would typically be considered low, while for use cases with limited motion artifacts, the PPG amplitude could typically be considered high. The selected PPG amplitude range is related to the configured LED current range. The AGC algorithm tends to overestimate the PPG amplitude.

Motion Relative Amplitude [%]: The Motion Relative Amplitude sets the limit relative to the configured PPG range in percent. If the occurrences of the signal amplitudes are higher than the set value, then it is considered with motion artifacts and the PPG amplitude control does not adjust the LED current.

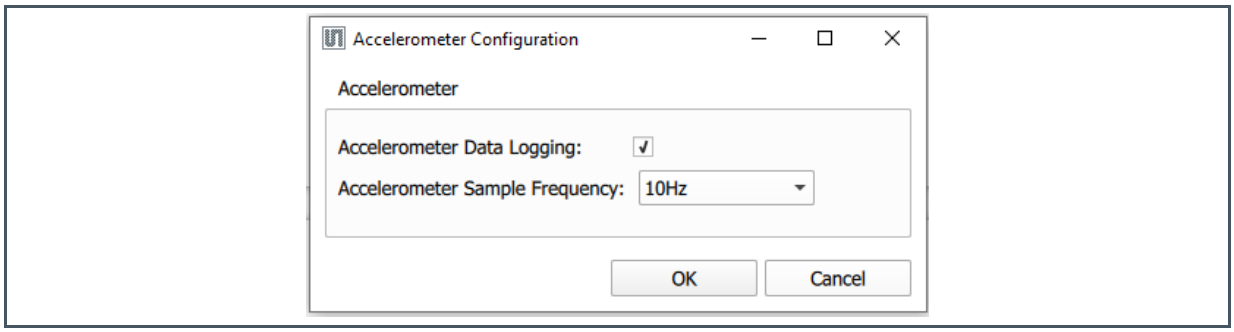
5.3.18 Accelerometer

Figure 73:
Accelerometer Configuration

```
"accelerometer": {
    "sample_rate": 10
},
```

The accelerometer is also activated when the HRM algorithm is selected. However, the accelerometer can be enabled and disabled via the user interface.

Figure 74:
Accelerometer

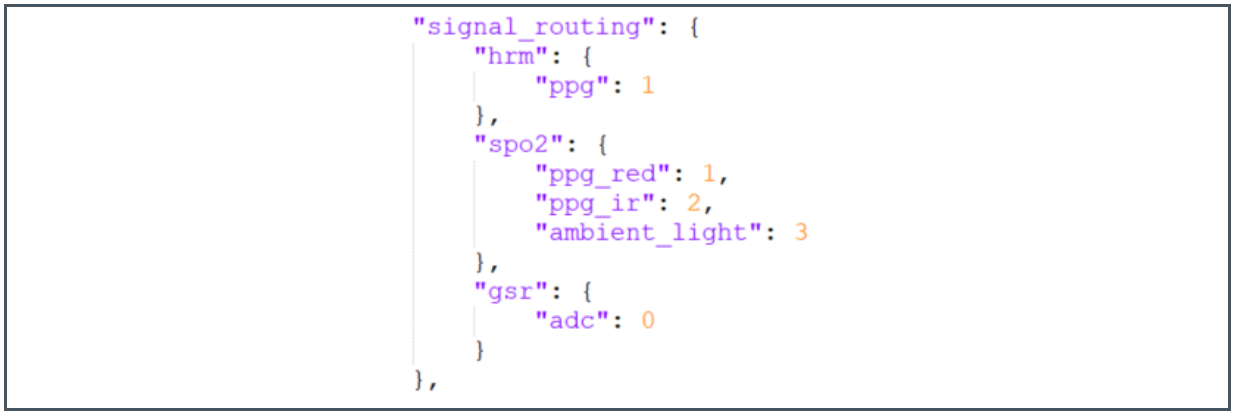


The accelerometer is used for displacement information. The HRM application includes this accelerometer data and makes the accelerometer useful and practical.

5.3.19 Application Settings

The “Application Settings” setting is located on the right-hand side of the evaluation software (Figure 9). This setting is mainly used to select and change the HRM, SpO2, and GSR configuration blocks and parameters.

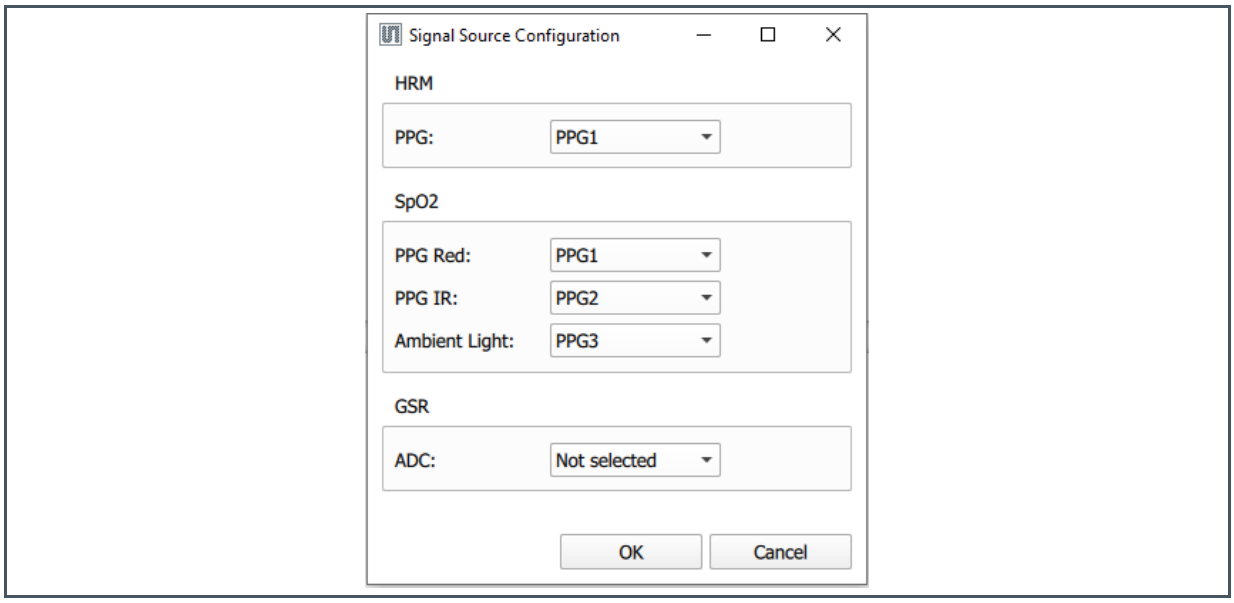
Figure 75:
Signal Routing Configuration



```
"signal_routing": {
    "hrm": {
        "ppg": 1
    },
    "spo2": {
        "ppg_red": 1,
        "ppg_ir": 2,
        "ambient_light": 3
    },
    "gsr": {
        "adc": 0
    }
},
```

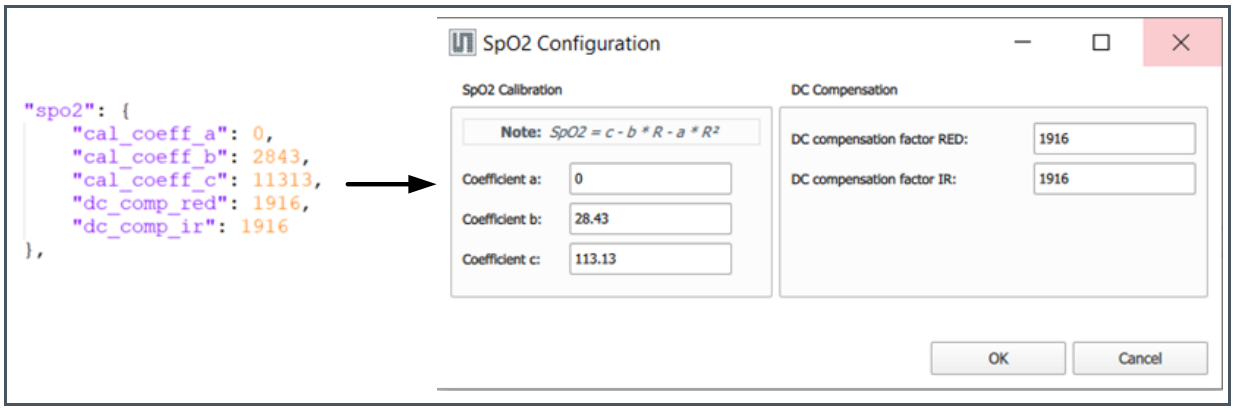
The “Signal Routing” window, which is a PPG signal source configuration and GSR signal routing, is used to select the HRM, SpO2, and GSR blocks, as shown in Figure 76.

Figure 76:
Signal Routing



"SpO2" is for configuring the SpO2 Parameters. Enter the parameters associated with the specific settings of the AS7050 in the SpO2 configuration settings. Due to production and assembly tolerances, it is recommended that the below-mentioned factors for the photodiode offset current compensation ($PD_{off\_fact\_red}$ and $PD_{off\_fact\_ir}$) are determined for the device under development; after the sensor has been integrated and the optical configuration is finalized.

Figure 77:
SpO2 Configuration



5.4 Galvanic Skin Resistance or Resistance Measurement

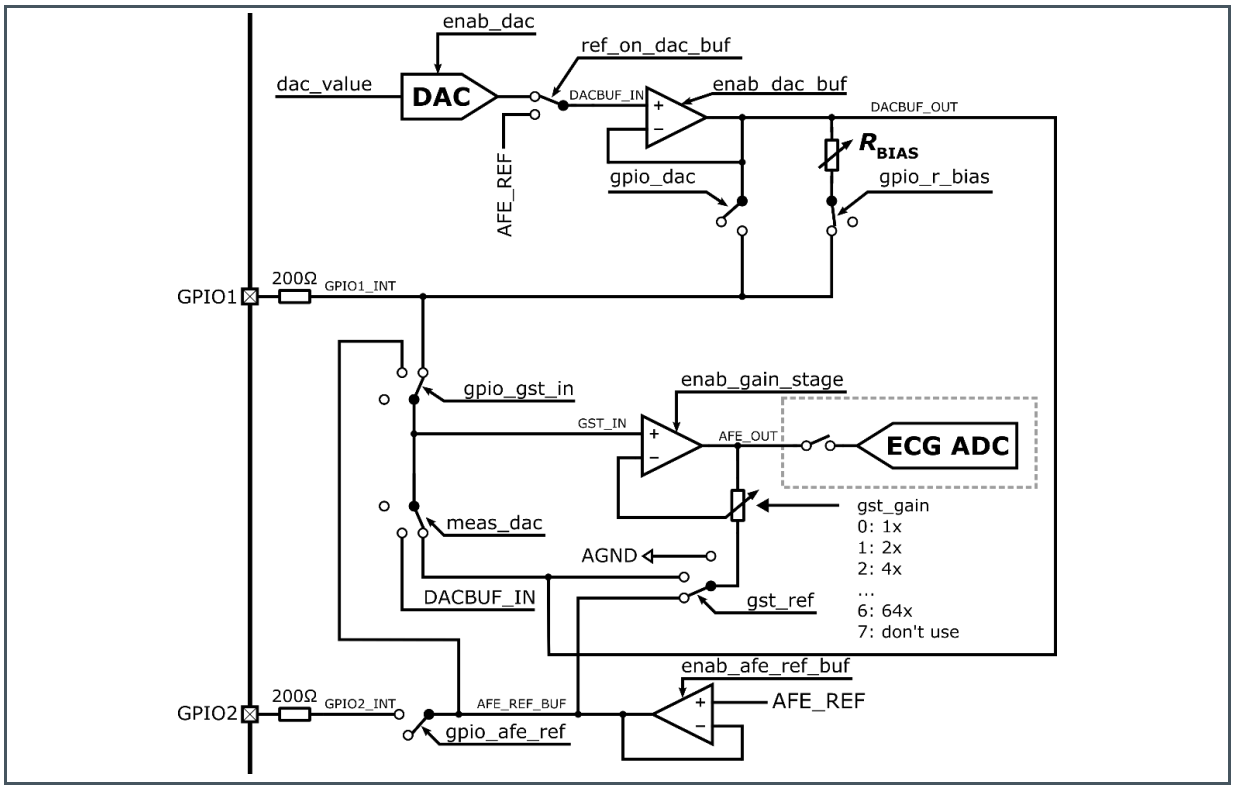
The AS7050 can be configured to measure the changes in a person's skin resistance, also called Galvanic Skin Resistance (GSR). GSR is a part of a set of measurements of electrical activity in the skin known as Electro-dermal activity (EDA). The impedance of the skin changes partially due to the amount of sweat and blood flow present in the skin.

The skin resistance is measured by applying a small stimulus through an electrode to one part of a person's skin and measuring the impedance from another part of the skin. The amount of change observed can vary, depending on where the electrodes are placed, due to variations in the density of sweat glands throughout the body. The palm contains up to 2000 sweat glands per square centimeter hence giving a convenient placement of electrodes on the fingers. Placing the electrodes on the wrist is also possible, but due to fewer sweat glands, the resistance is much higher as compared to the palm.

5.4.1 Analog Frontend for GSR

The two general-purpose pins, GPIO1 and GPIO2 can be used either as configurable GPIO pins or as analog input pins for the analog front-end beside the LED driver function. The electrical analog front-end consists of two signal paths with dedicated functions.

Figure 78:
Analog Front-End for GSR



For the Galvanic Skin Resistance (GSR) measurement, GPIO2 is set to the reference voltage for the AFE block (V_{AFEREF}), and the series connection of the buffered DAC Voltage (V_{DAC}), and the bias resistor (R_{Bias}) is applied to GPIO1. The DAC voltage is continuously modulated symmetrically around V_{AFEREF} with an amplitude of ΔV_{DAC} (symmetrical voltage difference between V_{DAC} and V_{AFEREF}) and a frequency of f_{SEL_DAC}.

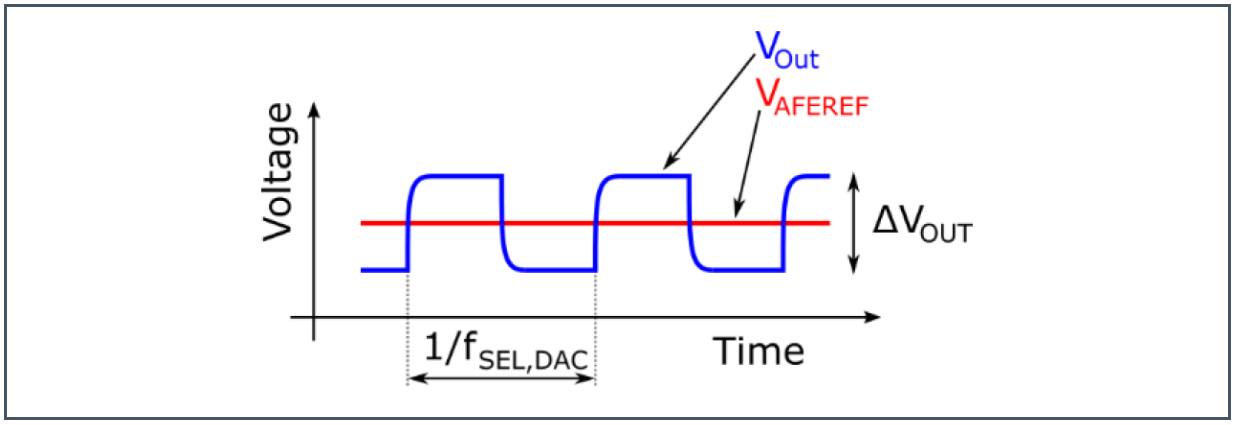
Subsequently, the voltage at GPIO2 is amplified in the gain stage with the gain G_{GST} and becomes the AFE output voltage V_{Out} (ΔV_{Out} = Peak-to-peak voltage of V_{Out}), which is digitized in the ECG ADC.

Out of ΔV_{Out}, the GSR can be calculated with the following formula:

Equation 1:

$$R_{GSR} = \frac{R_{Bias}}{\frac{2G_{GST}\ \Delta V_{DAC}}{\Delta V_{out}} - 1}$$

Figure 79:
AFE Waveforms to Measure the GSR



- The range of the resistor should be 10 kΩ to 4.7 MΩ.
- The maximum current flowing through the skin resistor is 500 µA.
- Voltage excitations of the skin should be sinus or square pulse with a frequency of 15 Hz.

5.4.2 Configuration on GSR Routines

Figure 80:
GSR Routines

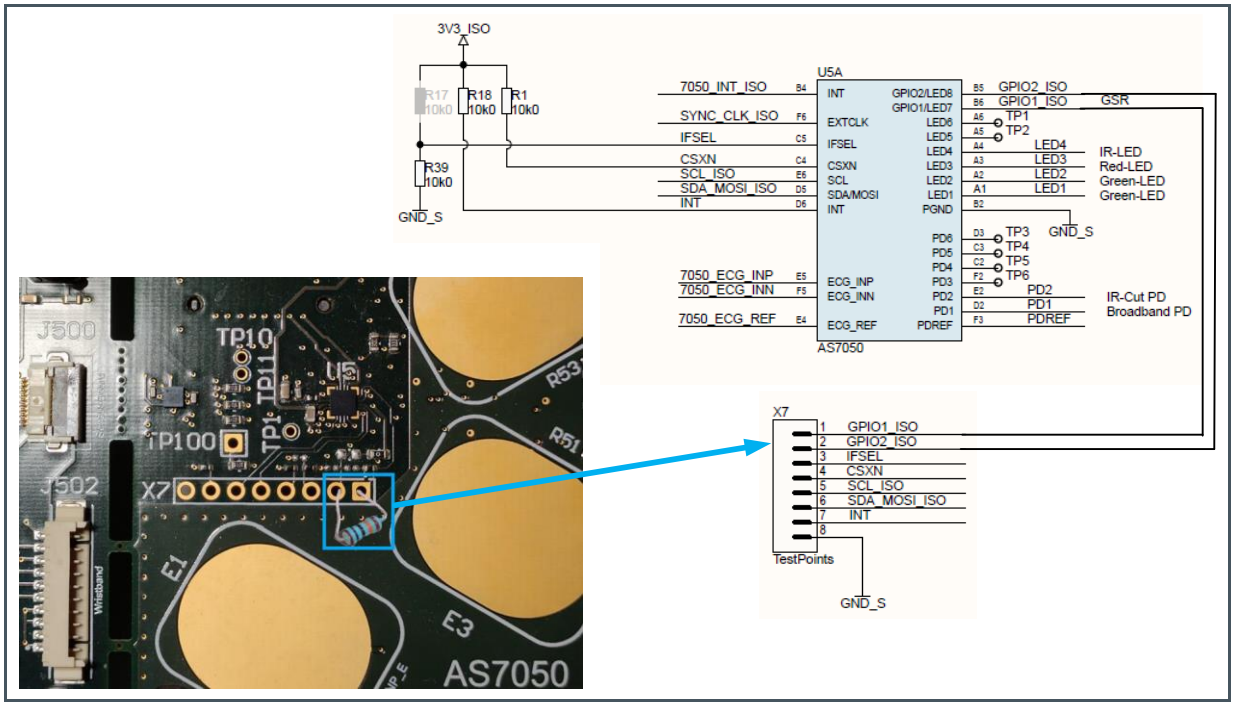
Signal Name	V_{DAC} Trim	R_{bias} Trim	GSR Measurement
AFE_meas_dac<1:0>	2	0	0
AFE_gst_ref<1:0>	2	0	1
Afe_gpio_r_bias	0	0 –> 1	1

Signal Name	V_{DAC} Trim	R_{bias} Trim	GSR Measurement
Afe_gpio_dac	0	1	0
AFE_gpio_gst_in<1:0>	1	1	1
AFE_gpio_afe_ref	1	1	1
AFE_gain<2:0>	1	1	1
AFE_ref_on_dac_buf	0	0	0
Enab_afe_ref_buf	1	1	1
enab_afe_lv	1	1	1
enab_gain_stage	1	1	1
enab_dac_buf	1	1	1
enab_dac	1	1	1

5.4.3 Resistance Measurement with the EVK via the GUI

The “ECG 25 Hz, GSR measurement” configuration preset is provided for the user to quickly start using the device. This can be chosen from the “Configuration Presets” Tab. This configuration file serves as an example to understand the GSR measurement. The resistor connected in Figure 81 is for demonstration purposes. Please prepare the EVK board and connect the resistor, of the desired value, to pins 1 and 2 of connector X7 (Figure 81).

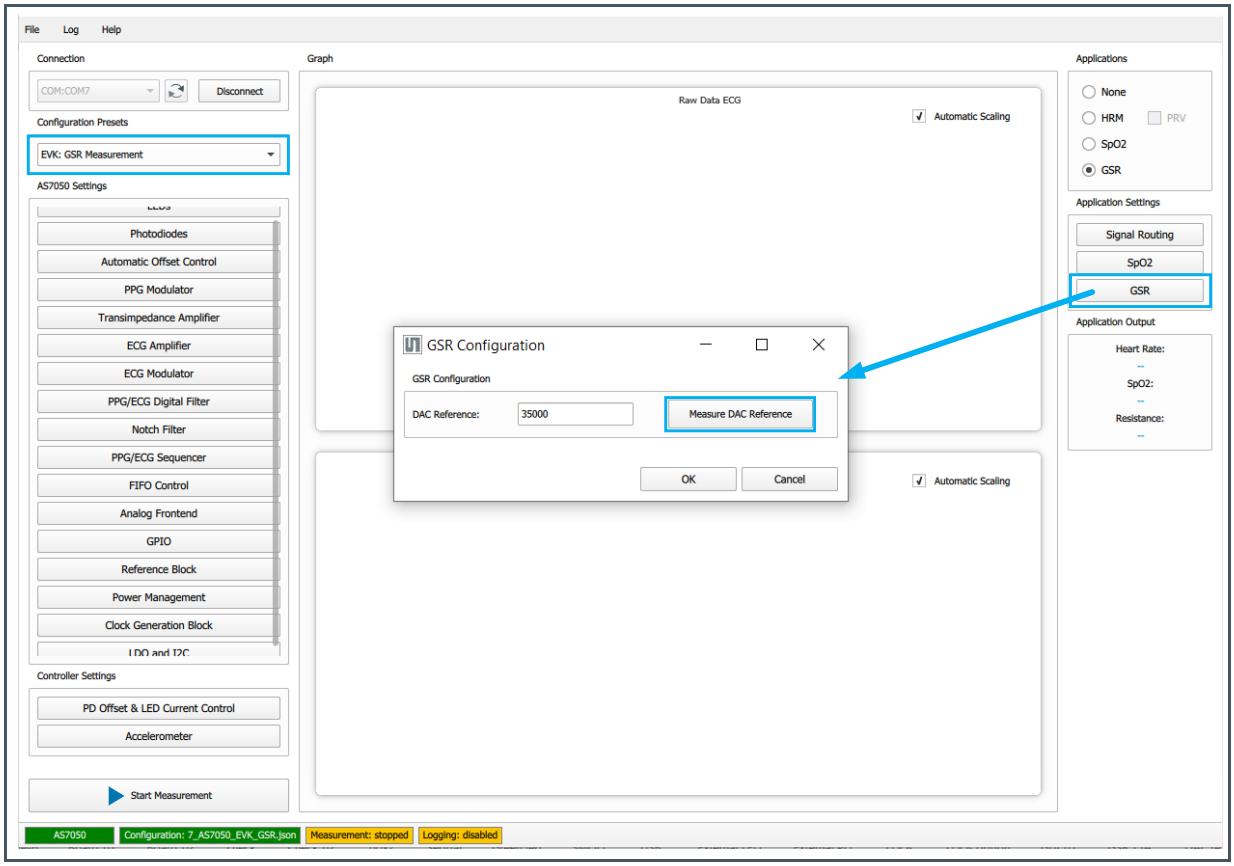
Figure 81:
Attaching 100 kOhm Resistor to the EVK Board



GSR Measurement

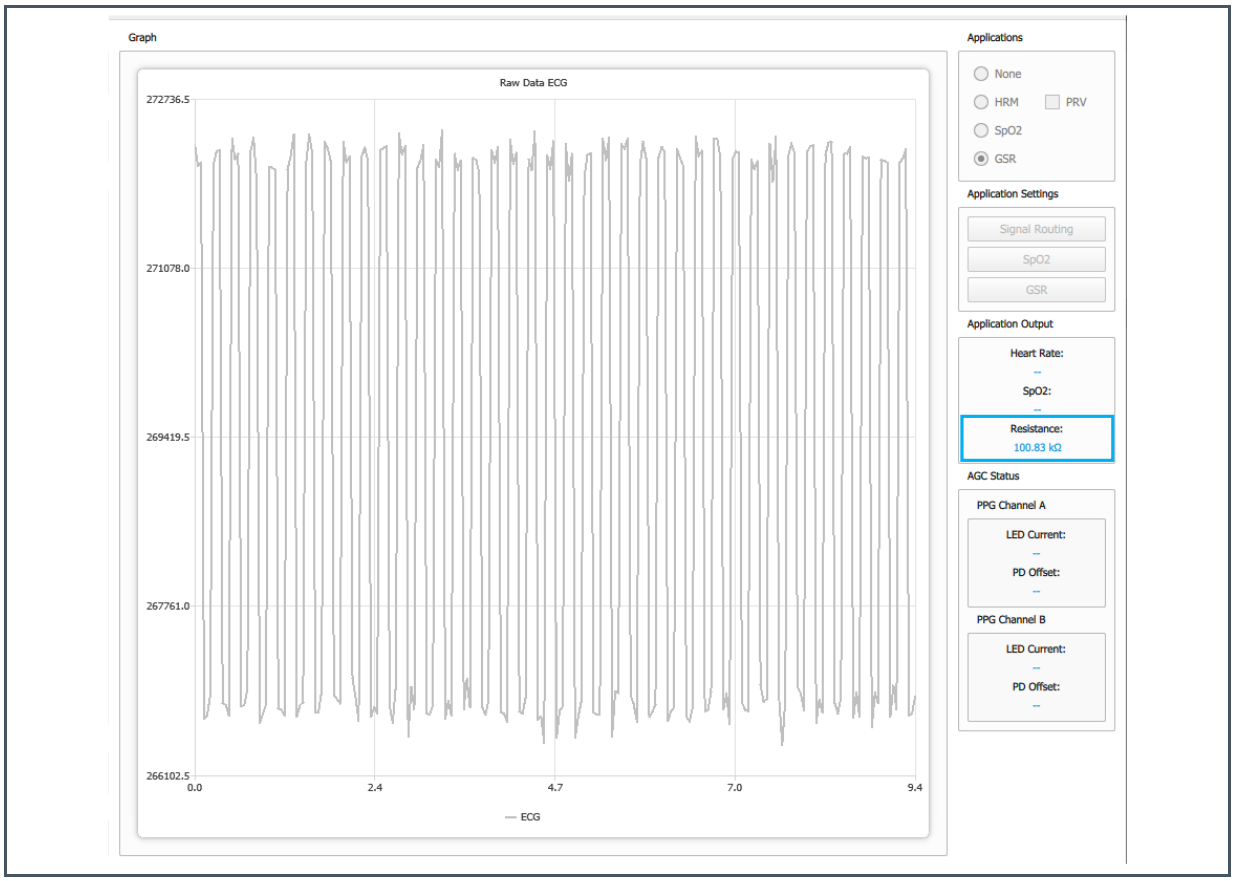
1. Select the “ECG 25 Hz, GSR measurement” configuration preset from the provided configuration presets.
2. Then, select the “GSR” option from the Application settings.
3. Afterward, a pop-up window, “GSR Configuration”, will open.
4. By default, DAC Reference is 35000, but the DAC voltage needs to be set to V_{AFEREF} each time. Therefore, click “Measure DAC Reference” as shown in Figure 82. Then, the system will set a new DAC Reference.

Figure 82:
Measuring DAC Reference



5. Afterward, click the “Start Measurement” button.
6. Then, the resistance value will be seen in the Application Output block, as shown in Figure 83.

Figure 83:
Resistance Value in the Application Output Block



5.5 Menu Bar of the User Interface

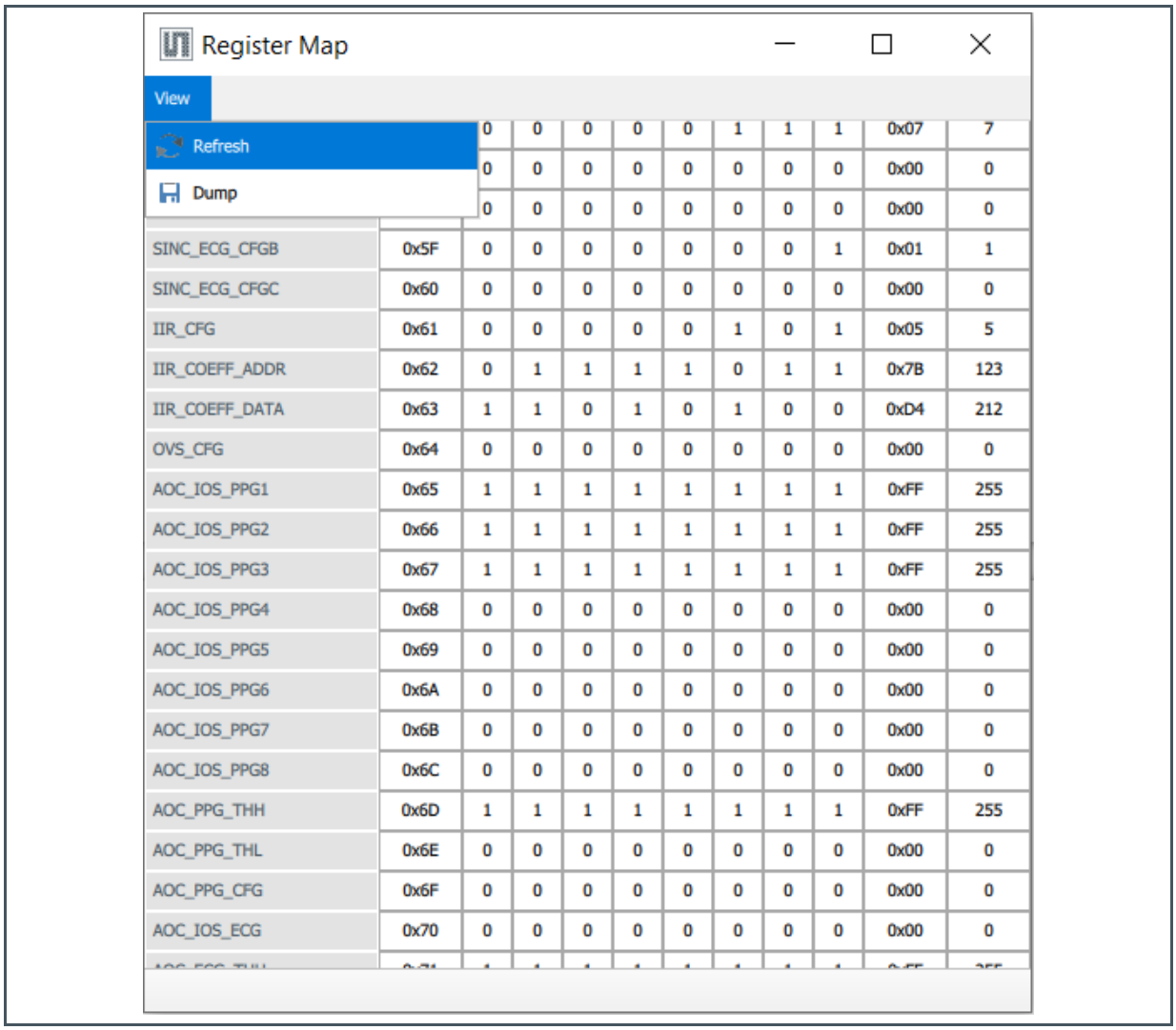
This chapter contains options to the register map list, to load and save a configuration file, to save the log file with the timestamp, and to update the firmware.

5.5.1 Register Map

The “Register Map” window is used to view/change the contents of the complete set of the AS7050 user register. To open it, click on the file, then “ “→ Register Map” menu.

Changing a register value can be done either by modifying its value in the relevant “Value” field or by toggling a bit by clicking on the relevant bit cell. Changing a value in the register map will not update the current selection in the configuration windows of the GUI. Also, a change in any of the configuration windows will not trigger an automatic update of the already opened register map window. To update the values, click on the refresh button marked under the ‘View’ pane on the “Register Map” in Figure 84 below.

Figure 84:
Register Map Dialog Box



		0	0	0	0	0	1	1	1	0x07	7
		0	0	0	0	0	0	0	0	0x00	0
		0	0	0	0	0	0	0	0	0x00	0
SINC_ECG_CFGB	0x5F	0	0	0	0	0	0	0	1	0x01	1
SINC_ECG_CFGC	0x60	0	0	0	0	0	0	0	0	0x00	0
IIR_CFG	0x61	0	0	0	0	0	1	0	1	0x05	5
IIR_COEFF_ADDR	0x62	0	1	1	1	1	0	1	1	0x7B	123
IIR_COEFF_DATA	0x63	1	1	0	1	0	1	0	0	0xD4	212
OVS_CFG	0x64	0	0	0	0	0	0	0	0	0x00	0
AOC_IOS_PPG1	0x65	1	1	1	1	1	1	1	1	0xFF	255
AOC_IOS_PPG2	0x66	1	1	1	1	1	1	1	1	0xFF	255
AOC_IOS_PPG3	0x67	1	1	1	1	1	1	1	1	0xFF	255
AOC_IOS_PPG4	0x68	0	0	0	0	0	0	0	0	0x00	0
AOC_IOS_PPG5	0x69	0	0	0	0	0	0	0	0	0x00	0
AOC_IOS_PPG6	0x6A	0	0	0	0	0	0	0	0	0x00	0
AOC_IOS_PPG7	0x6B	0	0	0	0	0	0	0	0	0x00	0
AOC_IOS_PPG8	0x6C	0	0	0	0	0	0	0	0	0x00	0
AOC_PPG_THH	0x6D	1	1	1	1	1	1	1	1	0xFF	255
AOC_PPG_THL	0x6E	0	0	0	0	0	0	0	0	0x00	0
AOC_PPG_CFG	0x6F	0	0	0	0	0	0	0	0	0x00	0
AOC_IOS_ECG	0x70	0	0	0	0	0	0	0	0	0x00	0

5.5.2 Saving the Current Configuration Settings to a File

The current configuration settings can be exported to a file. To do this, click on the “File → Save Configuration” menu. This will open the “Save Configuration File” dialog box shown in Figure 86. Enter the file name, choose the file location, then click “Save”.

5.5.3 Loading the Configuration Settings From a File

To load a previously exported configuration setting, click on the “File → Load Configuration” menu. This will open the “Select Configuration File” dialog box. Select the configuration file from which to load the settings and click the “Open” button.

The settings imported from the file can be reviewed in the relevant configuration windows.

If the GUI is connected to the board, the newly imported settings will be applied immediately; otherwise, upon successful connection to the board.

Figure 85:
Save and Load Configuration

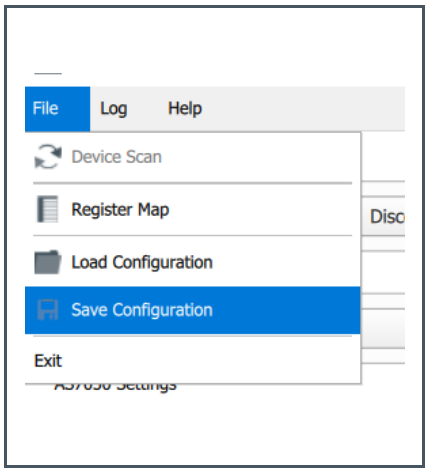
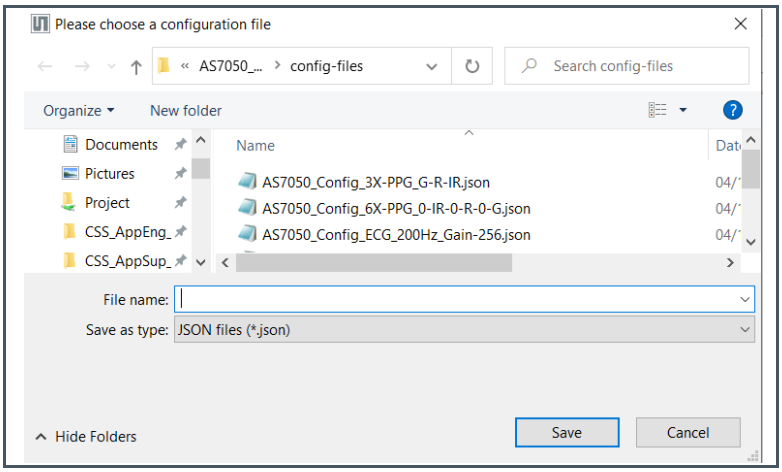


Figure 86:
Save Configuration File Dialog Box

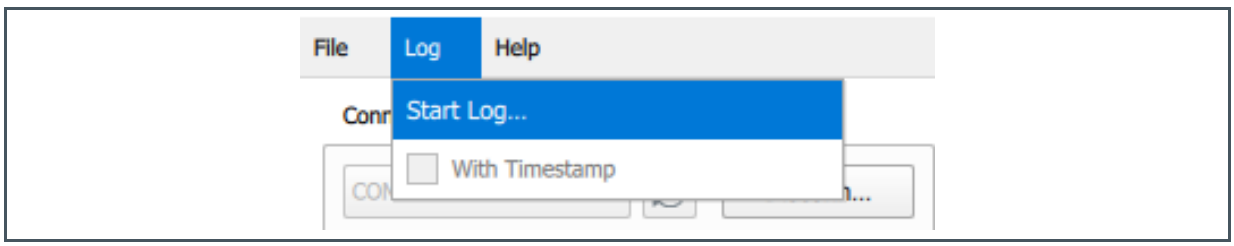


5.5.4 Raw Data Logging and Exporting

Before starting the measurement by clicking the “Start measurement”, click “Log → Start Log” to save the raw data from the AS7050. A pop-up window will appear to select the file location and save the CSV file. When a measurement is stopped with the “Stop measurement” button, afterward, click “Log → Stop Log”.

With Timestamp: If the timestamp is activated, the timestamp will be added to the selected log file name when the measurement starts.

Figure 87:
Logging of Raw Data



5.5.5 About Dialog

The about dialog displays a dialog box with the software name, software version number, firmware version number, python package version number, and copyright plus company link with the technical support link.

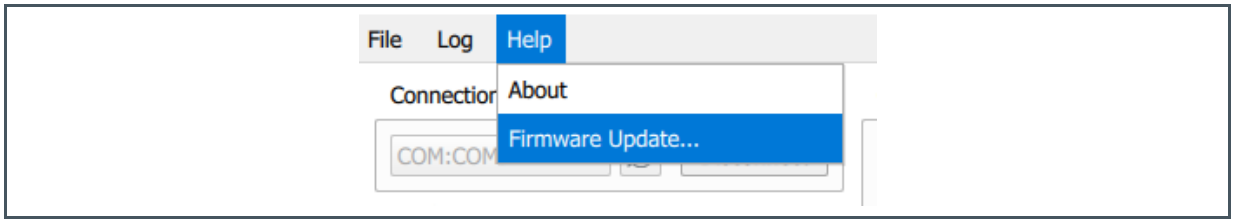
Click “Help → About”.

5.5.6 Firmware Update

There is an option to upgrade the firmware (FW). To achieve this, perform the following steps:

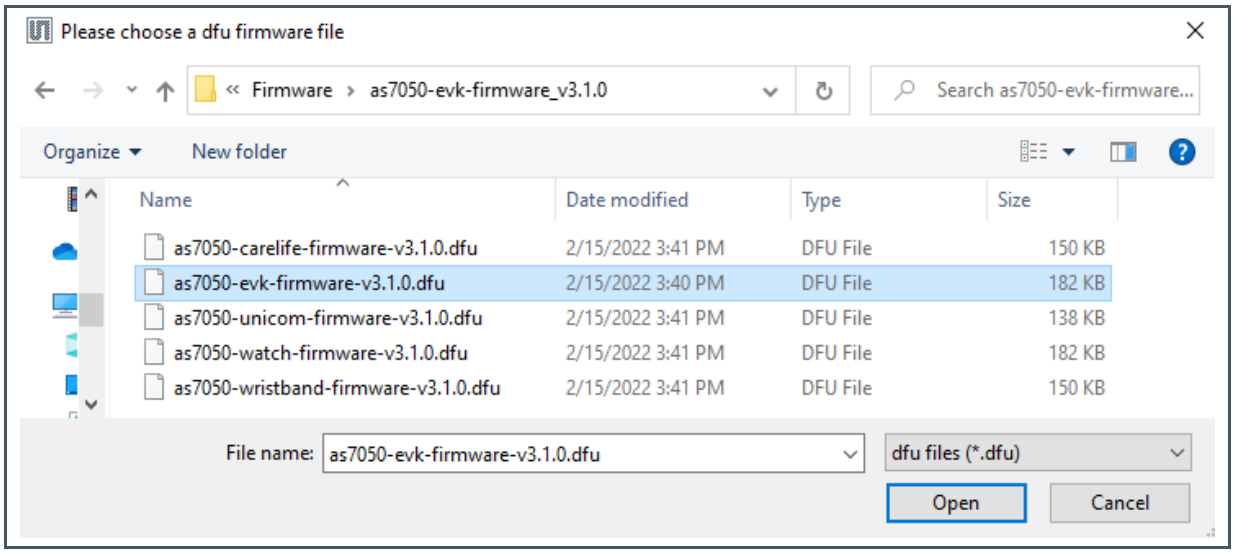
1. Click on the “Help” button and in the drop-down menu click on “Firmware Update…”.

Figure 88:
Firmware Update



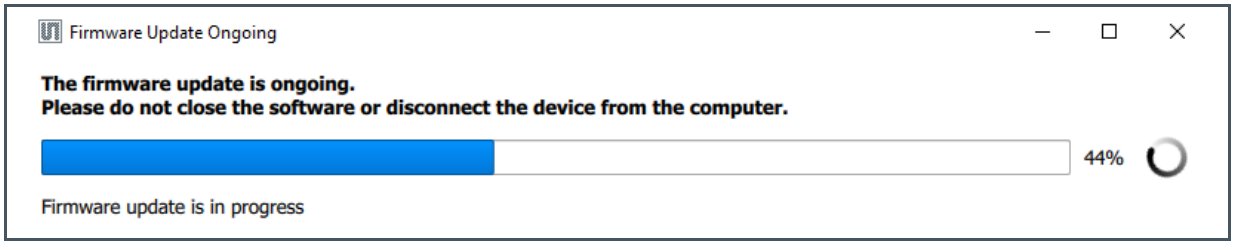
2. In the pop-up window, choose the DFU firmware file used for the AS7050 kit.

Figure 89:
Choose the Right DFU File



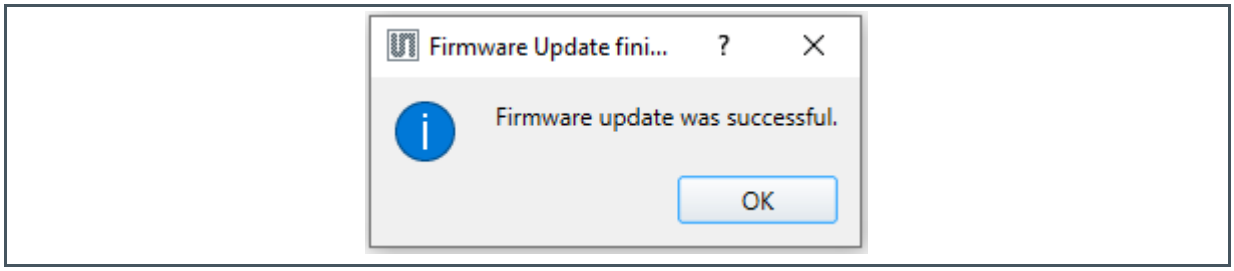
3. Afterward, a pop-up window will open to indicate the update is in progress.

Figure 90:
Firmware Upgrade Stage



4. After the update is complete, a pop-up message will appear in the GUI to indicate the update was successful.

Figure 91:
Successful Firmware Update



6 Revision Information

Changes from previous version to current revision v1-00	Page
Initial version	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

7 Additional Documents

For further information, please refer to the following documents:

1. ams-OSRAM AG, *AS7050 Biosignal Converting Unit* (DS000725), datasheet.

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