Mira050

Datasheet

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Mira050 0.5 MP NIR-enhanced high speed global shutter image sensor

1 General description

1.1 Key specifications & features

Table 1: Key specifications

Parameter	Value	Remark
Active pixels	576 (H) x 768 (V) CSP 600 (H) x 800 (V) Bare Die	On CSP the addressable area is 600 x 800 but only 576 x768 is useable.
Pixel	2.79 µm × 2.79 µm	BSI stacked technology with high NIR sensitivity. Low noise and low cross talk
Optical format	1/7”	
Dimensions	2.29 mm x 2.83 mm	Active area 60% of total.
Shutter type	Voltage domain pipelined global shutter	Possibility of exposure of next image during readout of the previous image.
Spectrum	Mono | NIR	
Supported lens chief ray angle (CRA)	0° to 30°	Extra wide acceptance angle of the Mira050 pixel means any lens profile with these CRA values can be used.
ADC modes	8-bit | 10-bit | 10-bit HS | 12-bit	
Max frames per second full resolution	200 fps	In 10-bit HS mode. Higher fps possible using crop.
Analog gain	1x → 4x step: 2x 1x → 16x step: 2x 1x → 4x step: 3% 1x → 32x step: 2x 1x → 16x step: 3%	12-bit | 10-bit HS (Default mode) 10-bit (Default mode) 10-bit HS (Fine gain mode) 8-bit (Default mode) 8-bit (Fine gain mode)
Digital gain	1x → 16x step: 1/16x	8-bit |10-bit | 10-bit HS | 12-bit
Data interface	MIPI CSI-2 v1.3 DPHY v1.2 1 Data lane | 1 Clock lane	1.5 Gbps with data scrambling support

Table 2: Key benefits & features

Features	Benefits
Programmable registers	Programming of window coordinates, timing parameters, exposure time, mirror, flipping, cropping
High sensitivity and NIR enhanced pixel	High sensitivity and compact pixel size achieved via state of the art BSI technology with NIR enhancement resulting in less power hungry illuminators
Context switching	Two register contexts for on the fly configuration changes
On-chip processing	• Defect pixel detection and correction • Image statistics generation • Event detection • In pixel background light cancellation • Digital pixel binning • Black sun protection • Flexible ROI selection
On-chip advanced power management	Smart powering of on chip blocks with respect to frame rate and exposure time resulting in extended battery life
On-chip temperature sensor	Accurate temperature reading on junction temperature
Illumination synchronization trigger	Accurate timing between illumination and actual exposure

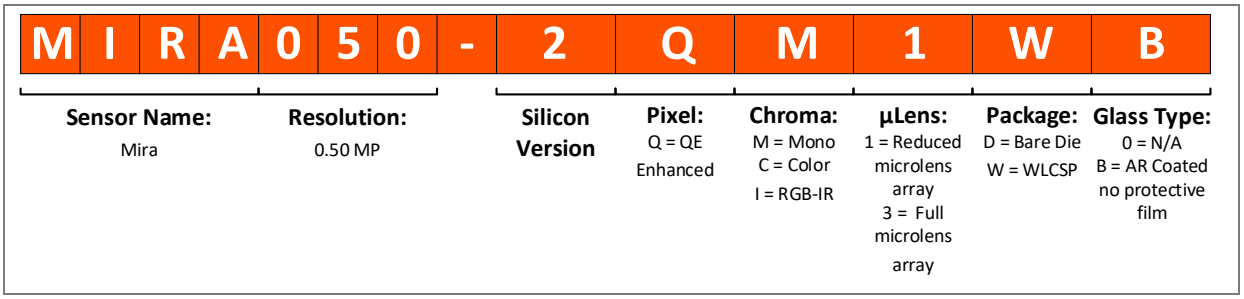
Table 3: Key electro optical parameters (Typical)

Parameter	Value	Remark
Full Well Charge (FWC)	9000e-	1x 12-bit
Min Dark Temp. Noise (DTN)	4.9e-	8x 10-bit
Dynamic Range (DR)	63.3 dB	1x 12-bit
Shutter Efficiency (dB)	-95 dB 940 nm -120 dB 550 nm	In non-pipeline mode
Dark Current (DC)	30e-/s	60°C
Quantum Efficiency (QE)	93% 550 nm 56% 850 nm 36% 940 nm	CSP with AR coated glass
Power Consumption Active	11 mW – 96 mW	Advanced on chip power management adjusts power to various parts of the chip based on frame rate and ROI. Max value refers to 12-bit mode at 120 fps 0.5 MP, min value refers to 8-bit mode 15 fps, 0.5 MP. Lower values possible with reduced ROI

2 Ordering information

Product code	Ordering code	Package	Delivery form	Color filter	Delivery quantity
Mira050-2QM3D0	Q65113A8201	Reconstructed wafer (bare die)	R/W	None	Upon Request
Mira050-2QM1WB	Q65113A8197	CSP	CSP	None	Multiples of 120
Mira050-2QC3D0	Q65113A8203	Reconstructed wafer (bare die)	R/W	RGB	Upon Request
Mira050-2QC1WB	Q65113A8202	CSP	CSP	RGB	Multiples of 120
Mira050-2QI3D0	Q65113A8205	Reconstructed wafer (bare die)	R/W	RGB-IR	Upon Request
Mira050-2QI1WB	Q65113A8204	CSP	CSP	RGB-IR	Multiples of 120

Figure 1: Product code description



3 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at absolute maximum rating conditions is not implied, nor at any other conditions beyond those indicated under “Operating Conditions”.

Table 4: Absolute maximum ratings of Mira050

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Electrical parameters						
VDD28	Analog and pixel supply voltage			3.3	V	
VDD18	Digital IO supply			3.3	V	
VDD12	Core supply			1.3	V	
I_{SCR}	Input current (latch-up immunity)		± 100		mA	JESD78E 90°C
VI	Digital input voltage level	-0.3		3.6	V	
Electrostatic discharge						
ESD_{HBM}	Electrostatic discharge HBM			± 2	kV	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM			± 500	V	JS-002-2018
Temperature ranges and storage conditions						
R_{THJP}	Junction to package thermal resistance		3.3			°C/W
T_J	Operating junction temperature	-30		90	°C	
T_{BODY}	Package body temperature			260	°C	IPC/JEDEC J-STD-020 (1)
	Number of reflow cycles			3		Due to the small pad pitch, standard reflow process may need to be adjusted to achieve reliable solder result.
T_{DRY}	Recommended dry bake temperature	105		125	°C	
t_{DRY}	Recommended dry bake time	8		24	h	125 °C
MSL	Moisture sensitivity level			3		Represents a floor life time of 168 h
RH_{NC_CSP}	Relative humidity (non-condensing) for CSP	5		85	%	
RH_{NC_RW}	Relative humidity (non-condensing) for RW			30	%	
T_{STRG_CSP}	Storage temperature for CSP	-40		85	°C	
T_{STRG_RW}	Storage temperature for RW	17		28	°C	
t_{STRG_CSP}	Storage time for CSP			1	year	According to MSL3
t_{STRG_RW}	Storage time for RW			3	months	Refers to indicated date of packaging

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices.” Use of underfill is recommended to ensure board level reliability requirements are met if components are mounted on application PCB.

4 Electrical characteristics

Table 5: Electrical characteristics of Mira050

Symbol	Parameter	Min	Typ.	Max	Unit
Continuous power dissipation					
P_T	CPD@120 fps,12-bit, 0.5 MP		96		mW
P_T	CPD@15 fps, 8-bit, 0.5 MP		11		mW
Power supplies					
VDD28	Analog supply voltage	2.7	2.8	2.85	V
VDD18	Digital IO supply voltage	1.75	1.8	1.85	V
VDD12	Core supply voltage	1.15	1.2	1.25	V
IDD28	Analog supply current			60	mA
IDD18	Digital IO supply current			10	mA
IDD12	Core supply current			100	mA
Digital I/O					
VIH	High level input voltage	0.7×VDD18			V
VIL	Low level input voltage			0.3×VDD18	V
VOH	High level output voltage	0.8×VDD18		VDD18	V
VOL	Low level output voltage	VSS18		0.2×VDD18	V
treq_exp	REQ_EXP pulse width	2xCLK_IN			
treq_frame	REQ_FRAME pulse width	2xCLK_IN			
Reference clock					
fCLK_IN (1)	CLK_IN frequency	12	24	64	MHz
	CLK_IN accuracy		±50		ppm
DCCLK_IN	CLK_IN duty cycle	45	50	55	%
C-Cjitter,CLK_IN	CLK_IN cycle-to-cycle jitter			100	ps
trise/fall,CLK_IN	Rise and fall transition time			5	ns

(1) The MIPI block requires an escape clock frequency between 12 MHz and 20 MHz (excluding the boundary conditions of 12 MHz and 20 MHz). Given the PLL architecture the input clock ranges between 20 MHz < fCLK_IN < 24 MHz should not be used (both boundaries 20 MHz and 24 MHz can still be used).

5 Functional description

This chapter provides a brief overview of the sensor's architecture and its functionality.

5.1 Sensor architecture

Figure 2 shows a high-level representation of the Mira050. Mira050 is a high-speed global shutter CMOS image sensor for NIR consumer applications. It is a stacked sensor with optimized silicon layer for pixels (sensor layer) and readout/digital (readout layer).

The sensor is compliant to the MIPI CSI-2 v1.3 protocol interface and the D-PHY v1.2 physical layer specifications. It transfers the data over one lane to the host processor. Changing parameters of the sensor goes through the CCI built-in interface.

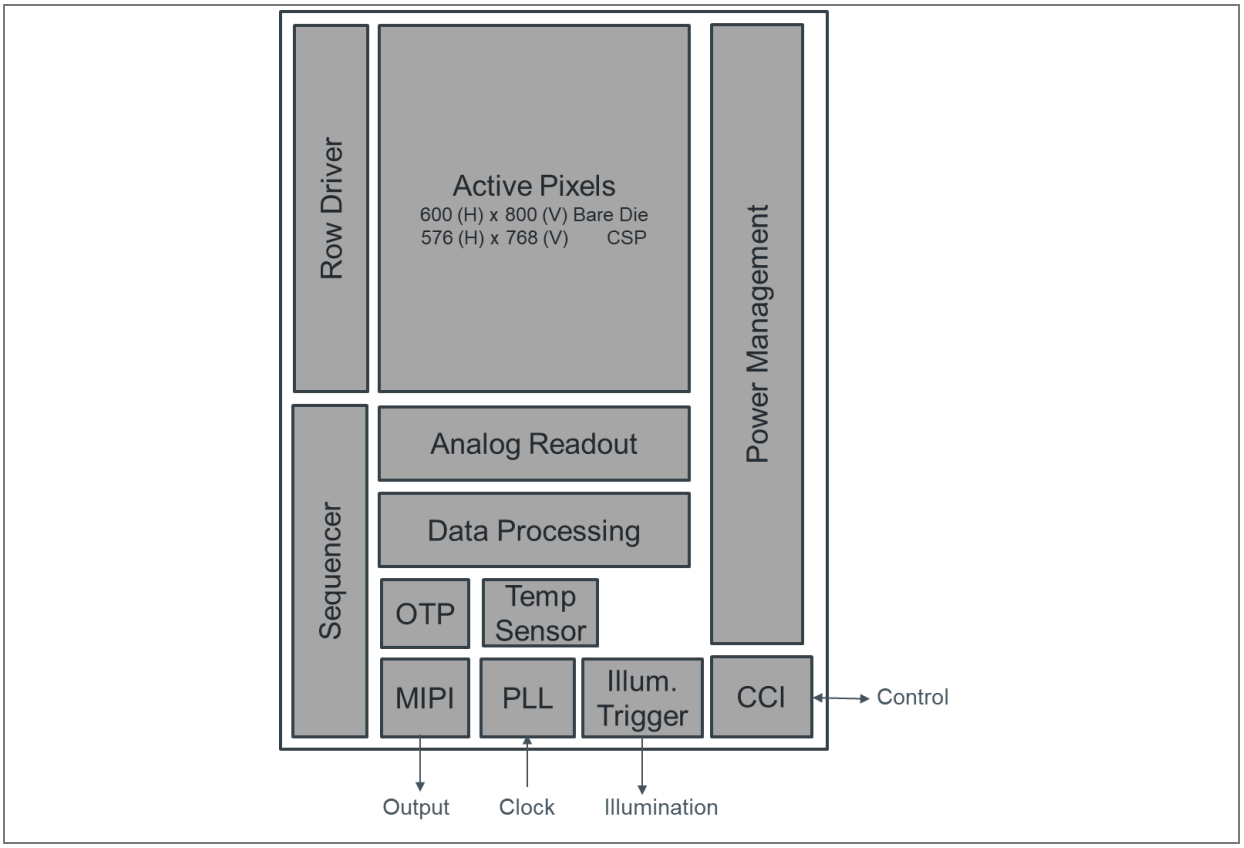
A programmable on-chip sequencer generates all internal exposure and readout timings. External triggering and exposure programming is possible.

The on-chip PLL transforms a low-frequency CMOS input clock into all high-frequency clocks needed to operate the sensor.

The sensor has special features to control other components in the system. It has dedicated outgoing signals for system synchronization between the image sensor itself and an external illumination component (i.e. a NIR illuminator).

The sensor has a built in temperature sensor to allow the user to measure junction temperature.

Figure 2: Sensor architecture block diagram



5.2 Column ADC

Based on the configuration, the column ADC converts the analog pixel value to an 8-, 10- or 12-bit value.

5.2.1 Black sun protection

The black sun protection circuit is used to avoid dark spots in the image, caused by high light levels in extremely over saturated scenes.

5.2.2 Analog gain

The Mira050 has two modes of operation in terms of analog gain. One is Default gain mode which can apply a gain of 1x, 2x, 4x in 12-bit or 1x, 2x, 4x, 8x and 16x in 10-bit with an additional 32x gain in 8-bit mode. The dark temporal noise and FWC for each of the gain modes is given in Table 6.

Also included in the table is the power consumption per gain mode for a typical use case fps in each mode. For details, please refer to the product description PD001051.

Table 6: Typical performance metrics at different gains for non-continuous MIPI clock mode in CSP configuration

Gain	12-bit		10-bit		8-bit		10-bit HS	
	Noise e-	Power mW 30 fps	Noise e-	Power mW 30 fps	Noise e-	Power mW 30fps	Noise e-	Power mW 30 fps
1x	6.1	31	6.9	26	12.3	16	7.3	18.5
2x	5.5	34	5.7	28	9.1	16	6.3	18.6
4x	5.3	39	5.4	30.5	6.8	22	5.8	25.6
8x	NA	NA	4.9	36	6.1	24	NA	NA
16x			5.5	42	5.4	28		
32x			NA	NA	5.8	36		

(1) Parameters are affected by temperature as well as process variations.

The second mode with respect to analog gain is fine gain mode. This gain mode sacrifices maximum frame rate and power efficiency to provide the user with fine tunable analog gain. In this fine gain mode the ADC can operate in 10-bit HS mode which allows the user to set gain from 1x to 4x in steps of 3% or in 8-bit mode with where gain can be set from 1x to 16x in steps of 3%. For details on this, please refer to app note AN001056.

5.2.3 Digital gain

The Mira050 also has a digital gain function where a digital gain can be applied from 1x to 16x in steps of 1/16x.

5.3 Data processing

The data processing block performs digital operations on the pixel data. It is the complete path from reading the data from the ADC output memories up to the inputs of the MIPI block. It supports the following features:

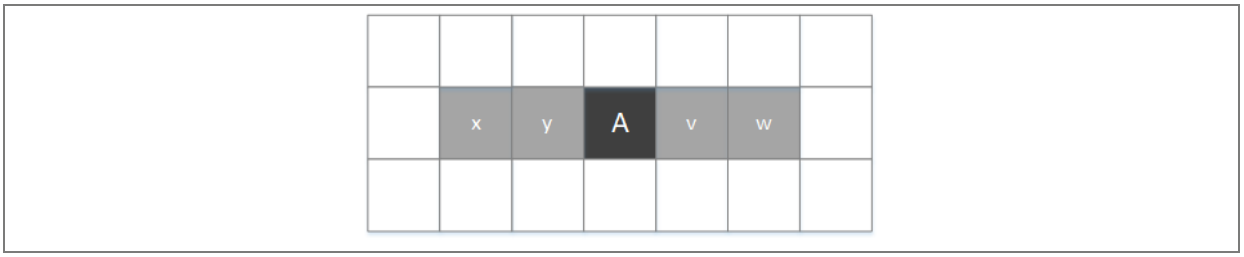
5.3.1 Digital and analog correlated double sampling

The sensor supports digital and analog correlated double sampling (CDS). The CDS logic subtracts the value corresponding to reset level of the pixel from the value corresponding to signal level of the pixel in the digital domain. The combination of analog and digital CDS allows better performance in terms of column fixed pattern noise and 1/f noise.

5.3.2 Defect pixel detection and correction

The sensor supports the detection of defect pixels using horizontal neighboring pixels as reference and applies a correction to that pixel. Both the detection and correction algorithms are configurable. On-chip, the sensor uses the two left hand (x and y) and right hand pixels (v and w) from the same row in order to detect whether current pixel A is defect. Pixels from the rows above or below are not used. When detected as defect the pixel can be corrected. For details please refer to the product description PD001051.

Figure 3: Defect pixel: used pixels for detection



5.3.3 Image statistics

The image sensor can output an image histogram and the number of clipped pixels to reduce the post-processing load on any connected processor. The value of the pixels of a frame can be statistically investigated and gathered into a histogram containing 32 bins. Next to the 32 equally distributed bins, also the number of clipped black and clipped white pixels are

separately gathered and sent out. For details, please refer to the product description PD001051.

5.3.4 Background light cancellation

For use cases that involve extremely bright background conditions, the sensor can operate in background light cancellation mode. In this mode, two exposures are performed consecutively. A first exposure is performed without activating any external illumination and captures the information of the background scene. A second exposure follows with the external illumination active. This exposure contains the information of the background light and that of the external illumination. The signal of the second exposure is stored and subtracted from the first exposure to cancel out the background light. The operation is done on-chip, so a single readout provides the background-light-free image to the external processor, halving power consumption or doubling the frame rate compared to off-chip background light cancellation. For details, please refer to 6.7.1 and 6.8.4 with more information in the product description PD001051.

5.3.5 On-chip event detection

The on-chip event detection can be used for numerous applications, but is mainly intended for supporting a *Sensing Mode* (or auto wake-up mode). In this mode, the sensor runs at a low frame rate with low power consumption. When an event is detected, the sensor autonomously switches the active context to enable high frame rate readout (full performance). For details please refer to the product description PD001051.

5.3.6 Binning and subsampling

The Mira050 supports digital binning and digital sub sampling. Please refer to the product descriptiondocument PD001051 for detailed information.

5.4 CSI-2 data protocol handling & D-PHY communication interface

Data is transmitted off-chip according to the CSI-2 data protocol as defined by MIPI. The physical layer is a D-PHY interface with one data lane and one clock lane operating up to 1.5 Gbps.

5.5 Sequencer

The on-chip sequencer will generate all required control signals to operate the sensor from only a few external control signals. This sequencer can be activated and programmed through the CCI interface.

Among the different features, the sequencer has implemented following:

1. CCI protocol and register bank management.
2. Exposure and frame timing generation based on external inputs or internal settings.
3. Windowing/cropping.
4. Mirroring and flipping.

5.6 CCI interface

The sensor operation must be configured by uploading register settings. These static register values control the behavior of the on-chip sequencer, analog and mixed-signal blocks. To write and read register settings, the CCI (Camera Control Interface) interface is used. This interface is fully compliant with the CCI standard which is a subset of the I²C standard. CCI consists of two wires, SCL and SDA, carrying the clock and data respectively. The Mira050 image sensor always operates as the CCI slave.

5.7 PLL

Various clock frequencies are required internally to operate the sensor. These are derived from a single input clock using an on-chip PLL.

5.8 Temperature sensor

An on-chip thermal sensor is included in the readout layer. The temperature data can be read out through the CCI interface.

5.9 Readout delay

For easy integration with complex systems, where two images sensors are connected to a single MIPI receiver, the sensor has a on-chip delay mechanism that allows de delay of the readout of one of sensors, until the readout of the other is finished.

5.10 OTP memory

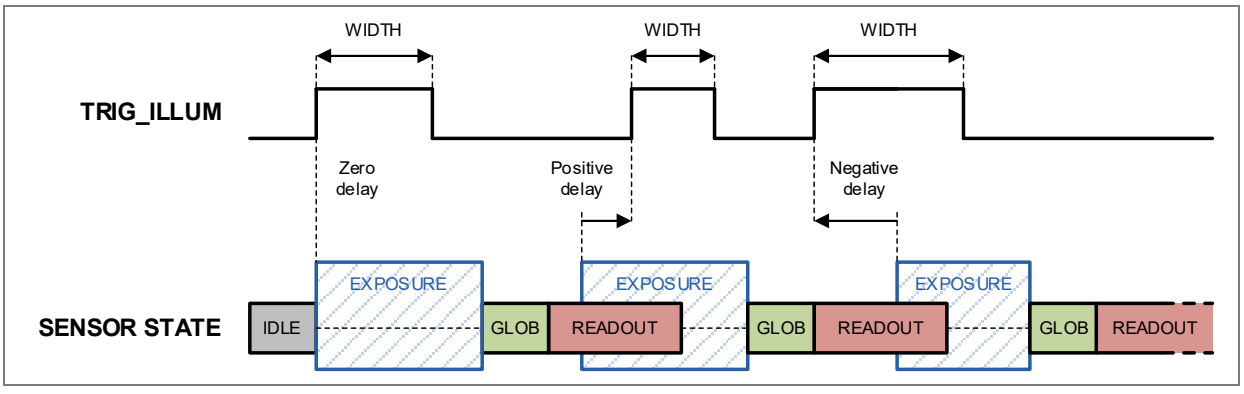
A non-volatile, 8 kbit One Time Programmable memory is included on-chip. Part of the memory is used by ams OSRAM to store a unique device ID and sensor calibration data, another part is available to the customer. For details please refer to the product description PD001051.

5.11 Illumination trigger

The illumination trigger (TRIG_ILLUM) output pin can be used to control an off-chip driver for a flash or illumination device. The trigger is synchronized to the exposure of the pixel array. The delay between the trigger and the exposure phase can be programmed, as well as the width of the trigger signal.

Figure 4 shows how the TRIG_ILLUM signal can be positioned with respect to the sensor's exposure phase. The delay is the time between the TRIG_ILLUM rising edge and the start of exposure on the pixel array. The width is the high time of the TRIG_ILLUM signal.

Figure 4: Illumination trigger



The illumination trigger is synchronized to the actual exposure on the pixels. Any latency between external requests and start of exposure on the pixels is automatically taken into account.

5.12 Low power mode (power management unit - PMU)

The sensor automatically uses a smart low power mode of functionality which considerably reduces the overall power consumption of the sensor. This functionality is most efficient when high data rate mode is used (e.g. 1.5 Gbps). In such mode, the sensor quickly sends the frame data off-chip then enters low power mode until a next frame is needed, reducing the power consumption almost linearly with the fps decrease.

6 Operating the sensor

This chapter explains how to operate the sensor and introduces the user to the sensor's interfaces.

6.1 Power supplies

6.1.1 External power supplies

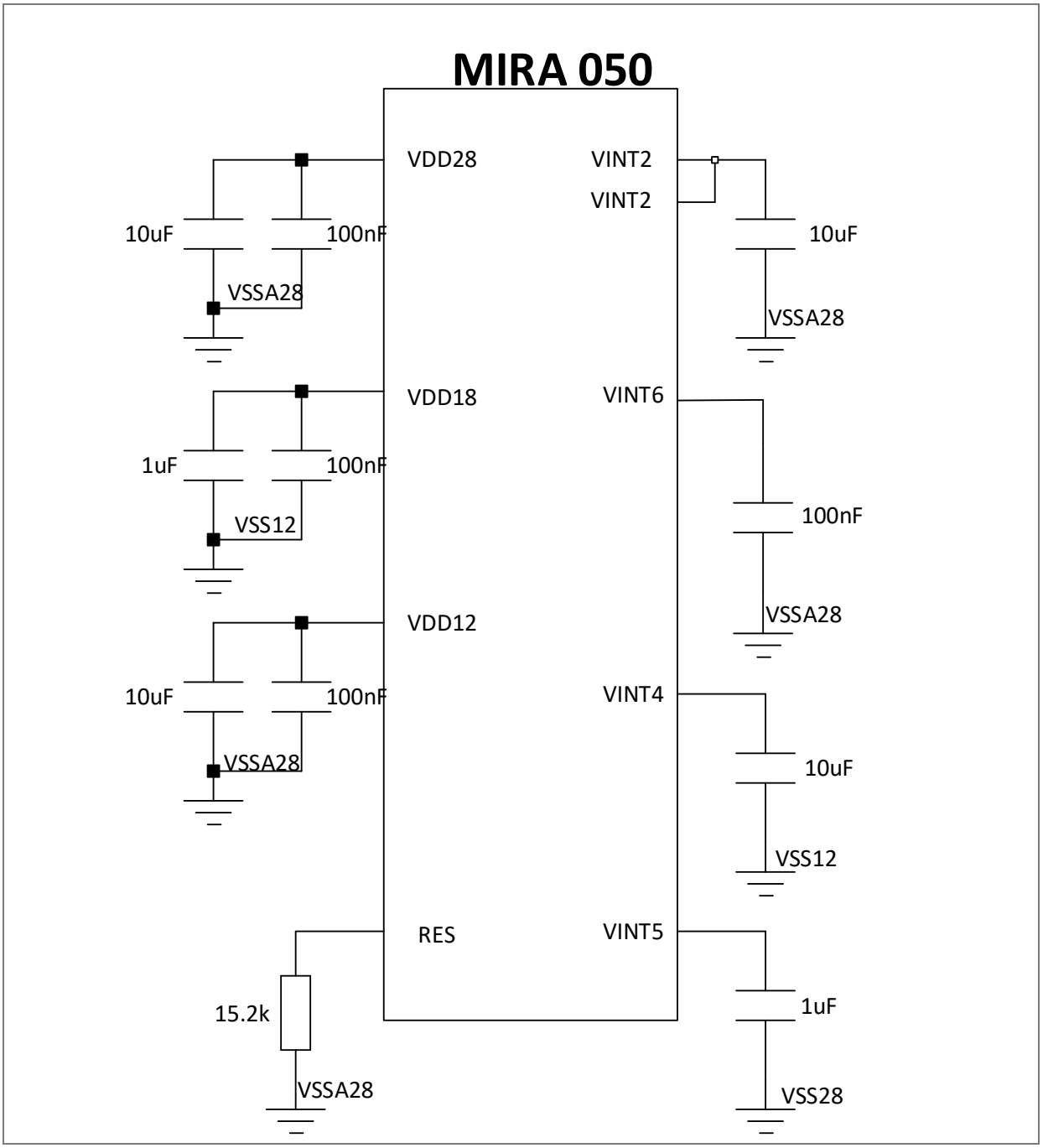
To power the sensor, three externally generated supplies are required as listed in Table 5. Avoid using switching power supplies, when possible, especially for the analog supplies. Please ensure that during startup enough current is supplied to the sensor as shown in Table 5.

For decoupling capacitance please see Figure 5. In case of multiple pins for the same supply, local decoupling is needed for each pin. For optimal noise performance, it is advised to keep the analog and digital ground nets separated and connect them together as close as possible to the external supply regulators.

6.1.2 Biasing (on-chip regulators)

Operating the pixel and readout layer requires multiple supply levels. These levels can be generated using on-chip regulators. The regulator output voltages are controlled using the CCI interface. Each supply regulator requires decoupling by using at least 1 µF capacitor. Figure 5 shows the voltage regulator pins that need to be decoupled using capacitors. To obtain an accurate bias reference in the sensor, an external bias resistor of 15.2 kΩ ±2% must be placed between pin C4 (CSP) or pin 16 (bare die) and ground. Use of 15.0 kΩ ±0.5% or 15.4 kΩ ±0.5% is also possible as bias resistor.

Figure 5: Regulator decoupling and biasing(1)



(1) There are 2 VINT2 pins and both need to be shorted externally via low resistance path (max 0.1 Ohm).

6.2 Power-up/down sequence

A specific order and timing must be applied to the sensor supplies to guarantee a proper power-up/power-down sequence and to avoid peak currents.

Attention: Failure to observe this may lead to malfunction.

Please ensure that enough current is supplied during startup as shown in Table 5.

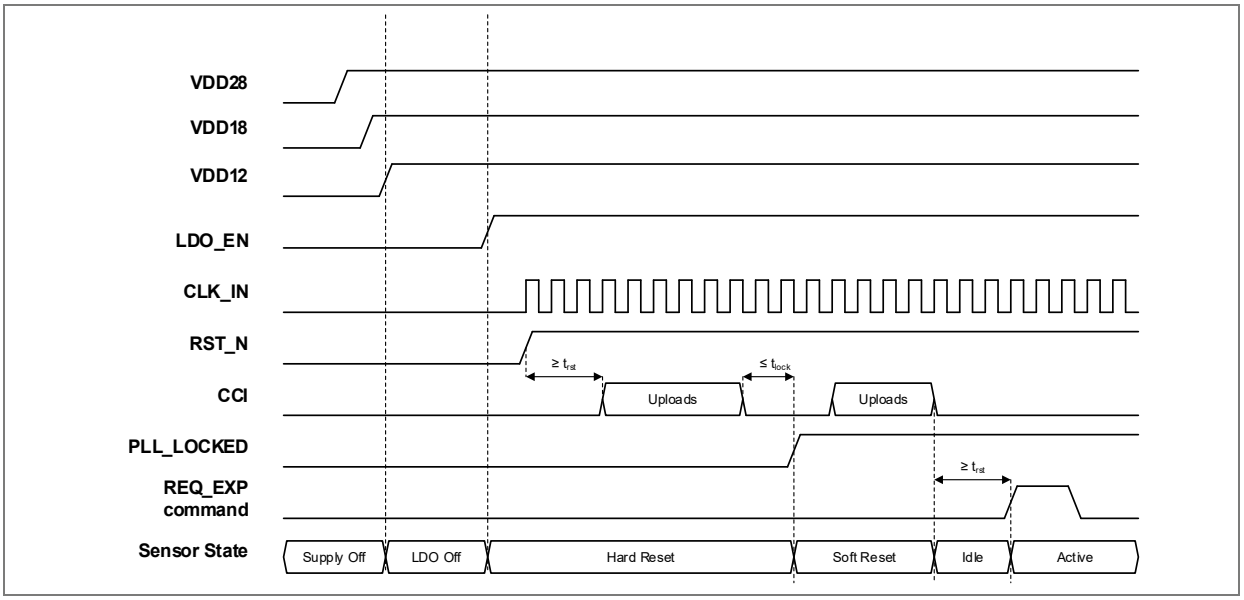
6.2.1 Power-up sequence

1. Apply power to VDD28. Allow the supply to finish ramping up and stabilize.
2. Apply power to VDD18 and VDD12. Allow these supplies to finish ramping up and stabilize.
3. Enable the LDO by asserting LDO_EN high. Wait for 0.1ms for the LDO to stabilize.
4. Apply the external clock on the CLK_IN clock input pin.
5. Drive pin REQ_1 low.
6. Release the hard reset signal on the RST_N input pin.
7. CCI communication is now available and must be used to configure and enable the PLL.

   Wait for the PLL to lock. Check the lock status on TDIG1 pin or in the read-only register PLL_LOCKED to determine when the PLL is ready.
8. The sensor is now in its default state and can be further configured for image capture and pixel data output.

An overview of these different steps is shown in Figure 6.

Figure 6: Power-up sequence



(1) t_{rst} = 50ns t_{lock}= 5000 CLK_IN cycles.

6.2.2 Power-down sequence

1. Stop all image capture processes.
2. Set RST_N IN input pin to LOW state.
3. The external clock can now be disabled on the CLK_IN input pin.
4. Disable power on VDD12 and VDD18.
5. Disable power VDD28.

6.3 PLL and clocking

The sensor has two CMOS clock inputs: CCI_SCL and CLK_IN. CCI_SCL is part of the CCI used to configure the sensor. All other internal sensor clocks are derived from the PLL, taking CLK_IN as input clock. Refer to Section 3 for the electrical specifications of the input clocks. Please refer to the product description document PD001051 for detailed information.

6.4 Camera control interface (CCI)

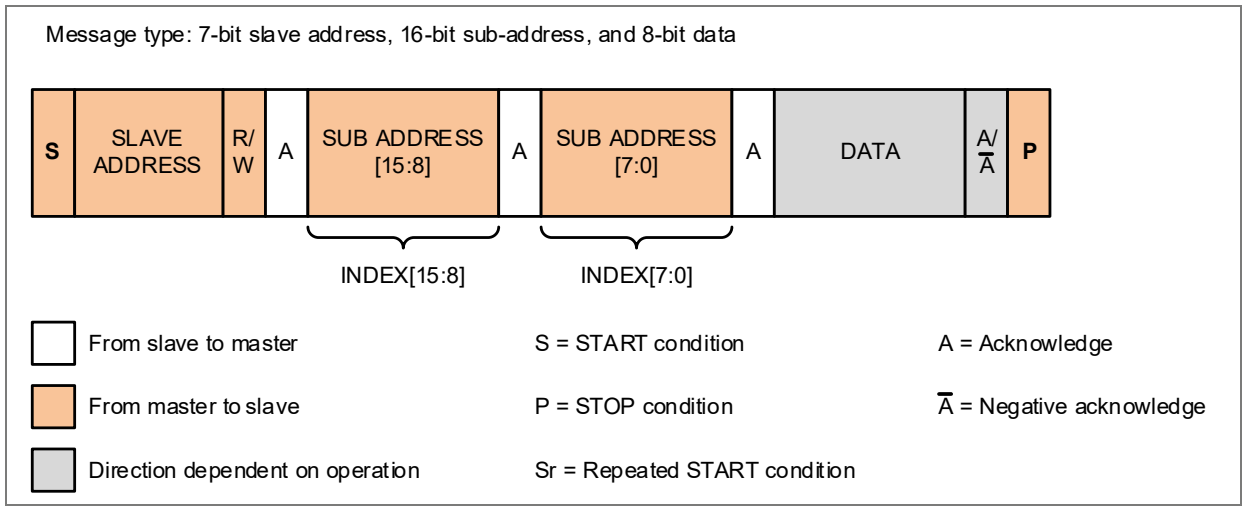
The two-wire serial Camera Control Interface (CCI) enables read/write access to control and status registers within the sensor, which always acts as a slave on the CCI bus. The CCI is defined in the MIPI CSI2 specification CSI-2-v1.3. The slave address of Mira050 is 011011Xb, where X depends on the CCI_ADDRESS input pin of the sensor.

Typically, there is a dedicated CCI interface between the sensor and the host system. CCI is a subset of the I²C protocol. Therefore, the Mira050 can also be connected to the system I²C bus. Care must be taken so that I²C masters do not try to utilize those I²C features that are not supported by CCI devices.

6.4.1 Message format

Figure 7 shows the general CCI message format. The sensor uses 16-bit sub-address (index) with 8-bit data, which means every 8 bits of data is followed by an ACK/NACK. A message may contain multiple 8-bit data fields if a multi-byte register is accessed. Every CCI transaction starts with a *start condition* and ends with a *stop condition*. The *repeated start* condition is only used in read operations starting from a random address location.

Figure 7: CCI message format



The sensor contains many registers of different sizes. Multi-byte registers have their most significant byte located at the lowest address and their least significant byte located at the highest address (i.e., **big endian** byte format). Partial access to multi-byte registers is not allowed. Use sequential read/write operations to access multi-byte registers.

6.4.2 Read and write operations

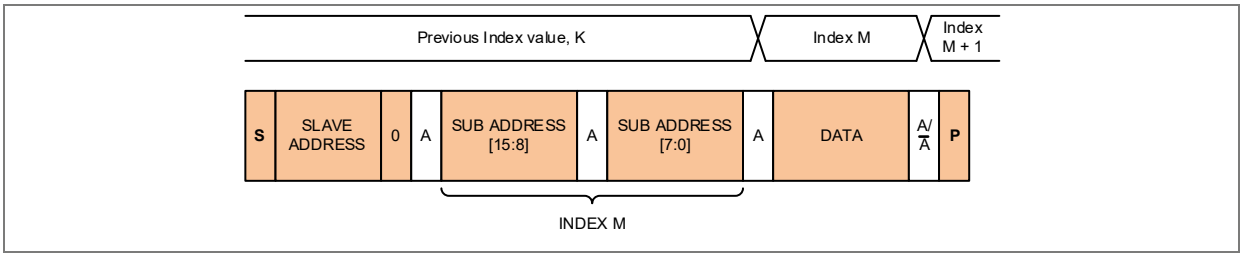
The Mira050 supports four different read operations and two different write operations:

- Single write to random location.
- Single read from random location.
- Single read from current location.
- Sequential write to random location.
- Sequential read from random location.
- Sequential read from current location.

Each operation is detailed below. The sub-address (index) in the sensor is auto-incremented after each data byte (in a read or write operation).

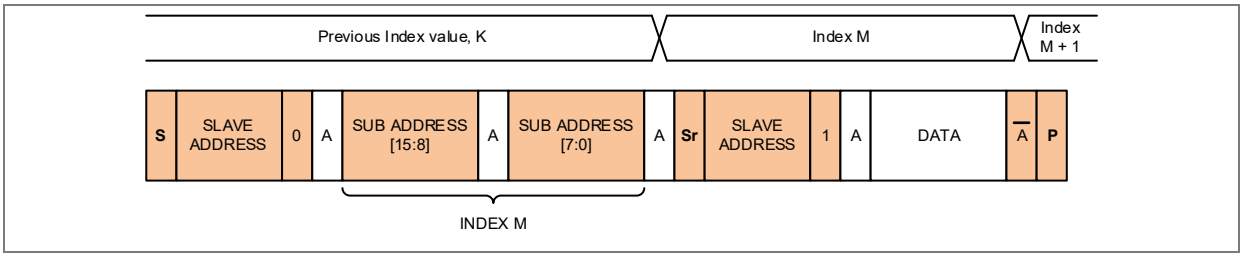
The single write to random location is illustrated in Figure 8. The master issues a write operation to the sensor, followed by the sub-address (index) and data. The write operation is terminated with a stop condition from the master.

Figure 8: CCI single write to random location



In a single read from random location the master does a dummy write operation to the desired index, issues a repeated start condition, and then addresses the sensor again with a read operation. After acknowledging its slave address, the sensor starts to output data onto the SDA line as shown in Figure 9. The master terminates the read operation by setting a negative acknowledge followed by a stop condition.

Figure 9: CCI single read from random location



If the host skips the dummy write operation and directly accesses the sensor with a read operation, the sensor will output the data from the last used index onto the SDA line. This is illustrated in Figure 10.

Figure 10: CCI single read from current location

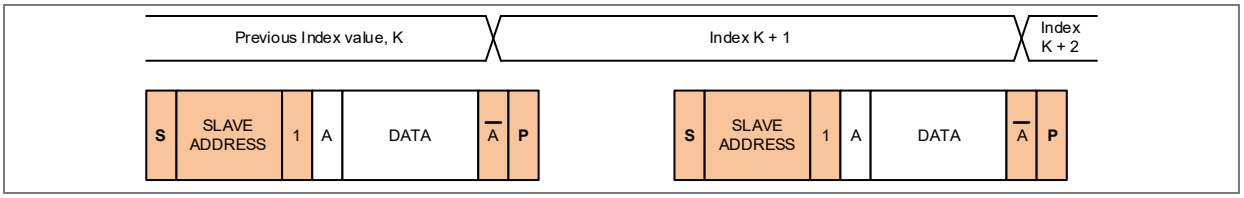


Figure 11 illustrates the sequential write to random location. The sensor auto-increments the index after each data byte is received. The sequential write operation is terminated with a stop condition from the master.

Figure 11: CCI sequential write to random location

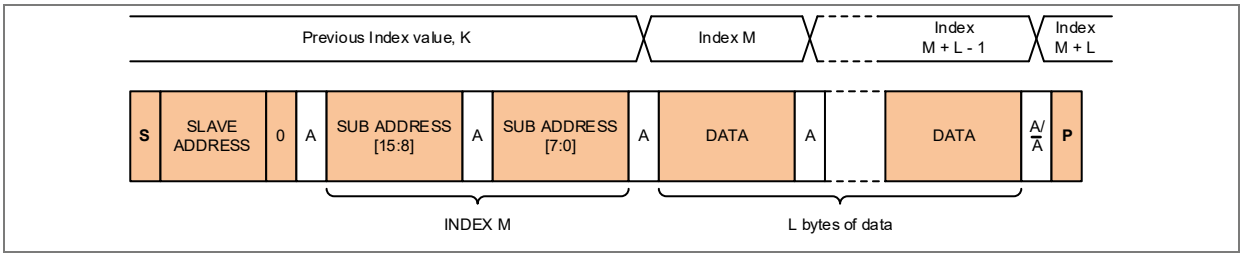
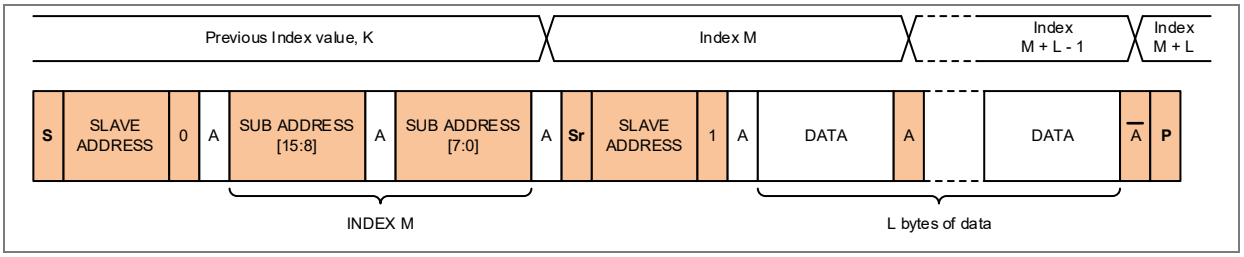


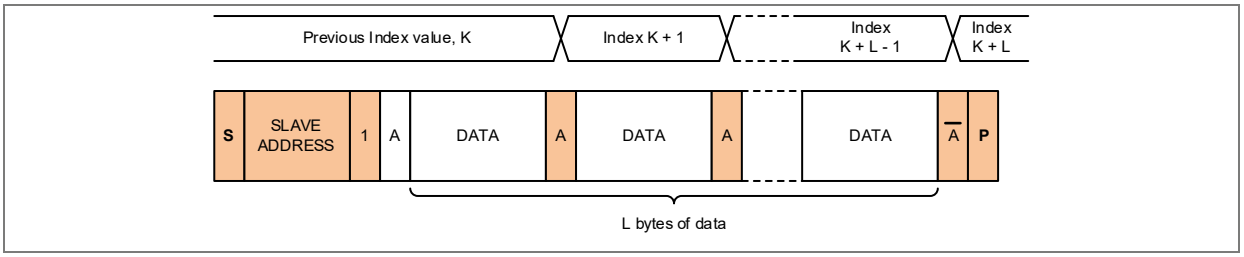
Figure 12 illustrates the sequential read from random location. The master does a dummy write to the desired index, issues a repeated start condition, and then addresses the slave again with a read operation. If the master issues an acknowledge after receiving a byte of data, the sensor continues to output data from the next index. When the master has read the last data byte, it issues a negative acknowledge and stop condition.

Figure 12: CCI sequential read from random location



The command sequence for a sequential read from current location is shown in Figure 13. The difference with the sequential read from random location is that there is no dummy write operation. The sensor will output data from the last used index. The master terminates the read operation by issuing a negative acknowledge and stop condition.

Figure 13: CCI sequential read from current location



6.4.3 Timing characteristics

The CCI timing diagram is shown in Figure 14. The timing specifications are shown in Table 7.

Figure 14: CCI timing diagram

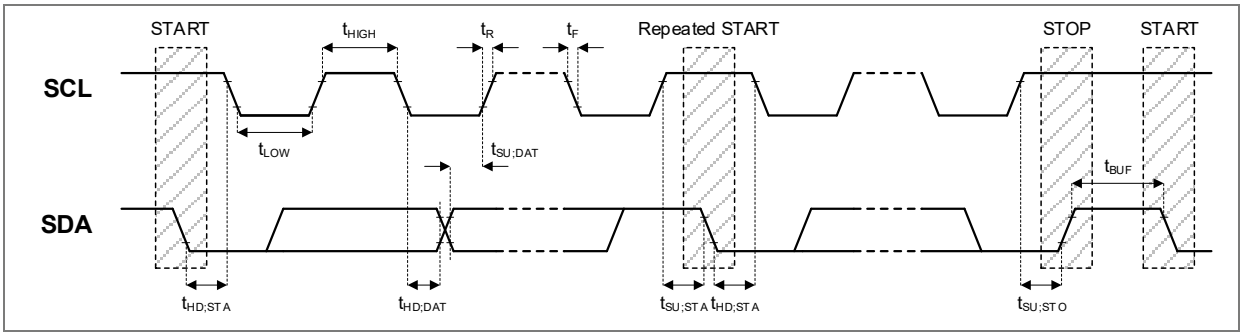


Table 7: CCI timing specification

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	-		400	kHz
t_{LOW}	LOW period of the SCL clock	1.3		-	µs
t_{HIGH}	HIGH period of the SCL clock	0.6		-	µs
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6		-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6		-	µs
$t_{HD;DAT}$	Data hold time	0		-	µs

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SU;DAT}$	Data setup time	0.1		-	µs
$t_{SU;STO}$	Setup time for STOP condition	0.6		-	µs
t_R	Rise time of both SDA and SCL signals	-		0.3	µs
t_F	Fall time of both SDA and SCL signals	-		0.3	µs
t_{BUF}	Buss free time between a STOP and START condition	1.3		-	µs

6.4.4 Context switching

A *context* is a collection of register settings that is used to define a specific image acquisition setup. The sensor supports two contexts, named A and B. At any time, one of the contexts is active while the other one is inactive. Switching from one context to another is called a *context switch* and can be done on the fly through the CCI interface.

The following settings are context switchable. These settings are part of both contexts and can be programmed independently inside each context.

- Exposure/frame settings
  - Exposure time
  - (target) Frame time
  - Number of frames in an acquisition sequence (only for Triggered Internal and Background Light Cancellation)
  - Illumination trigger alignment
- Region of interest (ROI)
  - One programmable horizontal window
  - Up to 10 programmable vertical windows
  - Subsampling in X and Y direction
  - Binning in X and Y direction
  - Mirroring in X and Y direction
- Digital gain
- Enable/disable of different features
  - Illumination trigger
  - Synchronization trigger
  - On-chip event detection
  - On-chip histogram generation
- Data transmission options
  - Pixel data + histogram data (when enabled)
  - Histogram data only

By default, a context switch is synchronized to the start of a new frame readout. This ensures the sensor uses a consistent set of register settings throughout the acquisition of the entire frame. The synchronization mechanism can be disabled to switch the active context when the sensor is IDLE.

Figure 15 shows a typical context switch example with synchronization enabled. Here, the sensor is continuously acquiring frames at a steady frame-rate using context A. Somewhere during the acquisition, the user changes register settings in the inactive context (context B). These modifications do not influence the current sensor operation. Once all modifications are done, a context switch is performed. The sensor synchronizes the context switch to the start of a new frame readout. All following frames will be acquired with context B, which is now active.

Note that internally in the sensor, the exposure and readout settings do not update to the new context at the same time. This is because the exposure of the next frame can overlap with the readout of the current frame. The sensor logic makes sure that an exposure of a frame and the readout of that frame are done with the same context settings.

Figure 15: Synchronized context switch

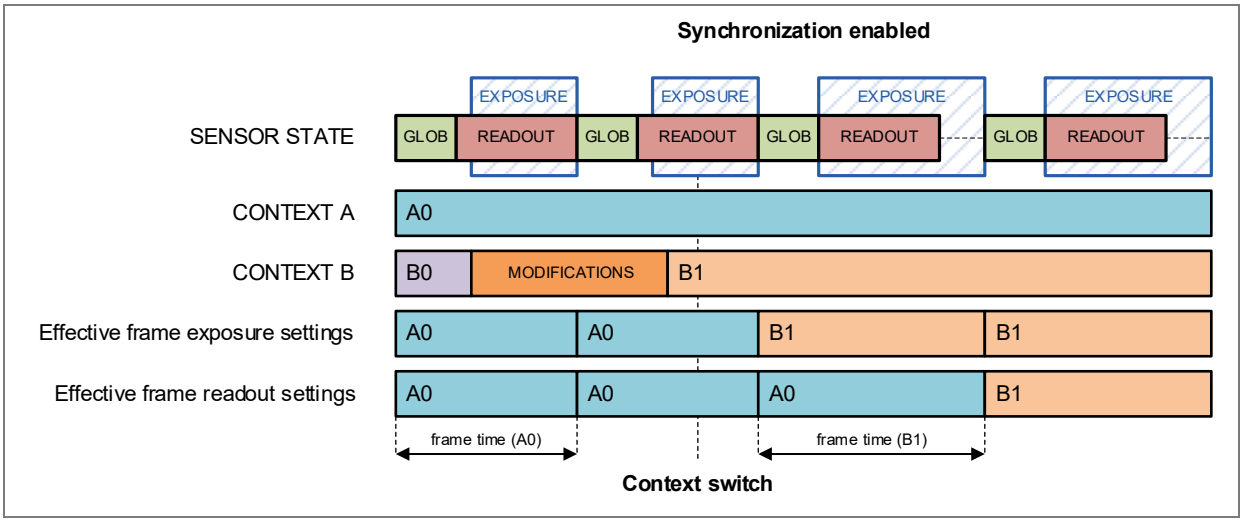
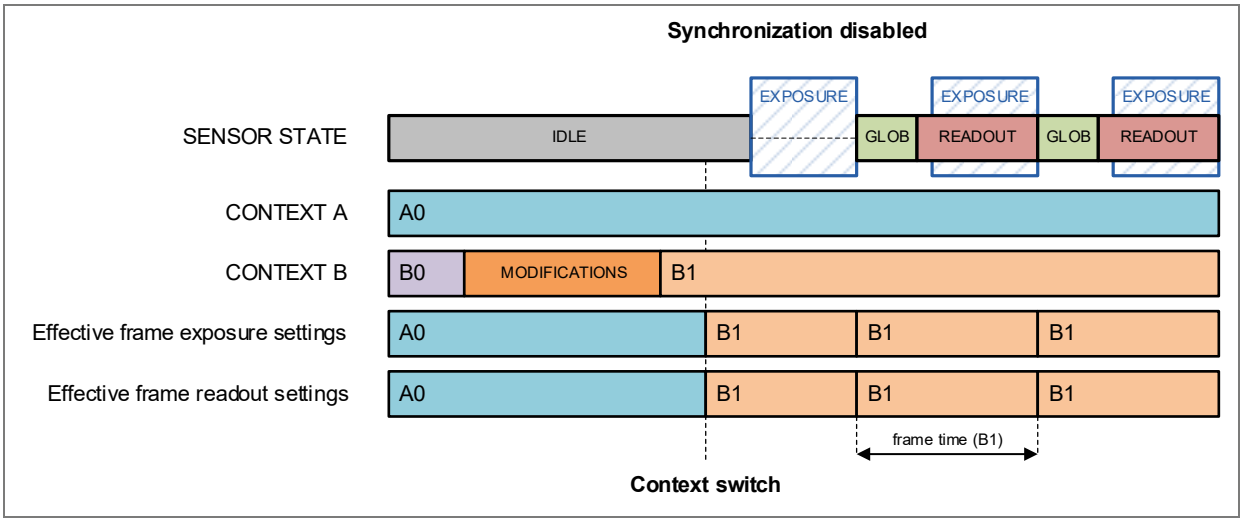


Figure 16 shows an example of an immediate (non-synchronized) context switch. In this case, the user switches from context A to context B when the sensor is IDLE. Since synchronization is disabled, the new context becomes active immediately. When image acquisition starts, all frames will be acquired with context B. Note that with synchronization enabled, the first frame would still be acquired with the old context (context A) because of the synchronization mechanism.

Figure 16: Immediate (non-synchronized) context switch



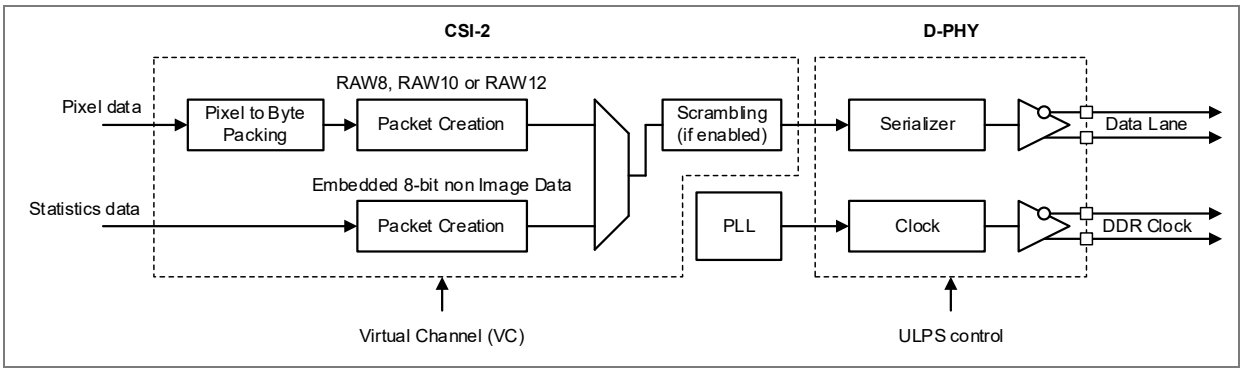
6.5 CSI-2 and D-PHY

The sensor's MIPI interface consists of a CSI-2 protocol layer combined with a D-PHY physical layer. The type of data lane used is a CIL-MFEN. The type of clock lane used is a CIL-MCNN.

Figure 17 shows an overview of the output data interface. The pixel data is transmitted as RAW8, RAW10, or RAW12 CSI-2 packets. The packet type depends on the bit depth. If on-chip statistics gathering is enabled, it is transmitted as "Embedded 8-bit non Image Data" at the end of each frame. The user can set the Virtual Channel to be used for all data packets. The generation of Line Start and Line End packets depends on the selected frame mode.

The sensor supports data scrambling, which requires CSI-2 v2.0 compatibility.

Figure 17: MIPI output interface overview



The D-PHY layer serializes the CSI-2 packets and transports them to the receiving system on a single data lane. The D-PHY clock lane transports a DDR clock that is used by the receiving system to sample the data on the data lane. This clock lane can operate in continuous or non-continuous mode. The clock lane and data lane both support Ultra-Low Power State (ULPS).

The following sub-sections provide more details on the supported CSI-2 and D-PHY features.

6.5.1 Frame mode

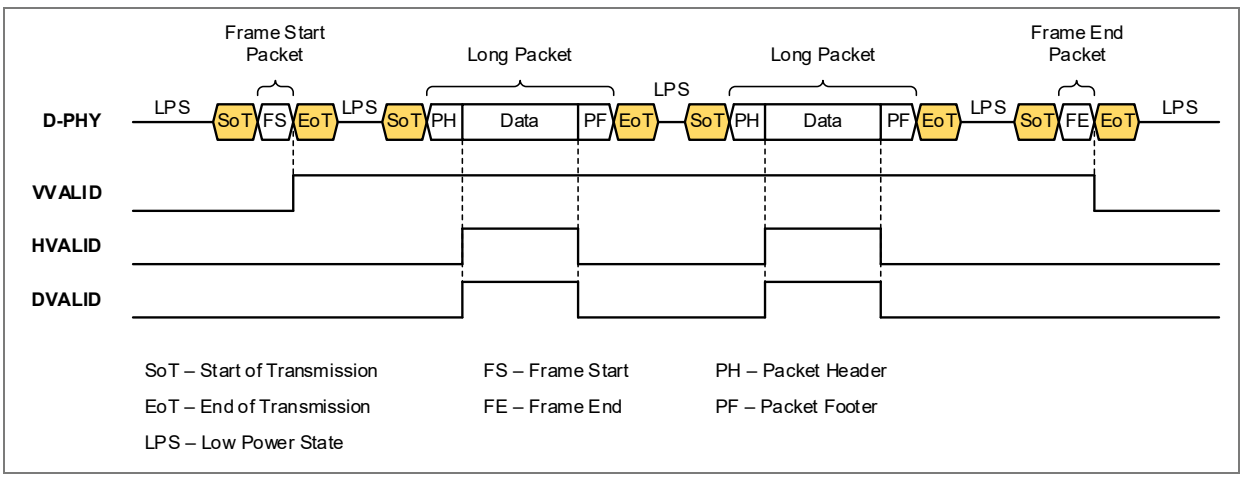
The frame mode determines whether the output interface inserts Line Start and Line End packets in the data stream. Two frame modes are available:

- Global timing mode
- Accurate timing mode

By default, the sensor operates in *global timing mode*, which means that Line Start and Line End packets are not generated. Figure 18 shows an example of a frame with two rows, transmitted on the output interface in global timing mode.

Note that the VVALID, HVALID and DVALID signals in the figure are only concepts to help illustrate the behavior of the packets on the interface. These signals are not part of the output interface and are not generated by the sensor.

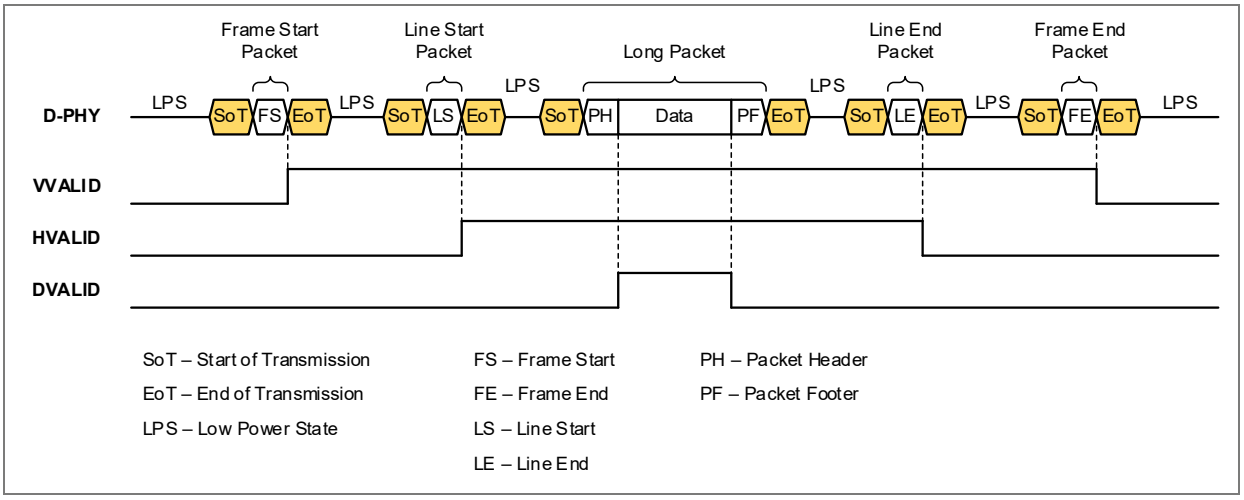
Figure 18: Frame mode – global timing mode



When using *accurate timing mode*, each data packet is surrounded by a Line Start and Line End packet pair. Figure 19 shows an example of a frame with one row, transmitted on the output interface in accurate timing mode.

Accurate timing mode increases the line time and possibly decreases the maximum achievable frame rate. This is due to the additional time it takes to transmit the Line Start and Line End packets. Power consumption will be higher due to increased high-speed activity on the D-PHY lanes.

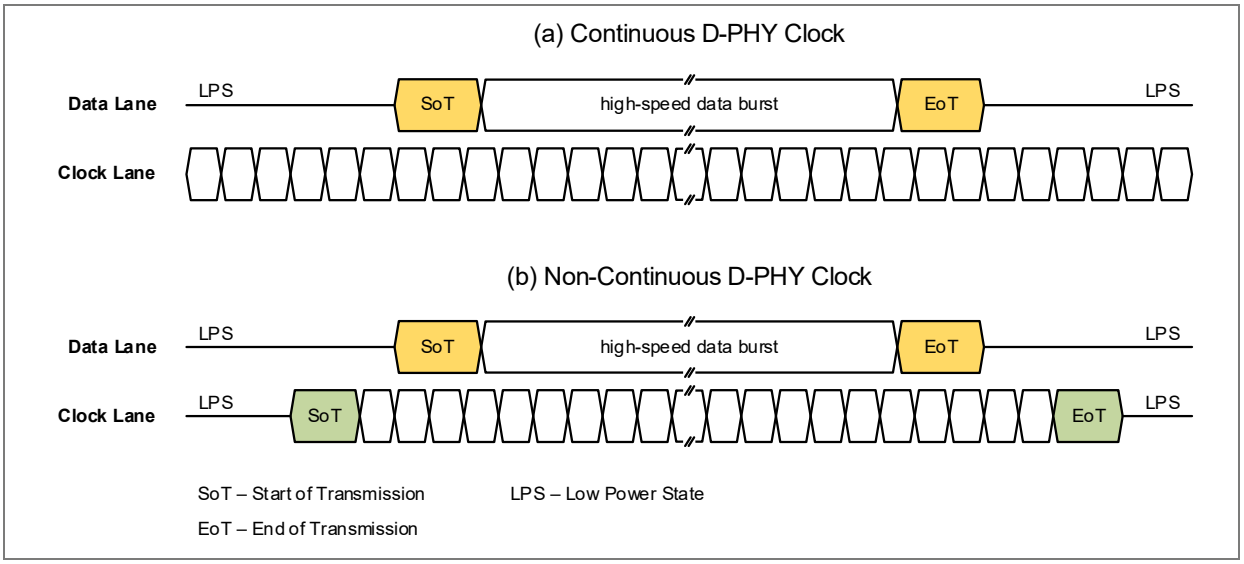
Figure 19: Frame mode – accurate timing mode



6.5.2 Continuous and non-continuous D-PHY clocking

The D-PHY clock lane can operate in continuous or non-continuous mode as shown in Figure 20. In *continuous clock mode*, the clock lane remains in high-speed mode between data bursts. The clock lane starts transporting a DDR clock as soon as the output interface is properly initialized and remains in high-speed mode indefinitely. In *non-continuous clock mode*, the clock lane goes to Low Power State in between data bursts. The clock lane exits Low Power State prior to the transmission of a high-speed data burst on the data lane. It re-enters Low Power State after the high-speed data burst is completed. Note that the Start of Transmission (SoT) and End of Transmission (EoT) sequences are different for the clock and data lane.

Figure 20: Continuous and non-continuous clock mode



The choice between continuous and non-continuous clock mode depends on power, throughput and receiver complexity. Using continuous D-PHY clocking is straightforward and allows the highest data throughput, but it consumes more power as the clock lane is also running when no data is being transmitted.

6.5.3 Timing parameters

All DPHY-v1.2 data rate dependent timing parameters are adjustable through register settings. This ensures that the timing specifications on the interface can be met when operating the sensor in different modes or at different output data rates.

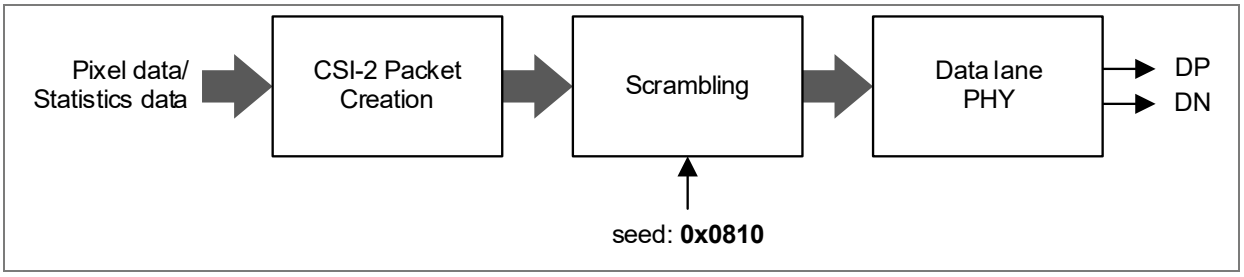
6.5.4 Data scrambling

Data scrambling is a CSI-2 version 2.0 feature.

Data scrambling is a technique used to mitigate the effects of EMI and RF self-interference by randomizing the data in the CSI-2 packets. Figure 21 gives a high-level overview of the data scrambling used in the output interface. When enabled, the long packet header, data payload, long packet footer, and short packets are scrambled before they are transmitted across the D-PHY data lane. Scrambling applies to pixel data and statistics data (if enabled). Data scrambling does not affect the D-PHY clock lane.

The lane seed value used to initialize the scrambler is 0x0810.

Figure 21: Data scrambling



6.6 Reset

The sensor has two reset states, called *hard reset* and *soft reset*. In the hard reset state, the entire sensor is reset. This includes resetting the CCI interface and internal register banks. All registers will be reset back to their default value. In the soft reset state, the entire sensor is reset, except for the CCI interface and internal register banks. All registers will retain their values. All static register configuration is done while the sensor is in soft reset state.

Hard reset state is entered by asserting the asynchronous reset input pin (RST_N) low. Note that CCI communication is not possible until the RST_N pin is deasserted high. Soft reset is controlled through register write operations.

6.7 Image acquisition

This section gives a general overview of the sensor's image acquisition. It explains important concepts, which the user needs to understand in order to configure the sensor correctly. These concepts also help in understanding the sensor's possibilities and limitations.

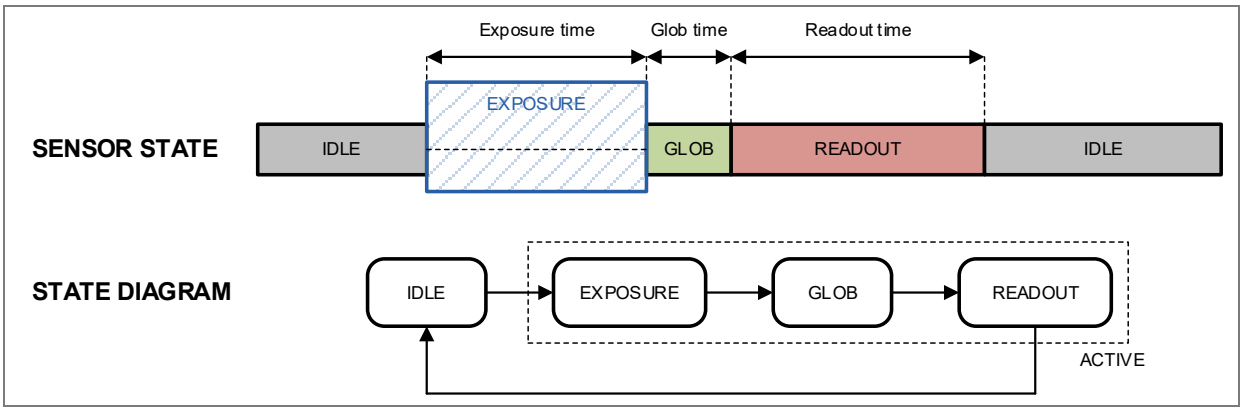
The image acquisition consists of several phases that are reflected by the sensor's state. The sensor can be in any of the following states:

- **IDLE**: The sensor awaits external requests.
- **ACTIVE**: The sensor is acquiring a frame. This state has three sub-states, called EXPOSURE, GLOB and READOUT.
  - **EXPOSURE**: The global shutter is opened and photons are accumulated in the pixels. The length of this state is called the *exposure time*. This total accumulation or integration of incident light over the exposure time is called the *integrated pixel value*.
  - **GLOB**: The global shutter is closed by sampling all integrated pixel values. The length of this state is called the *glob time*. The glob time is a constant for a given use case.

– **READOUT**: The acquired frame with metadata and mandatory overhead is read out. The length of this state is called the *readout time*.

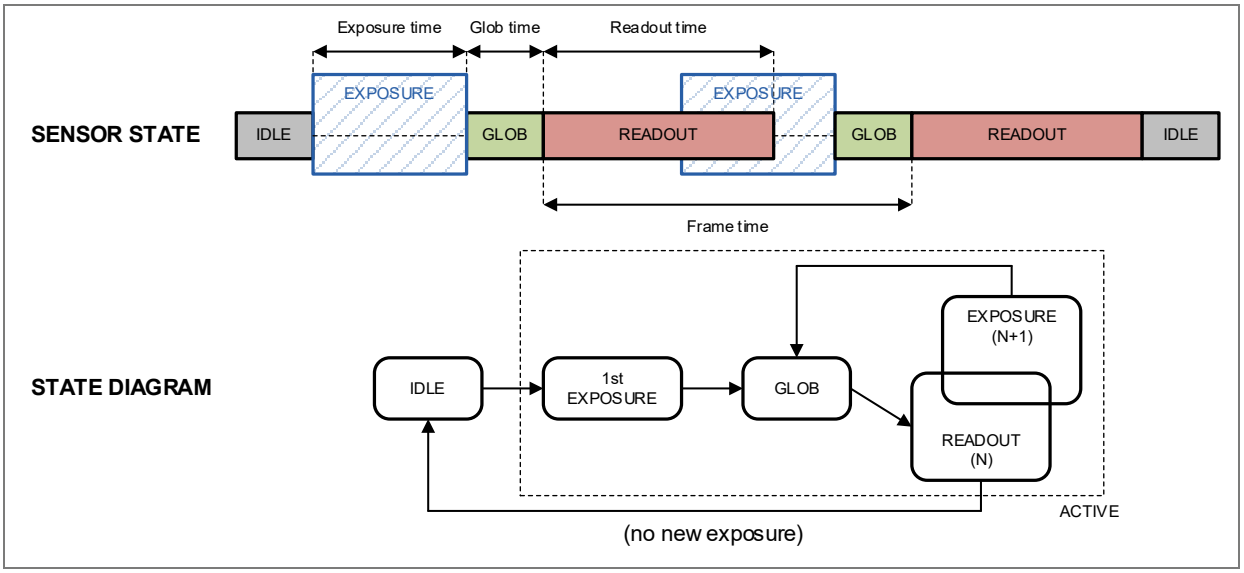
During image acquisition, the sensor moves through several states, as shown in Figure 22. After an external request, the sensor goes through a sequential succession of EXPOSURE – GLOB – READOUT to grab a single image. After this cycle, the sensor moves back to IDLE, waiting for new requests. Since only one frame is captured before returning to IDLE, this mode of operation is referred to as *sequential operation*. This means that the sensor moves through the states in a sequential manner, with only one state activated at any given time.

Figure 22: Sequential image acquisition



When multiple frames are acquired back-to-back without passing through IDLE state, the sensor operates in *pipelined mode*, as shown in Figure 23. In this mode, the sensor can be in the EXPOSURE state and READOUT state at the same time. While the readout of frame N is busy, the exposure of frame N+1 is already started. The EXPOSURE can partially overlap or fully overlap with the READOUT state. The time between two consecutive frames is called the *frame time*.

Figure 23: Pipelined image acquisition



Depending on the selected Sensor Control Mode, the exposure time and frame time are controlled through external timing or through register settings. Refer to section 6.8 for more information on the Sensor Control Modes. The readout time depends on the selected data rate, output interface configuration and region of interest.

6.7.1 Background light cancellation

Background Light Cancellation is a special sensor acquisition mode designed to handle very bright background conditions. As introduced in section 5.3.4, this involves two exposures, with an external illumination source alternatingly turned on or off, followed by a single image readout of the on-chip calculated difference image.

Information:

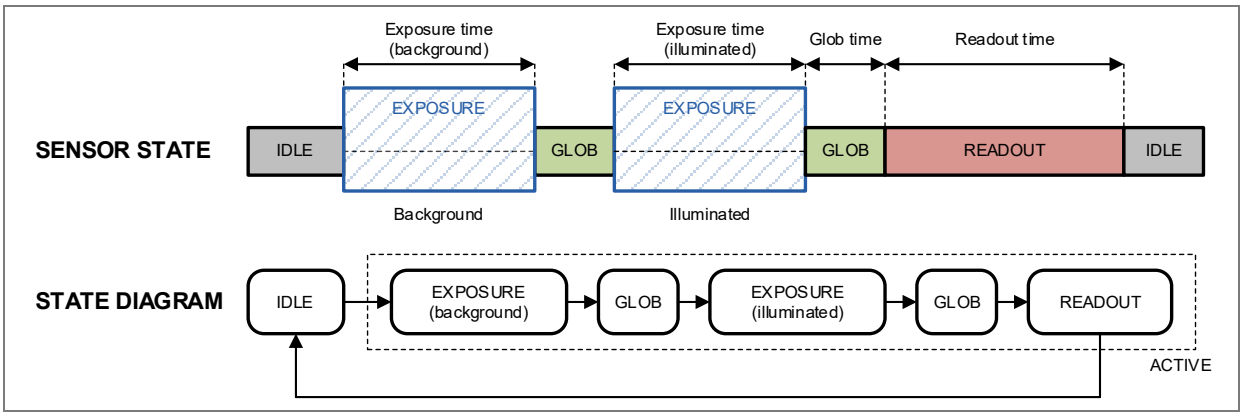
Use the sensor's Illumination Trigger to synchronize the external illumination source to the exposure of the illuminated scene. Refer Section 5.11.

Image acquisition in Background Light Cancellation mode is different from the normal operating mode as two exposure phases are needed for each readout. Each exposure is followed by a glob phase to sample the integrated pixel values of that exposure. Figure 24 shows the sequential image acquisition in Background Light Cancellation mode.

After an external request, the sensor goes through a sequential succession of EXPOSURE – GLOB – EXPOSURE – GLOB – READOUT to grab a single image. After this cycle, the sensor moves back to IDLE. The first EXPOSURE captures the background scene and the second EXPOSURE captures the illuminated scene. When enabled, the sensor's Illumination Trigger is activated during the second exposure. The READOUT phase reads out the difference image.

The exposure time of the background scene and the illuminated scene can be programmed independently.

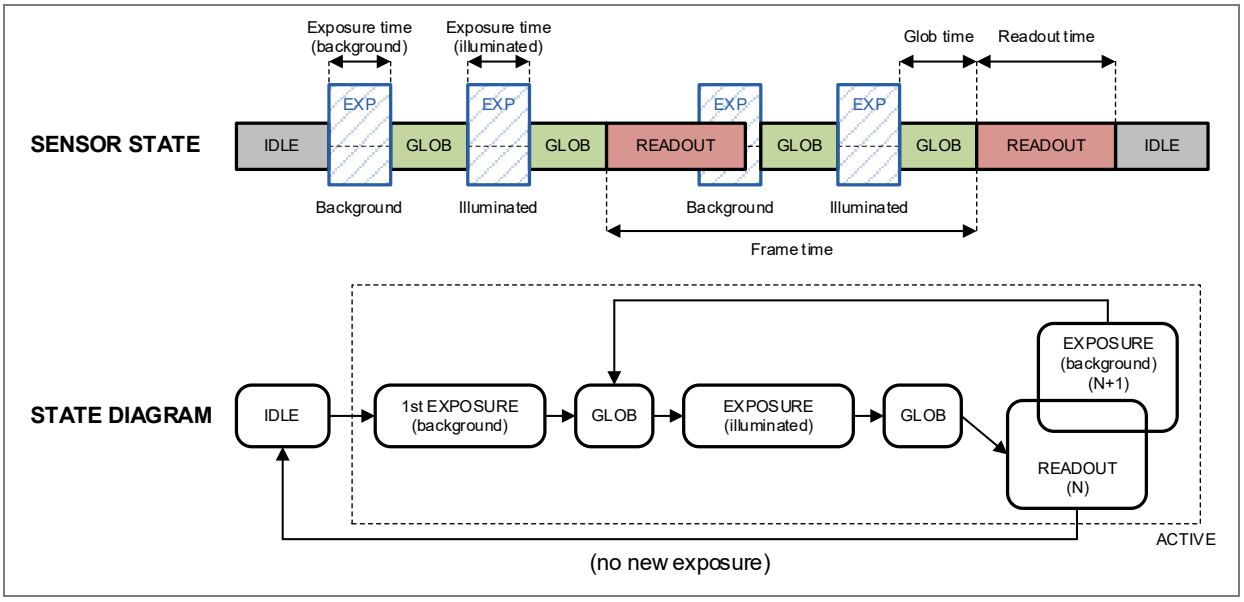
Figure 24: Sequential image acquisition with background light cancellation



Background Light Cancellation also supports pipelined image acquisition, as shown in Figure 25. While the readout of frame N is busy, the **background** exposure of frame N+1 is already started. The **background** EXPOSURE can partially overlap or fully overlap the READOUT state.

Background Light Cancellation uses a dedicated Sensor Control Mode called 'Background Light Cancellation'. Refer to section 6.8.4 for more details.

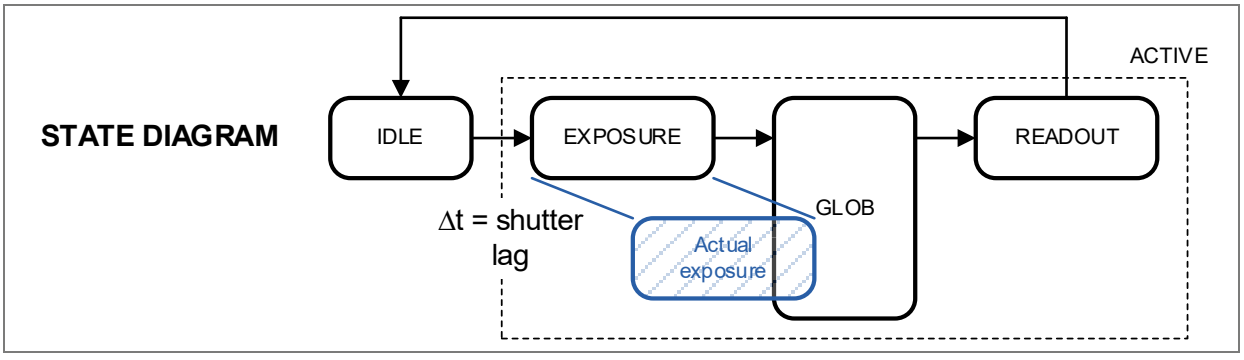
Figure 25: Pipelined image acquisition with background light cancellation



6.7.2 Shutter lag

The *shutter lag* is the time offset between the EXPOSURE state and the actual exposure on the pixel array. Figure 26 shows the state diagram for sequential image acquisition with the shutter lag annotated. Shutter lag is also present for pipelined image acquisition.

Figure 26: Sequential image acquisition with shutter lag



The actual exposure ends in the GLOB state when the integrated pixel values are sampled and the global shutter is closed. This sampling operation takes some time, which means the actual exposure does not end immediately at the start of the GLOB state, but somewhere

during the GLOB state. This *time overlap* between the actual exposure and GLOB causes the *shutter lag*.

By default, the sensor also introduces the shutter lag at the start of EXPOSURE to compensate for the time overlap. This is called *shutter lag matching* and acts as a delay between the external exposure request and the actual start of exposure on the pixel array.

Information:

Throughout this document, the terms “exposure” and “exposure time” always refer to the EXPOSURE state. Whenever the “actual exposure” is meant, it is explicitly referenced to as such.

6.8 Sensor control modes

This section details all Sensor Control Modes that are available to the user. Depending on the selected mode, the image acquisition is controlled differently. Choosing a Sensor Control Mode depends on the amount of desired external control and ease of use.

Modes Full External, Triggered Internal, and Streaming are used to control the image acquisition as shown in Figure 22 and Figure 23.

The Background Light Cancellation mode is a dedicated control mode for background light cancellation. It is used to control the image acquisition as shown in Figure 24 and Figure 25.

Table 8 gives a brief overview of the available Sensor Control Modes. Each mode is detailed in one of the following sections.

Table 8: Sensor control modes

Name	External control	Internal control
Full external	Start of exposure End of exposure (and start of readout)	Readout details
Triggered internal	A finite sequence of 1 or more consecutive frames	Length of exposure Frame rate Sequence length (number of frames) Readout details

Name	External control	Internal control
Background light Cancellation	A finite sequence of 1 or more consecutive frames using Background Light Cancellation	Length of background exposure Length of illuminated exposure Frame rate Sequence length (number of frames) Readout details Background Light Cancellation operation
Streaming	An infinite sequence of consecutive frames (until a HALT command is received)	Length of exposure Frame rate Readout details

6.8.1 Request commands

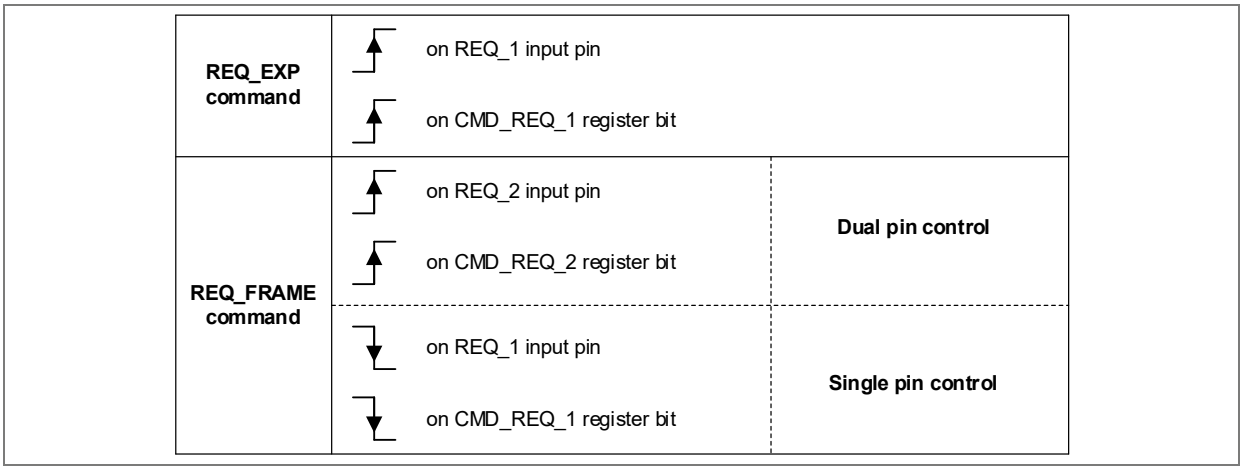
The sensor has two Request Commands to control image acquisition, named REQ_EXP and REQ_FRAME. The exact functionality of each command depends on the selected Sensor Control Mode. The Request Commands can be generated through the sensor's IO pins (this is referred to as *pin-controlled* operation) or through the CCI interface by setting certain register bits (this is referred to as *software-controlled* operation). By default, each Request Command is generated by its own sensor input pin or register bit. This is called *dual pin control*. It is also possible to generate both Request Commands from a single input pin or register bit. This is known as *single pin control*.

Figure 27 gives an overview of how the REQ_EXP and REQ_FRAME commands can be generated. The Request Commands are triggered by a rising or falling edge on the sensor input pin or register bit.

Information:

The REQ_2 sensor input pin is not available on the CSP package option. Use single pin control and/or software-controlled operation to generate the REQ_FRAME command.

Figure 27: Request command generation



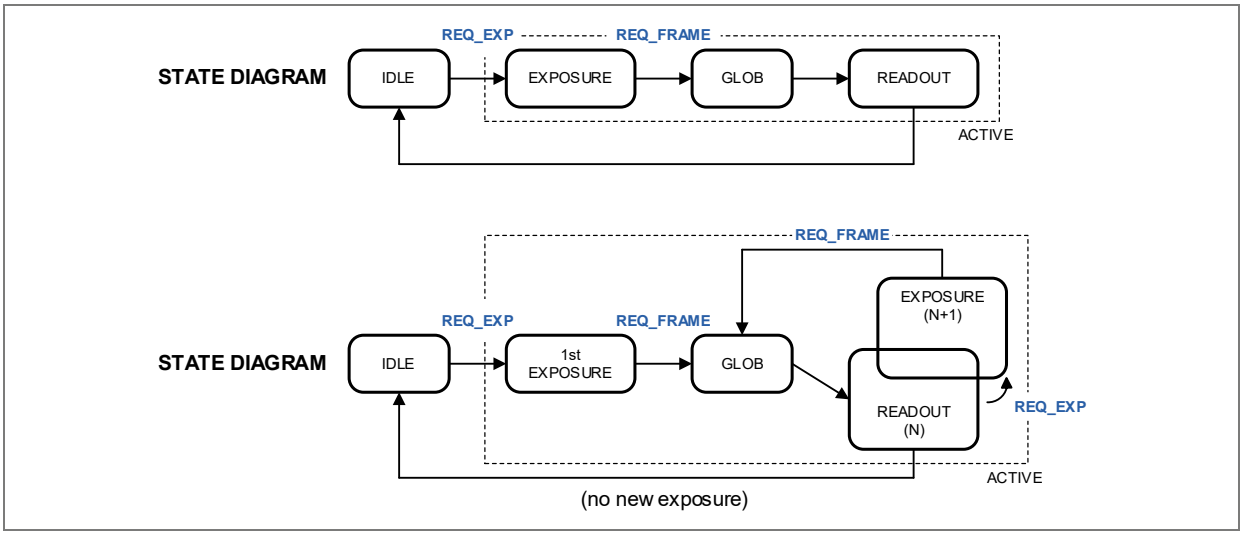
6.8.2 Full external

In the Full External control mode, all timing except the internal readout details is controlled through the REQ_EXP and REQ_FRAME commands. The REQ_EXP command moves the sensor to the EXPOSURE state. The REQ_FRAME command moves the sensor to the GLOB state, which is automatically followed by the READOUT.

The Full External mode provides maximum external control to the user. For example, the exposure can be started and ended at any time, and the exposure time can be varied from frame to frame. All requests commands are processed immediately with minimal latency. However, if the user applies improper timing to the sensor, corrupted frames and interrupted frame readouts may occur.

Figure 28 shows the state diagrams for sequential and pipelined image acquisition, with the request commands annotated.

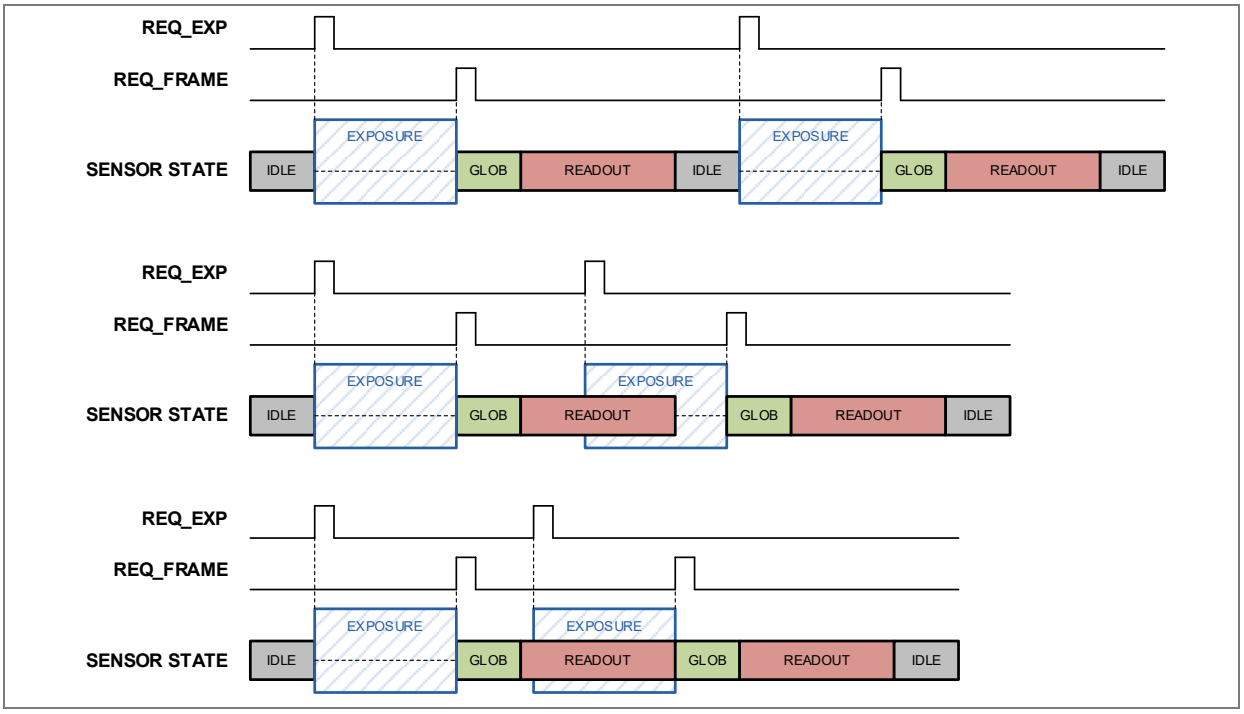
Figure 28: State diagrams in full external mode



The exposure time (i.e. length of the EXPOSURE state) is equal to the time between the REQ_EXP and REQ_FRAME commands. When multiple frames are acquired, the frame time is equal to the time between two REQ_FRAME commands. Figure 29 shows a timing diagram for some common situations. The different scenarios are described below:

- Operate the sensor in sequential mode.
- Operate the sensor in pipelined mode, with the parallel exposure extending beyond the readout phase.
- Operate the sensor in pipelined mode, with the parallel exposure ending together with the readout phase. This results in maximum frame rate.

Figure 29: Timing diagrams in full external mode



The flexible control timing of the Full External mode has some invalid timings that will result in corrupted image data. These corrupted images do not contain any useful data. All invalid control timings are shown in Table 9.

Table 9: Invalid control timing in full external mode

#	Invalid control timing	Sensor response
FE_i0	REQ_EXP during GLOB	Disrupts the GLOB execution, corrupting the data of the READOUT that follows that GLOB phase.
FE_i1	REQ_FRAME during GLOB	Initiates a new GLOB followed by READOUT. The image data in this READOUT is corrupt.
FE_i2	Two consecutive REQ_FRAME without REQ_EXP in between	The second REQ_FRAME initiates a new GLOB followed by READOUT. Since there was no EXPOSURE, the image data in the second frame is corrupt.
FE_i3	REQ_FRAME when sensor is IDLE	A GLOB is started followed by READOUT. Since there was no EXPOSURE, the image data is corrupt.

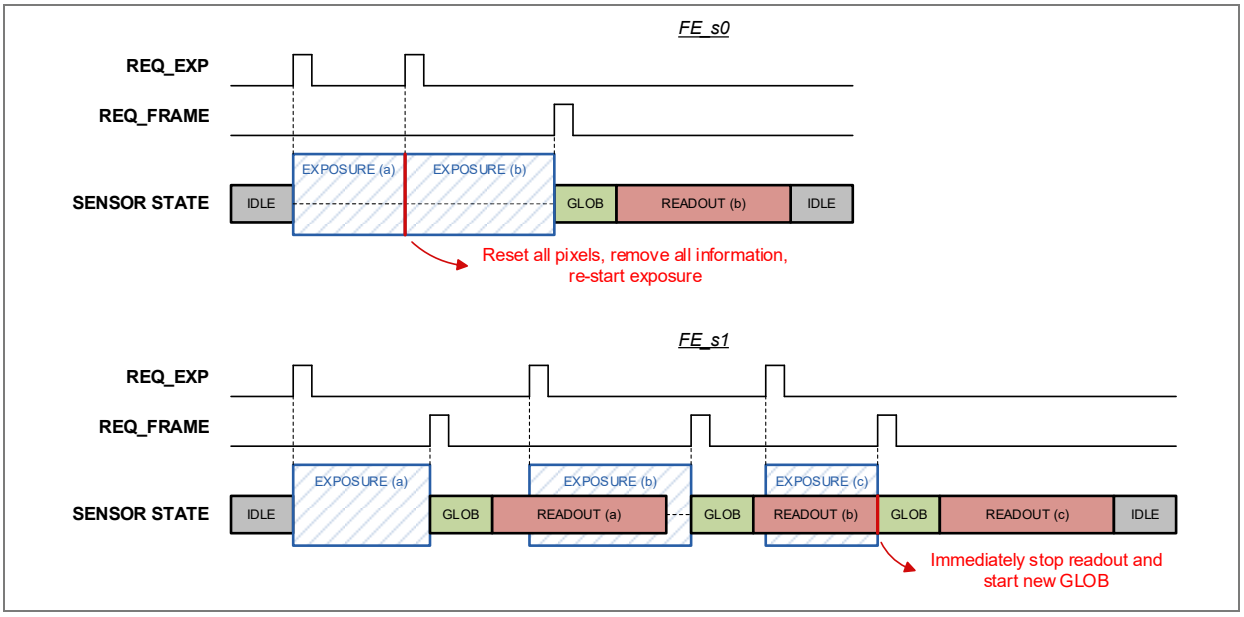
The Full External mode also has some special control timing, as shown in Table 10. These timings do not result in corrupted image data. However, data that was not yet read out is lost.

Table 10: Special control timing in full external mode

#	Special control timing	Sensor response
FE_s0	REQ_EXP during EXPOSURE	Initiates a new EXPOSURE, erasing all previously integrated information in the pixels. The next REQ_FRAME initiates a GLOB and READOUT that contains image data of only the second EXPOSURE.
FE_s1	REQ_FRAME during READOUT	Immediately interrupts the active READOUT to start a new GLOB (that is followed by another READOUT). The image data of the first READOUT that was not yet read is lost. The new READOUT contains valid data, if not violating FE_i2.

An example timing diagram for each of the special control timings is shown in Figure 30.

Figure 30: Special control timing diagrams in full external mode



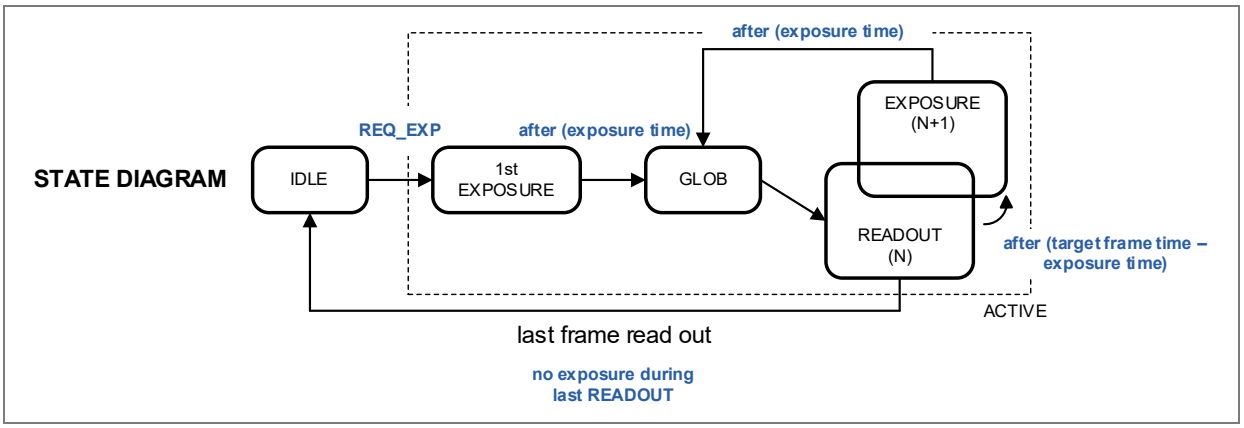
6.8.3 Triggered internal

In the Triggered Internal mode, a REQ_EXP command acquires a programmable number of frames, which are outputted at a programmable (target) frame rate. The exposure time of all frames is also programmed in the sensor. All REQ_FRAME commands are ignored in this control mode.

Figure 31 shows the state diagram in Triggered Internal mode with different events annotated. When the sensor is IDLE, a REQ_EXP command starts the first EXPOSURE of a sequence of frames. When the programmed exposure time elapses, the sensor automatically moves to the

GLOB state, which is followed by the READOUT state. The behavior in the READOUT state depends on the number of requested frames (set by register upload) and the amount of frames that have already been read during the active sequence. If the requested amount of frames is not yet reached, the sensor will start a new EXPOSURE for the next frame. The start of this EXPOSURE is timed in such a way that the time between two consecutive frames is equal to the programmed (target) frame time. After the last READOUT of a requested sequence, the sensor moves back to IDLE. No new EXPOSURE is started during the last READOUT.

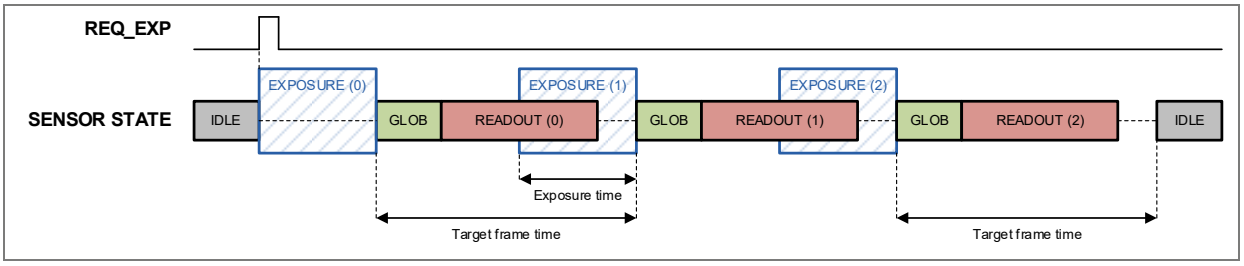
Figure 31: State diagram in triggered internal mode



An example timing diagram for the Triggered Internal mode is shown in Figure 32. The programmed amount of frames in this example is three. A REQ_EXP command starts the acquisition of these three frames. The time between each frame is the target frame time and is programmed in the sensor. Note that after the last frame READOUT, the sensor only returns to IDLE when the target frame time is elapsed.

To achieve maximum frame rate, the target frame time should be equal to the glob time plus the readout time. In that case, a new GLOB is started as soon as the previous READOUT is finished.

Figure 32: Timing diagram in triggered internal mode



The Triggered Internal mode has no invalid control timing. The special control timing is shown in Table 11. None of these cases results in data loss and there is no risk of corrupted image data.

Table 11: Special control timing in triggered internal mode

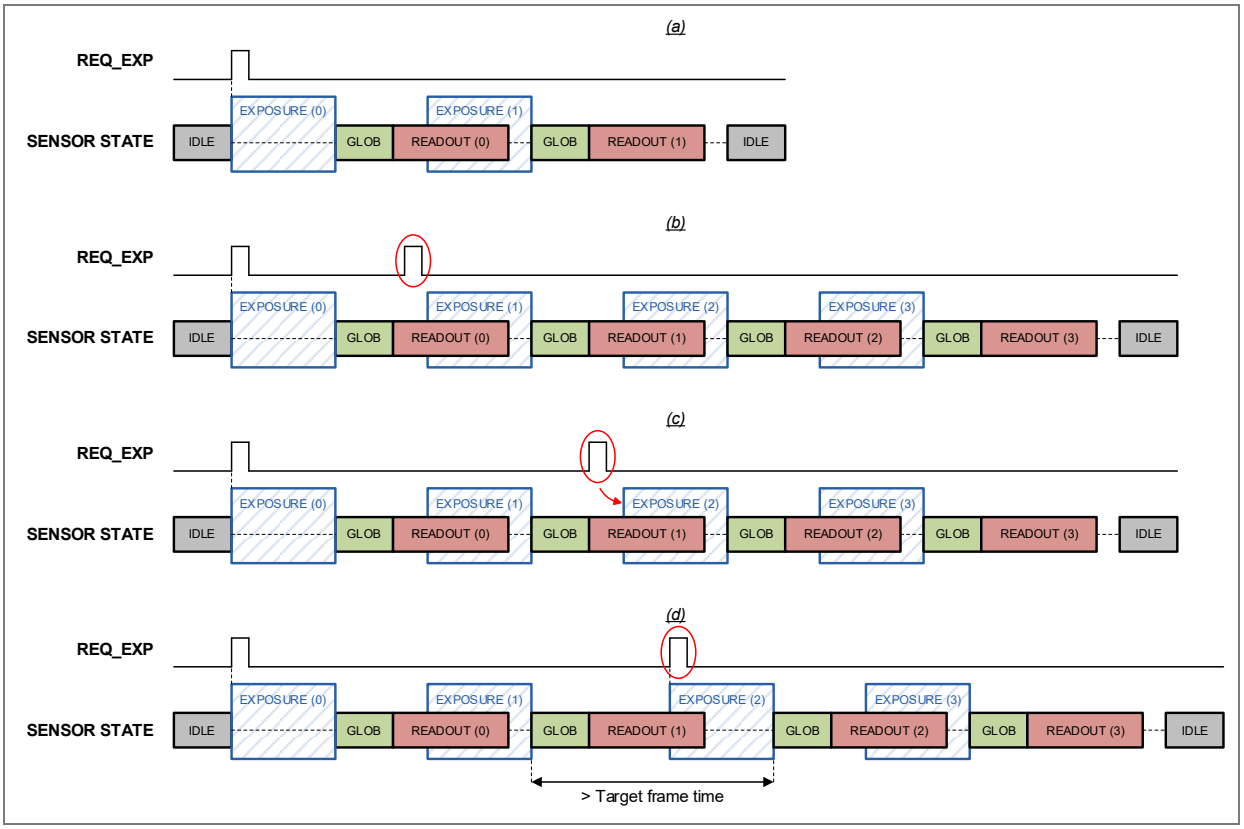
#	Special control timing	Sensor response
TI_s0	REQ_EXP **before** last READOUT of sequence started	Increases the active sequence length by the requested amount of frames. The maximum active sequence length is 255.
TI_s1	REQ_EXP **after** last READOUT of sequence started	Initiates a new 'first' EXPOSURE, followed by a complete new sequence. Depending on the timing of the new request, the frame rate may temporarily change.
TI_s2	REQ_FRAME command	The request is ignored.

The behavior of TI_s0 and TI_s1 is illustrated with some examples as shown in Figure 33. All examples use a sequence length of two frames. The different scenarios are:

1. Normal timing: After a REQ_EXP command, two frames are acquired. The sensor returns to IDLE after the frames are acquired.
2. TI_s0: A new request arrives **before** the last READOUT started. The sequence is extended by two frames. The sensor will output four frames in total before returning to IDLE.
3. TI_s1: A new request arrives **after** the last READOUT started. The sequence is extended by two frames. The new EXPOSURE start is delayed to maintain the programmed target frame time.
4. TI_s1: A new request arrives **after** the last READOUT started. The sequence is extended by two frames. The new EXPOSURE starts immediately and the frame rate is temporarily decreased to allow the exposure time to elapse.

The behavior of TI_s1 depends on when the new request arrives during the last READOUT. When the exposure time is smaller than the remaining frame time, the new exposure is delayed. This is shown in case (3). When the exposure time is larger than the remaining frame time, the new exposure starts immediately. This causes a temporary drop in frame rate, as shown in case (4).

Figure 33: Special control timing diagrams in triggered internal mode



6.8.4 Background light cancellation

In the Background Light Cancellation mode, a REQ_EXP command acquires a programmable number of frames, which are outputted at a programmable (target) frame rate. All frames are acquired using on-chip Background Light Cancellation. The exposure time of the background and illuminated exposure is programmed in the sensor. Both exposure times can be set independently. All REQ_FRAME commands are ignored in this control mode.

Information:

The Background Light Cancellation mode is very similar to the normal Triggered Internal mode. The key differences are:

- Background Light Cancellation performs two exposure phases in order to do the on-chip Background Light Cancellation operation.
- With similar settings, the maximum achievable frame rate in Background Light Cancellation mode is lower. This is because of the additional exposure (and accompanying glob) phase.
- Two exposure times have to be programmed in the Background Light Cancellation mode. One for the background exposure and one for the illuminated exposure.

Figure 34 shows the state diagram in Background Light Cancellation mode with different events annotated. When the sensor is IDLE, a REQ_EXP command starts the first **background** EXPOSURE of a sequence of frames. When the programmed background exposure time elapses, the sensor automatically moves to the first GLOB state. After this, the **illuminated** EXPOSURE is started. The sensor moves to the second GLOB state after the programmed illuminated exposure time, which is then followed by the READOUT state.

The behavior in the READOUT state depends on the number of requested frames (set by register upload) and the amount of frames that have already been read during the active sequence. If the requested amount of frames is not yet reached, the sensor will start a new **background** EXPOSURE for the next frame. After the last READOUT of a requested sequence, the sensor moves back to IDLE. No new EXPOSUREs are started during the last READOUT.

Figure 34: State diagram in background light cancellation mode

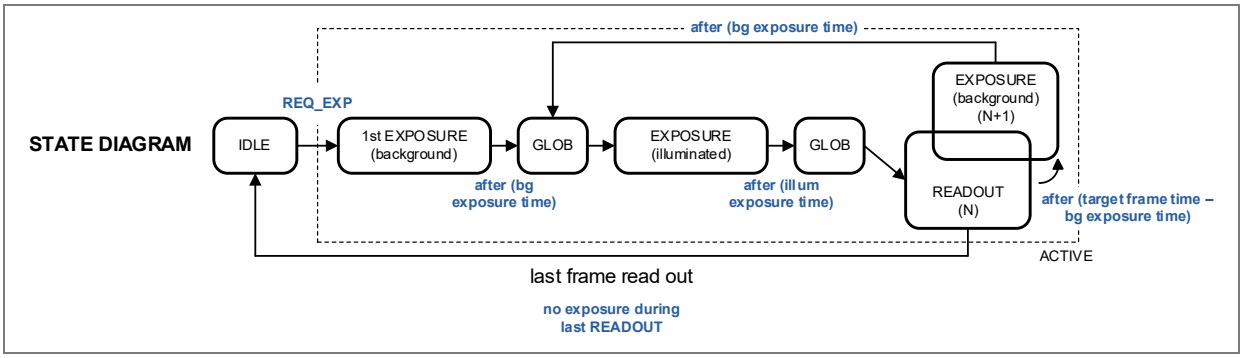


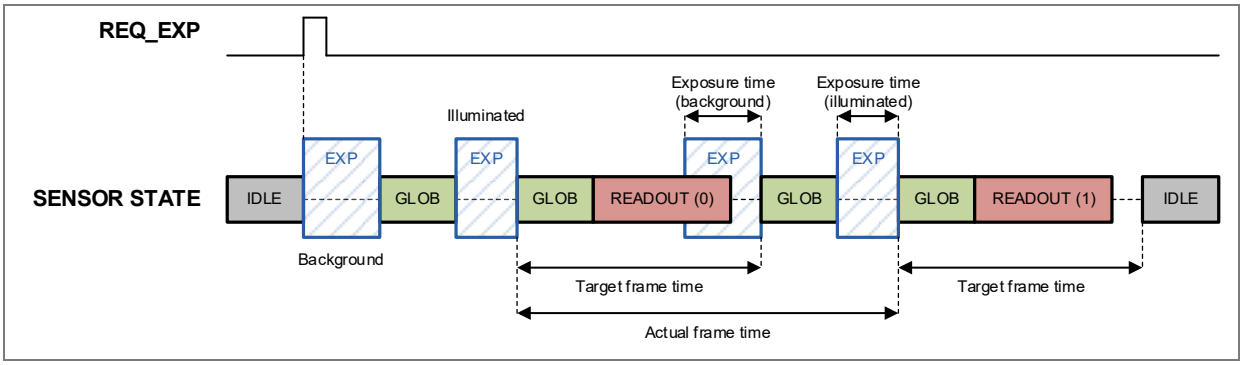
Figure 35 shows an example timing diagram for the Background Light Cancellation mode. The programmed amount of frames in this example is two. A REQ_EXP command starts the acquisition of these two frames. The actual frame time (as seen on the output interface) is

greater than the programmed target frame time because of the additional EXPOSURE/GLOB phase. The actual frame time is the programmed target frame time plus the illuminated exposure time and the glob time.

Note that after the last frame READOUT, the sensor only returns to IDLE when the target frame time is elapsed.

To achieve maximum frame rate, the target frame time should be equal to the glob time plus the readout time.

Figure 35: Timing diagram in background light cancellation mode



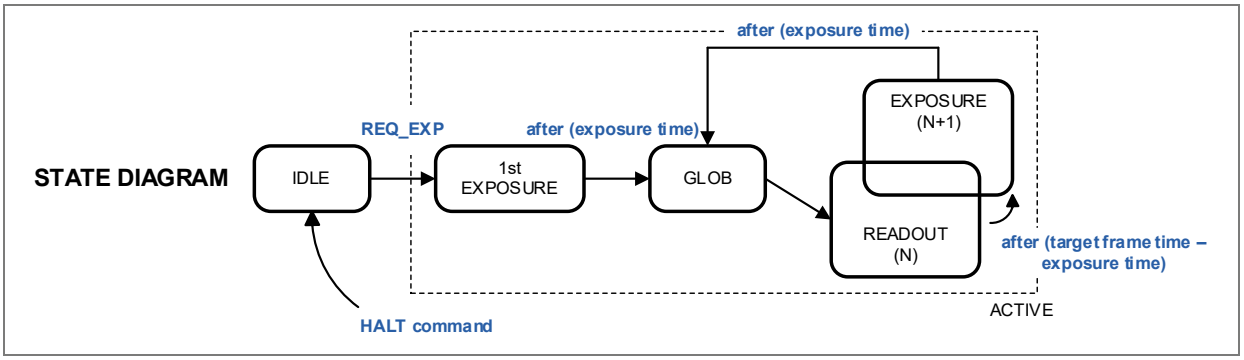
The Background Light Cancellation mode has no invalid control timing. The special control timing is identical to the normal Triggered Internal mode, as shown in Figure 33.

6.8.5 Streaming

In the Streaming mode, a REQ_EXP command starts the acquisition of an infinite amount of frames. The frames are outputted at a programmable (target) frame rate. The exposure time is also programmed in the sensor. The Streaming mode behaves like the Triggered Internal mode with an infinite sequence length. All REQ_FRAME commands are ignored in this control mode.

Figure 36 shows the state diagram for Streaming mode with different events annotated. After the first EXPOSURE is started, the sensor cycles indefinitely between READOUT/EXPOSURE and GLOB to acquire new frames. To exit Streaming mode, the user has to upload a HALT *software command* to the sensor. This puts the sensor back in the IDLE state. Refer to section 6.9 for more information about software commands.

Figure 36: State diagram in streaming mode



The Streaming mode has no invalid control timing and no special control timing. After entering the Streaming mode, all REQ_EXP commands are ignored.

6.9 Software commands

Software commands are internal sensor commands that are triggered through register upload. Table 12 gives an overview of all available software commands.

The CMD_HALT_BLOCK command can be used to get the sensor out of Streaming mode without a need to reset the on-chip logic.

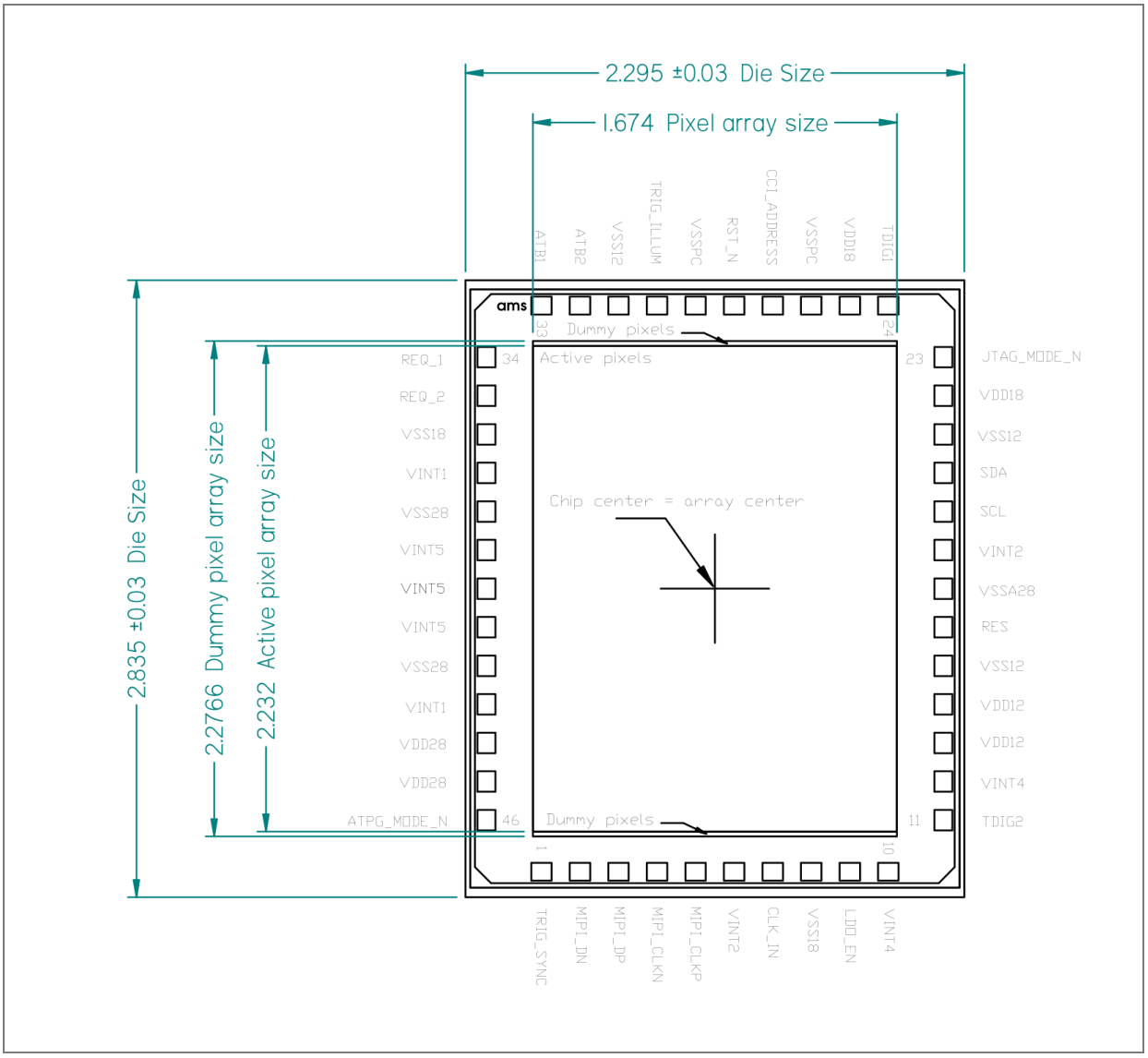
Table 12: Software commands

Software command	Description
CMD_REQ_1	A rising edge on this bit triggers a REQ_EXP command. When using *single pin control*, a falling edge on this bit triggers a REQ_FRAME command. See section 6.8.1 for details on request commands.
CMD_REQ_2	When using *dual pin control*, a rising edge on this bit triggers a REQ_FRAME command. See section 6.8.1 for details on request commands.
CMD_HALT_BLOCK	A rising edge on this bit triggers a blocking halt command. The sensor finishes the active frame readout and moves to the IDLE state afterwards.
CMD_ENTER_LP_STATE	Manual Low Power State (LPS) entry. A rising edge on this bit starts the LPS entry sequence.
CMD_EXIT_LP_STATE	Manual Low Power State (LPS) exit. A rising edge on this bit starts the LPS exit sequence.

7 Pin and package information

7.1 Bare die pin diagram

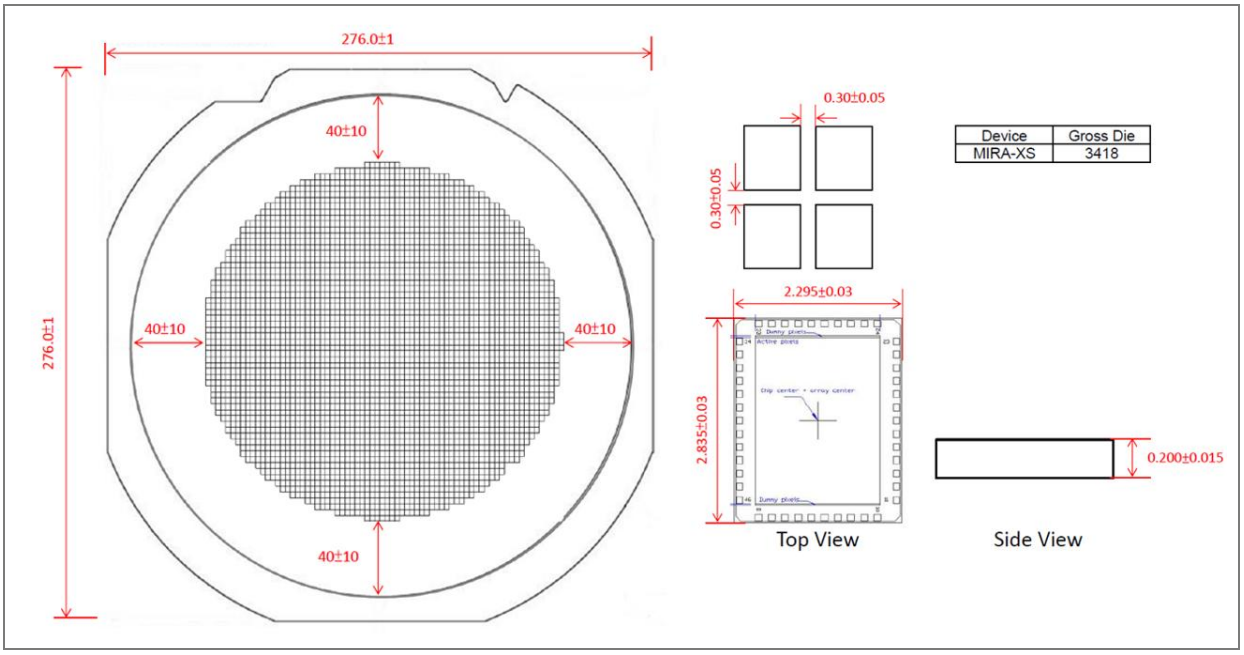
Figure 37: Mira050 pad names



(1) All dimensions are in mm.

7.2 Reconstructed wafer (bare die)

Figure 38: RW physical dimensions and die information



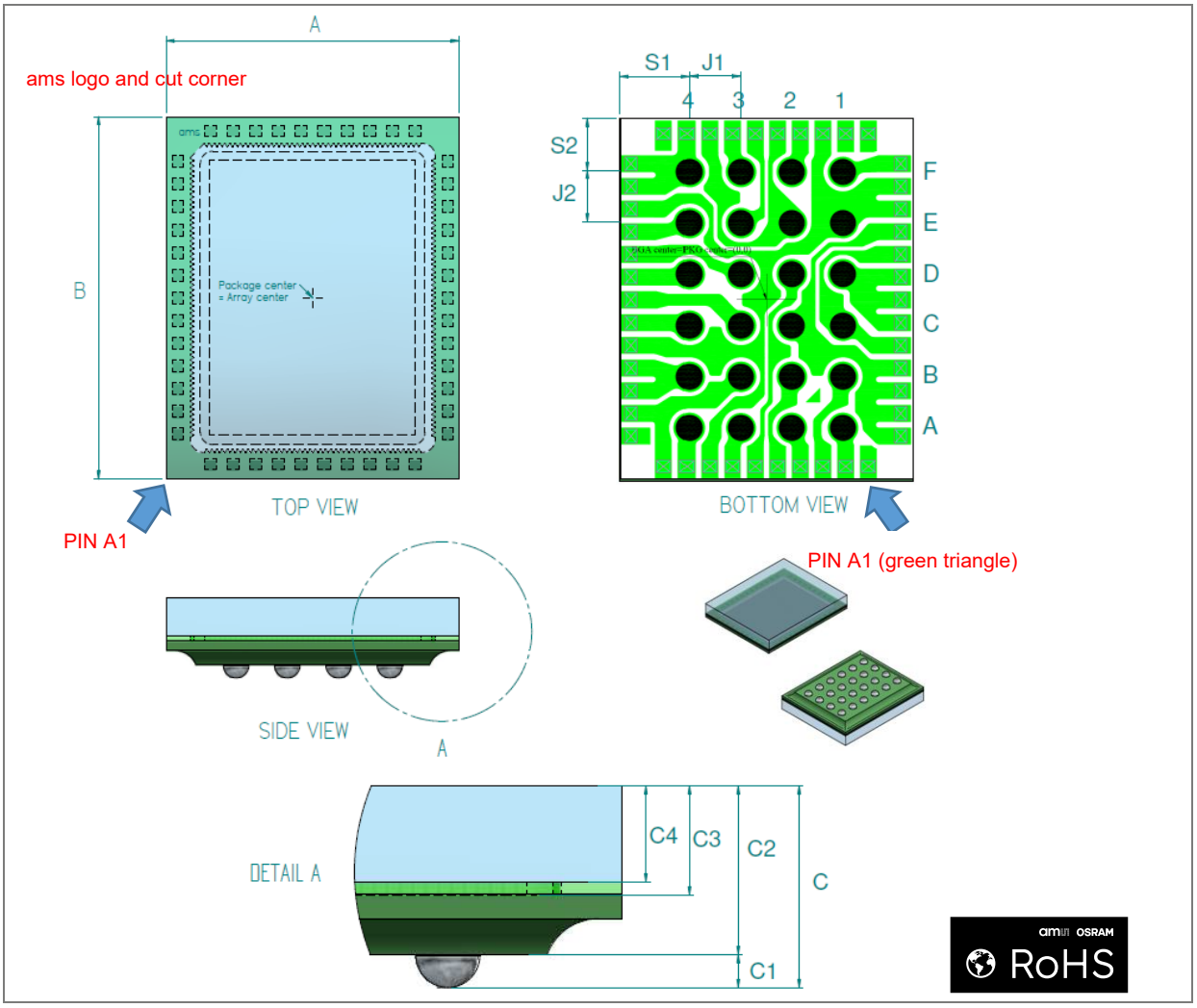
(1) All dimensions are in mm.

Table 13: Bondpad information

Bondpad specification	Data	Comment
Pad pitch	177.3 µm	Constant pitch on each side
Pad size	92 µm x 75 µm	Top aluminum metallization size
Pad opening	111 µm x 96 µm	Silicon opening around bond pad
Pad recess	4 µm	Recess from silicon surface

7.3 CSP package information

Figure 39: CSP package outline drawing(1)



(1) The ams Logo and cut corner (top) or the arrow on pin A1 (bottom) can be used for orientation purposes.
(2) All dimensions are in millimeters. Angles in degrees.
(3) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(4) N is the total number of terminals.
(5) This package contains no lead (Pb).
(6) This drawing is subject to change without notice.

Table 14: Package dimensions

Dimension	Symbol	Nominal	Min	Max	Tolerance
Package body dimensions X	A	2.29 mm	2.265 mm	2.315 mm	0.025 mm
Package body dimensions Y	B	2.83 mm	2.805 mm	2.855 mm	0.025 mm
Pixel array size X		1.607 mm	1.607 mm	1.607 mm	0 mm
Pixel array size Y		2.143 mm	2.143 mm	2.143 mm	0 mm
Package height	C	0.640 mm	0.580 mm	0.700 mm	0.06 mm
Ball height	C1	0.11 mm	0.08 mm	0.14 mm	0.03 mm
Package body thickness	C2	0.530 mm	0.500 mm	0.560 mm	0.03 mm
Thickness from top glass to wafer	C3	0.345 mm	0.330 mm	0.360 mm	0.015 mm
Glass thickness	C4	0.3 mm	0.29 mm	0.31 mm	0.01 mm
Ball diameter	D	0.2 mm	0.17 mm	0.23 mm	0.03 mm
Ball count	N	24			
Ball pitch X	J1	0.4 mm			
Ball pitch Y	J2	0.4 mm			
Side X	S1	0.545 mm	0.515 mm	0.575 mm	0.03 mm
Side Y	S2	0.4149 mm	0.3849 mm	0.4449 mm	0.03 mm

Table 15: Connectivity table CSP package

CSP bump	Pin name
A1	MIPI_DN
A2	MIPI_CLKN
A3	CLK_IN
A4	LDO_EN
B1	MIPI_DP
B2	MIPI_CLKP
B3	VINT4
B4	VDD12
C1	VSS28
C2	VDD28
C3	VSSA28
C4	RES

CSP bump	Pin name
D1	VINT5
D2	VINT2
D3	SCL
D4	VINT2
E1	VSS18
E2	VINT6
E3	RST_N
E4	SDA
F1	REQ_1
F2	TRIG_ILLUM
F3	CCI_ADDRESS
F4	VDD18

7.4 Detailed pin description

Table 16: Detailed pin description

Pin number		Pin name	Pin type[1]	Description
Bare die	CSP			
7	A3	CLK_IN	DI	CMOS input clock to PLL
28	E3	RST_N	DI	Hard reset
20	E4	SDA	DIO	CCI data
19	D3	SCL	DI	CCI clock
34	F1	REQ_1	DIO	Tie to ground if unused. Request exposure in dual-pin full-external mode/ Request exposure and frame readout in single-pin full-external mode.
35	E1	REQ_2	DI	Request frame readout in dual-pin full-external mode Not available on CSP
23	F4	JTAG_MODE_N	DI	JTAG pin compliancy select. When not in use Tie High Tied to VDD18 on CSP
46	C2	-	DI	Bare Die – Tie High CSP – Tied to VDD28
3	B1	MIPI_DP	HSO	MIPI data out P

Pin number		Pin name	Pin type[1]	Description
Bare die	CSP			
2	A1	MIPI_DN	HSO	MIPI data out N
5	B2	MIPI_CLKP	HSO	MIPI clock out P
4	A2	MIPI_CLKN	HSO	MIPI clock out N
24	-	TDIG1	DO	Digital test bus not connected on CSP
11	-	TDIG2	DO	Digital test bus not connected on CSP
30	F2	TRIG_ILLUM	DO	Light source trigger
1	-	TRIG_SYNC	DO	Slave trigger. Not connected on CSP
33	-	-	NC	Not Used
32	-	-	NC	Not Used
9	A4	LDO_EN	DI	Enables LDO
27	F3	CCI_ADDRESS	DI	CCI device address configuration
44, 45	C2	VDD28	S	Analog Supply
37, 43	C2	VINT1	S	CSP – tied to VDD28
17	C3	VSSA28[2]	G	Analog ground
22, 25	F4	VDD18	S	DIG IO supply
8, 36	E1	VSS18[2]	G	DIG IO ground
13, 14	B4	VDD12	S	Core supply
15, 21, 31	E1	VSS12[2]	G	Core ground
16	C4	RES	A	External resistor pin
6, 18	D2, D4	VINT2	C	Internally generated supply, pins are shorted externally
10, 12	B3	VINT4	C	Internally generated supply
39, 40, 41	D1	VINT5	C	Internally generated supply
42, 38	C1	VSS28[2]	G	Second analog ground
26, 29	E2	VINT6	C	

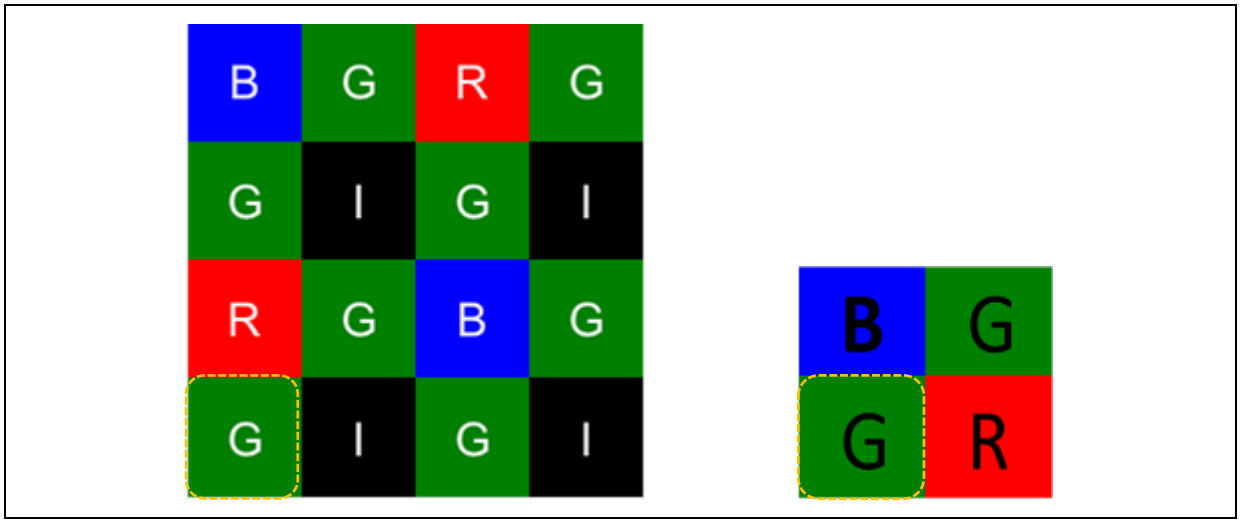
(1) Abbreviations
S-Supply
G-Ground
DI-Digital input
DO-Digital output
DIO-Digital input/output
HSO-High speed output
A-Analog reference
NC-No connect

(2) VSSA28, VSS18, VSS12 and VSS28 can be shorted if there are constraints on routing on PCB.

8 Color filter information

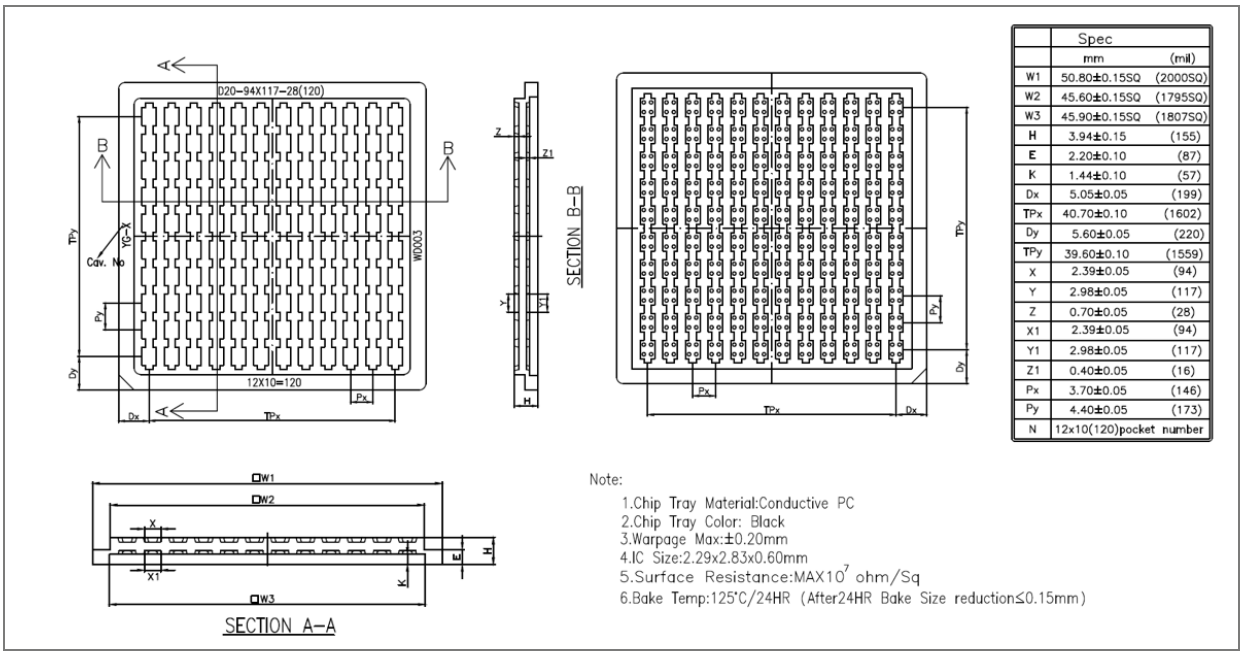
The following Figure 40 shows the color filter configuration used on the Mira050 both for RGB and RGBIR versions of the sensor. The first readout pixel is highlighted below.

Figure 40: Color filter configurations for RGB-IR (left) and RGB (right)



9 Tray information - CSP

Figure 41: Tray dimension information - CSP



	Spec	
	mm	(mil)
W1	50.80±0.15SQ	(2000SQ)
W2	45.60±0.15SQ	(1795SQ)
W3	45.90±0.15SQ	(1807SQ)
H	3.94±0.15	(155)
E	2.20±0.10	(87)
K	1.44±0.10	(57)
Dx	5.05±0.05	(199)
TPx	40.70±0.10	(1602)
Dy	5.60±0.05	(220)
TPy	39.60±0.10	(1559)
X	2.39±0.05	(94)
Y	2.98±0.05	(117)
Z	0.70±0.05	(28)
X1	2.39±0.05	(94)
Y1	2.98±0.05	(117)
Z1	0.40±0.05	(16)
Px	3.70±0.05	(146)
Py	4.40±0.05	(173)
N	12x10(120)pocket number	

(1) All dimensions are in mm.
(2) Chip tray material: Conductive PC.
(3) Chip tray material: Black.
(4) Warpage max: ±0.20 mm.
(5) IC size: 2.29x2.83x0.60mm.
(6) Surface resistance: MAX 10^7 ohm/Sq.
(7) Bake temp: 125°C/24hr (after 24hr bake size reduction ≤ 0.15 mm).

10 Appendix

10.1 Reference documents

Table 17: Referenced documents

Reference	Document title	Revision / Date
PD001051	Mira050 product description	-
AN001056	Mira050 fine analog gains	-
CSI-2-v1.3	MIPI alliance specification for Camera Serial Interface 2 (CSI-2)	1.3
CSI-2-v2.0	MIPI alliance specification for Camera Serial Interface 2 (CSI-2)	2.0
DPHY-v1.2	MIPI alliance specification for D-PHY	1.2

10.2 Glossary

Table 18: Glossary

Abbreviation	Definition
ACK	Acknowledge
ADC	Analog to Digital Convertor
AR	Augmented Reality
BSI	Back-Side Illumination
BSP	Black Sun Protection
CCI	Camera Control Interface
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide Semiconductor
CRA	Chief Ray Angle
CRC	Cyclic Redundancy Check
CS	Checksum
CSI	Camera Serial Interface
CSP	Chip Scale Package
DC	Dark Current
DCDT	Dark Current Doubling Temperature
DCDS	Digital Correlated Double Sampling
D-PHY	MIPI Physical Layer Protocol

Abbreviation	Definition
DR	Dynamic Range
DSNU	Dark Signal Non Uniformity
DTN	Dark Temporal Noise
ECC	Error Correction Code
EOF	End of Frame
EOI	End of Integration
EOL	End of Line
ESD CDM	Electrostatic Discharge Charge Device Model
ESD HBM	Electrostatic Discharge Human Body Model
FE	Frame End
FPS	Frames per Second
FS	Frame Start
FWC	Full Well Capacity
GLOB	Closing global shutter state by sampling all integrated pixel values
HS	High Speed
IO	Input-Output
LP	Low Power
LS	Line Start
LSB	Least Significant Bit
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NACK	Not Acknowledge
NIR	Near Infrared
OTP	One Time Programmable
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PLS	Parasitic Light Sensitivity
PRNU	Pixel Response Non-Uniformity
QE	Quantum Efficiency
RH	Relative Humidity
RMS	Root Mean Square
RNC	Row Noise Correction
ROI	Region of Interest
RW	Reconstructed Wafer
SCL	Serial Clock
SDA	Serial Data

Abbreviation	Definition
SNR	Signal-to-Noise Ratio
SOF	Start of Frame
SOI	Start of Integration
ULPS	Ultra-Low Power State
VC	Virtual Channel
VPTAT	Voltage Proportional to the Temperature
VR	Virtual Reality

11 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Changes from previous released version to current revision v9-01	Page
Changes from v8-00 to v9-00	
Updated document security class to “PUBLIC” from “CONFIDENTIAL”	
Changes from v9-00 to v9-01	
Updated figure 39	49
Corrected package dimensions	50

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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