Product Document

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Application Note

AN000611

NanEyeC MCU Interface

Single Ended Interface Mode for Standard MCUs

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Content Guide

1 Introduction

NanEyeC is a miniature image sensor with a resolution of 320 x 320 pixels designed for space-constrained vision applications. This application note focuses on the single ended interface mode (SEIM). It is designed to connect NanEyeC directly to standard microcontrollers via short connections and without the need for additional electronics.
Full details about the NanEyeC sensor and its configuration are provided in the NanEyeC datasheet DS000503.

2 NanEyeC SEIM

2.1 Single Ended Interface Mode

In addition to LVDS mode, NanEyeC supports a single ended interface mode (SEIM) allowing ams OSRAM customers to connect the image sensor to standard microcontroller units (MCU). The SEIM uses a clock line (SCLK), which is driven by the MCU, and a data line (SDAT) which is driven by the MCU during INTERFACE MODE periods and by NanEyeC during all other operation mode periods.

2.2 Word and Frame Format

Transmission between NanEyeC and an MCU is performed in 12-bit words. Such a 12-bit word is subsequently also referred to as a pixel period (PP).
A PP consisting of a start bit (1-bit) + data (10-bit) + stop bit (1-bit) as shown in Figure 1.

Figure 1:
Pixel Data Word Encoding SEIM

# Rising SCLK Edge	0	1	2	3	4	5	6	7	8	9	10	11
Function	Start	Pixel Data (10 bits)										Stop
Content	1	MSB									LSB	0

A frame consist of 320 lines. Each line starts with 8 training PPs (cp. Figure 2) followed by 320 pixel data PPs (cp. Figure 1). Each frame is terminated by 8 end of frame PPs (EOF; see Figure 3). Hence, a frame transmitted by NanEyeC consists of 320 (lines) x 328 PPs (line data) + 8 PPs (EOF).

Figure 2:
Training Word Encoding SEIM (0x555)

# Rising SCLK Edge	0	1	2	3	4	5	6	7	8	9	10	11
Function	Start	Training Pattern (10 bits)										Stop
Content	0	1	0	1	0	1	0	1	0	1	0	1

Figure 3:
End Of Frame Word Encoding SEIM (0x000)

# Rising SCLK Edge	0	1	2	3	4	5	6	7	8	9	10	11
Function	Start	End of Frame Pattern (10 bits)										Stop
Content	0	0	0	0	0	0	0	0	0	0	0	0

2.3 Sequence of Operation

As shown in Figure 4, each frame is preceded by an INTERFACE MODE period (648 PPs), a SYNC MODE period of 2 x 328 PPs and a DELAY MODE period of [2 to 498] x 328 PPs. An exception is the first frame after power-on reset. This frame is not preceded with a full INTERFACE MODE period but with a shorter, INITIAL INTERFACE MODE period followed by an INITIAL PRE-SYNC MODE.

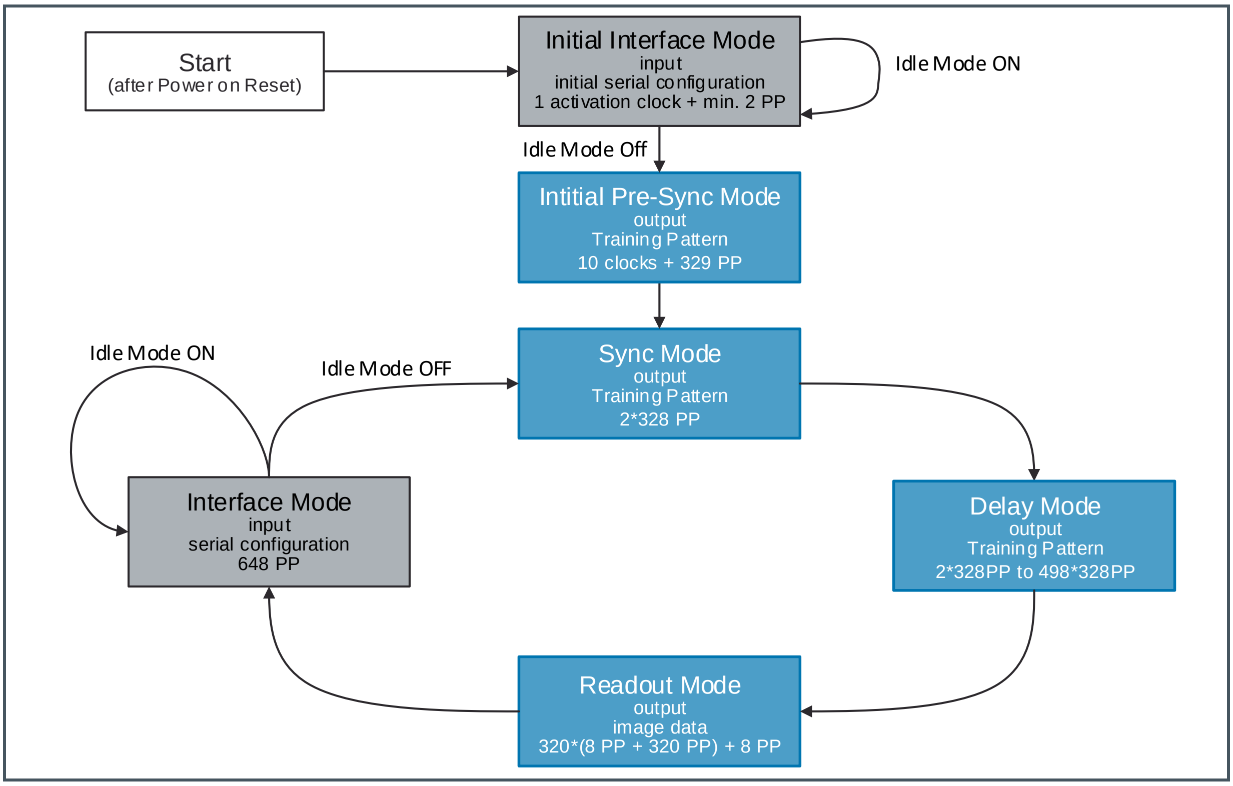
Operation Sequence Modes (as shown in Figure 4):

- **INITIAL INTERFACE MODE** consists of a single clock and a minimum of 2 PPs. The 2 PPs are used to write to NanEyeC register CONFIGURATION_1 (enable SEIM, disable IDLE mode, and other optional settings). Once IDLE mode is disabled, NanEyeC transitions to INITIAL PRE-SYNC MODE.
- **INITIAL PRE-SYNC MODE** consists of 10 clock periods plus 329 PPs. During INITIAL PRE-SYNC MODE, a fixed pattern is transmitted where one PP reads as 0xAAA.
- **INTERFACE MODE** consists of 648 PPs. Interface mode is used to write settings to the two NanEyeM registers. Register writes must not be performed in the last PP of interface mode!
- **SYNC MODE** consists of 2 x 328 = 656 PPs. During SYNC MODE, NanEyeC transmits a fixed training pattern of 0x555 (cp. Figure 2). Only for the first frame after power-on reset the pattern 0xAAA is transmitted instead.
- **DELAY MODE** increases exposure and frame rate by adding a delay ranging from a minimum of 2 x 328 PPs up to 498 x 328 PPs prior to frame readout. Note that including the minimum delay of 2 x 328 PPs in the operation sequence is mandatory.
- **READOUT MODE** is the period where NanEyeC transmits actual pixel data. Data transmission consists of 320 lines where each line starts with 8 PPs of training pattern (8 x 0x555) followed by 320 PP of pixel data. Note that the training pattern for the first line of the first frame after power-on reset is 0xAAA instead of 0x555.
- **INTERFACE MODE** consists of 648 PPs. Interface mode is used to write settings to the two NanEyeC registers.

Attention

Register writes must not be performed in the last PP of the INTERFACE MODE!

Figure 4:
Sequence Of Operation



2.4 NanEyeC Register Access

NanEyeC provides two write-only configuration registers which can be written during the INITIAL INTERFACE MODE and the normal INTERFACE MODE. A register write is performed as a 24-bit (2PP) write operation by the MCU. The content of the register update packet is structure as shown in Figure 5.

Figure 5:
Register Update Sequence

# Rising SCLK Edge	0	1	2	3	4	5	6	7	8	…	21	22	23
Function	Update Code				Register Address			Register Content (16 bits)					End
Content	1	0	0	1	**0**	**0**	**x**	MSB		…		LSB	0

For a detailed description of the NanEyeC register settings please refer to the NanEyeC datasheet DS000503. The most important actions for SEIM mode (applied during INITIAL INTERFACE MODE) are setting the output_mode[0] from LVDS (default) to SEIM and to disable idle_mode[0]. Both bits are located in the register **CONFIGURATION_1**.

3 MCU-Based SEIM Implementation

3.1 MCU Interface

To capture frames efficiently with a standard MCU, using a hardware peripheral is recommended instead of bit banging. A widely available MCU interface suitable for NanEyeC is the Serial Peripheral Interface (SPI). In contrast to typical SPI configurations, NanEyeM does not have a chip select (CS) line. The absence of a CS line means that NanEyeC cannot easily share an SPI bus with other SPI peripherals. This is only possible if there is an auxiliary mechanism to disconnect NanEyeC from the SPI bus by, e.g. shutting down NanEyeC using an MCU-controlled power supply.

In a basic SPI configuration, the bidirectional SDAT data pin of NanEyeC is connected to both the SPI “master out / slave in” (MOSI) pin and the “master in / slave out” (MISO) pin (see Figure 6). In this configuration, it is up to the MCU to ensure that no data is sent via the MCU’s MOSI pin while NanEyeC is transmitting data (and the MCU is receiving this data on the MISO pin). The actual implementation of this approach depends on the specific MCU used. Some MCU systems natively support a “3 wire”[1] (half duplex) SPI mode where the MOSI line supports bidirectional transmission. In such a configuration, the MISO line remains unused. Figure 7 shows this approach.

To reduce MCU load and make data transfers as efficient as possible, it is strongly advised to select an MCU which provides DMA engines serving the SPI peripheral. Moreover, some MCUs support 12-bit SPI transfers exactly matching the size of a NanEyeC pixel period. In contrast to 8-bit transfers, this slightly reduces MCU load for data re-alignment after capture.

Figure 6:
SPI Interconnection From MCU To NanEyeC With Separate, Selectively Activated MISO And MOSI Pins

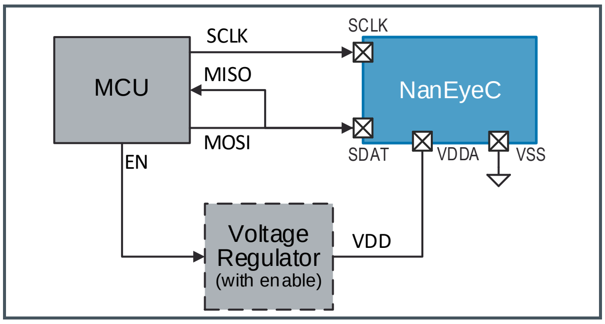
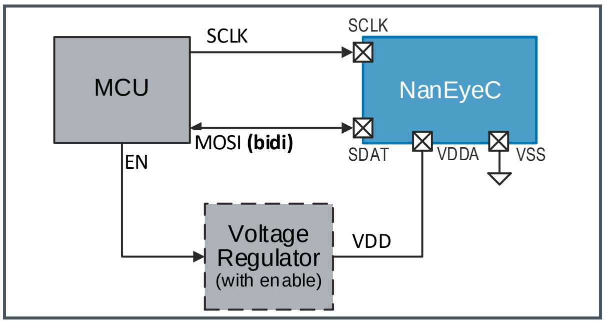


Figure 7:
“3 Wire” SPI Interconnection From MCU To NanEyeC



[1] The term “3 wire“ refers to CS, SCLK and MOSI lines. In case of NanEyeC, where no CS line is used, this effectively only 2 wires are used for communication.

3.2 Example MCU Firmware Architecture

For efficient image capturing it is important to consider a few architectural aspects when designing the firmware. Figure 8 shows an example firmware architecture. A key aspect for continuous, high-framerate image delivery is that the image capturing task uses DMA transfers for image acquisition and hence offloading the MCU. To enable continuous capture, a double (or multi) buffer structure is required for transferring captured image data from the capture to the processing task. In the image processing task the captured data is then post processed. Specifically, the following steps need to be performed:

- Remove the 8 training words from each captured image row
- Remove start and stop bits from each pixel
- Optionally reduce the 10-bit pixel data to 8-bit (depending on the application requirements)
- Apply pre-color gain
- Apply de-bayering
- Adjust image exposure

Figure 8:
Example Firmware Architecture

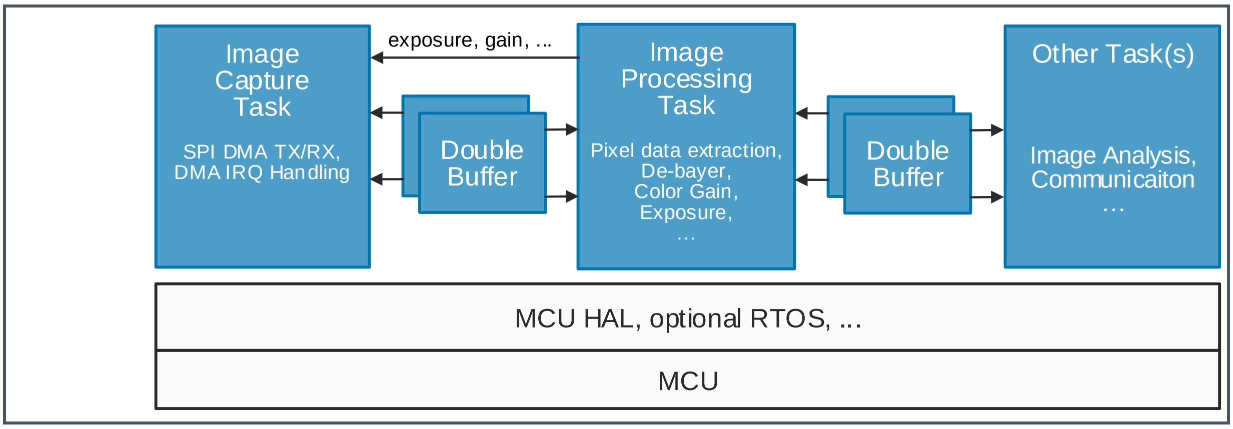


Image Capture Task
SPI DMA TX/RX, DMA IRQ Handling
exposure, gain, ...
Double Buffer
Image Processing Task
Pixel data extraction, De-bayer, Color Gain, Exposure, ...
Double Buffer
Other Task(s)
Image Analysis, Communicaiton
...
MCU HAL, optional RTOS, ...
MCU

3.3 Frame Capture Using 12-Bit SPI Interface

If the MCU supports 12-bit SPI transfers, this mode is recommended for image capturing. 12-bit words from NanEyeC are then stored in 16-bit words in MCU memory. The capture sequence is then as follows:

```
// !! IMPORTANT !!
// In this example, an SPI word (i.e., a word sent/read on the
// bus by the spi_ functions) has a length 12 bits.

// after power-on reset NanEyeC is in IDLE MODE
spi_GenClocks(1);  // generate a single clock for activation
spi_WriteWords(reg0_val, 2); // first  2 PP of INITIAL INTERFACE MODE
spi_WriteWords(reg1_val, 2); // second 2 PP of INITIAL INTERFACE MODE
wait (10us); // wait for IDLE start-up (longer times are also possible)
spi_GenClocks(10); // generate 10 alignment clocks (before first frame only)
spi_ReadWords_DMA(329); // INITIAL PRE-SYNC MODE (read and ignore)
spi_ReadWords_DMA(656); // SYNC MODE (read and ignore)
spi_ReadWords_DMA(2*328);   // DELAY MODE (can be extended to 498x328PP)
spi_ReadWords_DMA(320*328); // READOUT mode first image (read and ignore)
spi_ReadWords_DMA(8);       // end of frame (read and ignore)

// main capture loop
while(True) {
    spi_WriteWords(reg0_val, 2); // first  2 PP of INTERFACE MODE
    spi_WriteWords(reg1_val, 2); // second 2 PP of INTERFACE MODE
    spi_WriteWords(0x0, 644);    // rest of INTERFACE MODE (648 – 4PP)
    spi_ReadWords_DMA(4*328);    // SNYC and DELAY MODEs (read and ignore)
    img = spi_ReadWords_DMA(320*328); // READOUT MODE
    spi_ReadWords_DMA(8);        // end of frame (read and ignore)
    send_ImgToProcessingTask(img);
}
```

Start and stop bits for a pixel need to be masked/shifted out in a separate post-processing step.

DMA Transfer Size

The DMA controllers of many MCUs have the limitation that the DMA counter is only 16 bits. Therefore, the NanEyeC pixel data cannot be read in a single DMA transfer but has to be split up into several transfers. Starting the next DMA transfer takes a small amount of time resulting in a small gap in the SPI clock. This clock gap results in an effect where the pixels of the next DMA transfer might be overexposed. Therefore, it is recommended to align DMA transfer boundaries with the end of an image row and, if needed, reconstruct the values of overexposed pixels based on the values of neighbor pixels using averaging.

High-Speed Clocks

For high SPI clock frequencies above 40 MHz the NanEyeM data signal might not be stable enough at the rising edge of the clock. In these situations, it is recommended to sample at the signal at the falling edge of the clock (i.e., SPI CPHA to the second clock edge).

3.4 Frame Capture Using 8-Bit SPI Interface

If only 8-bit SPI transfers are supported by the MCU, 2PPs are transferred into memory as a unit of 3 bytes, which need to be separated into two distinct pixel values in a separate post-processing step. The capture sequence is then as follows:

```
1    // !! IMPORTANT !!
2    // In this example, an SPI word (i.e., a word sent/read on the
3    // bus by the spi_ functions) has a length 8 bits.
4
5    // after power-on reset NanEyeC is in IDLE MODE
6    spi_GenClocks(1);  // generate a single clock for activation
7    spi_WriteWords(reg0_val, 3); // first  2 PP of INITIAL INTERFACE MODE
8    spi_WriteWords(reg1_val, 3); // second 2 PP of INITIAL INTERFACE MODE
9    wait (10us); // wait for IDLE start-up (longer times are also possible)
10   spi_GenClocks(10); // generate 10 alignment clocks (before first frame only)
11   spi_GenClocks(12); // first PP of INITIAL PRE-SYNC MODE (read and ignore)
12   spi_ReadWords_DMA(492); // INITIAL PRE-SYNC MODE (read and ignore)
13   spi_ReadWords_DMA(984); // SYNC MODE (read and ignore)
14   spi_ReadWords_DMA(984); // DELAY MODE (can be extended to 498x328PP)
15   spi_ReadWords_DMA(320*492); // READOUT mode first image (read and ignore)
16   spi_ReadWords_DMA(12);      // end of frame (read and ignore)
17
18   // main capture loop
19   while(True) {
20       spi_WriteWords(reg0_val, 3); // first  2 PP of INTERFACE MODE
21       spi_WriteWords(reg1_val, 3); // second 2 PP of INTERFACE MODE
22       spi_WriteWords(0x0, 966);    // rest of INTERFACE MODE (648 – 4PP)
23       spi_ReadWords_DMA(4*492);    // SNYC and DELAY MODEs (read and ignore)
24       img = spi_ReadWords_DMA(320*492); // READOUT MODE
25       spi_ReadWords_DMA(12);       // end of frame (read and ignore)
26       send_ImgToProcessingTask(img);
27   }
```

Start and stop bits for a pixel need to be masked/shifted out in a separate post-processing step.

Compared to the 12-bit variant, with 8-bit SPI word size all transfer counts are multiplied by 1.5. Since the INITIAL PRE-SYNC MODE consists of an uneven number of PPs, this would require the transfer of a half-word (4-bit) in the SPI bus. To overcome this issue it is recommended to clock in the first PP of the INITIAL PRE-SYNC MODE using bit banging (line 10 in the listing above).

Data read from the sensor is stored in memory such that two pixels are stored in three consecutive bytes. In a post-processing step the start and stop bits of the pixels have to be removed and the pixels have to be separated. A corresponding code snippet is show below:

```
U8 *data; // array with captured pixel data
U16 first_pixel  = ((data[0] << 3) & 0x3F8) | (data[1] >> 5)
U16 second_pixel = ((data[1] << 7) & 0x380) | (data[2] >> 1)
```

3.5 Image Post-Processing and Control

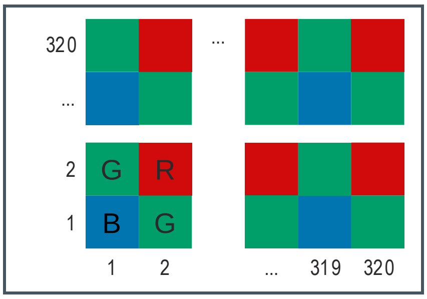
3.5.1 Pre-Color Gain

Pre-color gain changes pixel values after capture (and before color reconstruction). Adjustment values for red, green and blue pixels can be defined separately. The raw pixel values are the multiplied with these adjustment values resulting in either an attenuation or an amplification of the color component.

3.5.2 De-Bayering

For de-bayering, bilinear color reconstruction can be applied. This generates a color image from the raw image captured from the sensor Figure 9 shows the color filter pattern used for the sensor where each individual pixel is either red, green or blue. The other two color components have to be reconstructed form neighboring pixels.

Figure 9:
Color Filter Pattern



For red pixels, their green pixel value is the mean of the four surrounding green pixels (horizontal and vertical). The blue pixel value is the mean of the surrounding blue pixels (diagonal). This approach is shown in Figure 10 and Figure 11. For this example, the RGB value of the pixel is (50, 24, 35).

Figure 10:
Blue Value Reconstruction For Red Pixel

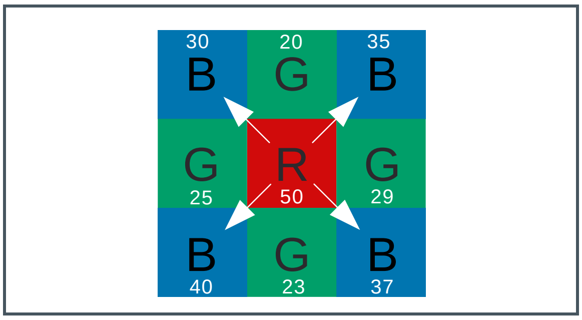
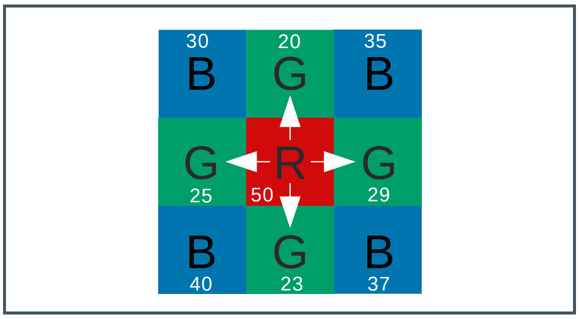
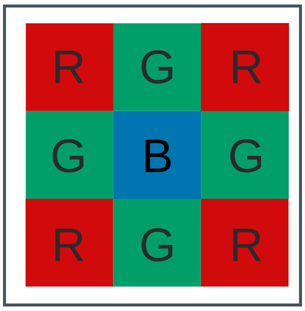


Figure 11:
Green Value Reconstruction For Red Pixel



For blue pixels the computation of red and green is done in an analog way (mean of green and red neighbors as show in Figure 12

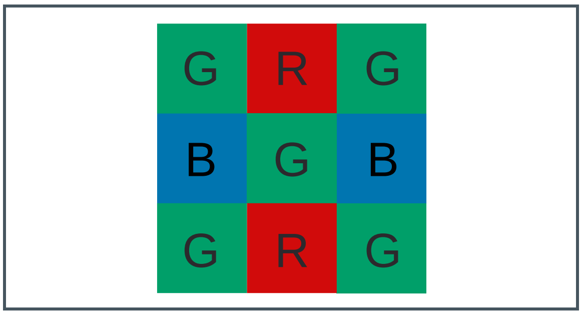
Figure 12:
Blue Pixel Neighborhood



R	G	R
G	B	G
R	G	R

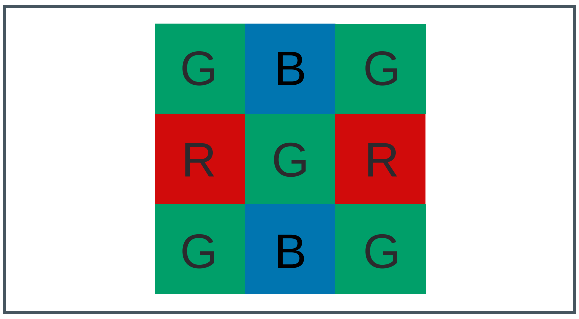
Finally, in case of green pixels the missing blue and red components are not computed from four but only two neighboring pixels, namely the two horizontal/vertical red/blue pixels as shown in Figure 13 and Figure 14.

Figure 13:
Green Pixel Neighborhood – Case 1



G	R	G
B	G	B
G	R	G

Figure 14:
Green Pixel Neighborhood – Case 2



G	B	G
R	G	R
G	B	G

3.5.3 Exposure Control

Image exposure is controlled be the following settings:

- Rows in reset
- Rows delay
- Gain (Ramp and CDS)

A simple approach to adjust image exposure is to compute the histogram of the image, determine the mean and assess its location within the histogram. If it is left of the histogram's center, the exposure of the image needs to be increased by:

  - Decreasing the rows in reset and/or
  - Increasing the rows delay and/or

- Increasing the gain settings.

Vice versa if the mean is right of the histogram’s center, the exposure needs to be decreases by:

- Increasing the rows in reset and/or
- Decreasing the rows delay and/or
- Decreasing the gain settings.

New rows in reset, rows delay and gain settings can be performed via NanEyeC registers which can be written by the host during INTERFACE MODE. Be aware that changing the rows delay setting also means that the amount of training pattern read from the sensor before the actual pixel data increases.

4 Revision Information

Changes from previous version to current revision v2-00	Page
Changed Security Class from CONFIDENTIAL to PUBLIC	
De-Bayering Section Figures Updated	11-12

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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Headquarters

ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

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