AS7058

Datasheet

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AS7058 IC for PPG, ECG and body impedance measurement

1 General description

The AS7058 is an integrated multi-vital sign monitoring device, which provides a complete photoplethysmogram (PPG), electrocardiogram (ECG), body impedance (BioZ), and electrodermal activity (EDA). PPG measures the pulse rate or blood oxygen by sampling light modulated by the blood vessels, which expand and contract as blood pulses through them. ECG is the reference for any measurement of the biopotential generated by the heart. With EDA, it is possible to measure the skin's water content, and with BioZ, the body composition with an electrical system.

The PPG acquisition system provides up to eight LEDs and eight photodiode inputs. The LEDs are powered by two high current 8-bit programmable LED drivers with four current ranges. Additionally, a special laser safety support system can be enabled, which offers the possibility to use VCSEL die as a light source. The photodiodes can be read out synchronously with two 20-bit ADCs. As the second product in the AS705x family, the AS7058 includes a new method of ambient light suppression method called advanced automatic offset control (AAOC). This method enables the system to adjust towards the ambient light situation before the actual measurement starts and minimizes the loss of data due to the saturation influence by ambient light.

The ECG channel has high-input impedance, low noise, high CMRR, programmable gain, an anti-aliasing low-pass filter, and a high-resolution 20-bit ADC. It is designed according to IEC 60601-2-47 Ambulatory ECG Systems monitoring compliance requirements.

The BioZ channel has a low-pass filter and a calibration routine available. The channel also has high input impedance, low noise, programmable gain, low-pass and high-pass filter options, and shares the high-resolution ADC with the ECG system. Several ranges of excitation current and frequencies are also available.

The AS7058 has a DC and AC lead-off detection for the ECG, a flexible clock system, and a PLL. All three inbuilt ADCs are synchronized. The device is available in a 42-ball wafer-level chip scale package (WLCSP) with dimensions 2.82 mm x 2.55 mm and operates over the temperature range -40 °C to 85 °C.

1.1 Key benefits & features

The benefits and features of AS7058 are listed below:

Table 1: Added value of using AS7058

Benefits	Features
Highly flexible LED/photodiode configuration.	Up to 8 LED output pins and 8 photodiode input pins.
Allows the smallest application size e.g. narrow HRM measurement band.	Small Wafer-Level-Chip-Scale-Package (WLCSP).
Electrocardiogram (ECG) with dry electrodes.	Embedded low-noise analog front-end for ECG signal acquisition.
Enables blood pressure measurements.	Synchronized PPG and ECG acquisition.
Outstanding HRM measurement quality.	Low noise analog front end for PPG acquisition.
Measuring the body composition and the skin’s water content.	An independent body impedance and an electrodermal activity system are included.
Long operating time.	A hardware sequencer to offload the processor with an adjustable LED driver with current control.
Low power operating mode.	Two PPG channels usable in parallel mode are available.
Acquiring several bio signals in parallel.	Either ECG, BIOZ or EDA (GSR) and two PPG channels, separated and usable simultaneously.
Improvement in ambient light suppression.	Includes a new type of offset cancelation for the PPG signal: Advanced Automatic Offset Control.

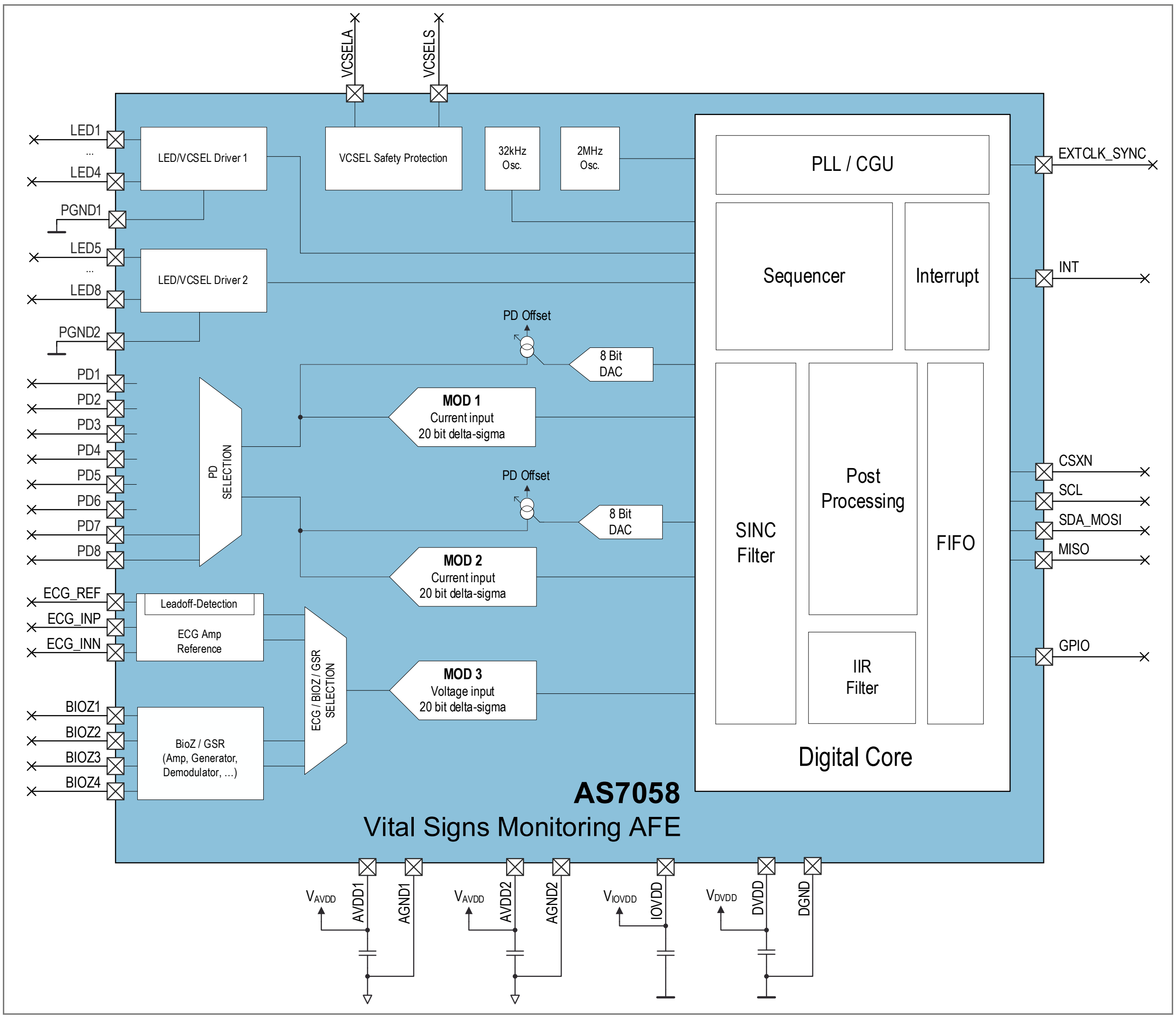
1.2 Applications

- Wearable vital sign monitors
- Fitness band
- Smart watch
- Heart rate monitor
- Hearables
- ECG monitoring
- Medical patches
- Pulse-oximetry devices
- Single- and multi-frequency body impedance devices
- Pulse Arrival Time (PAT), Pulse Transit Time (PTT), Pulse Wave Velocity (PWV) Assessments

1.3 Block diagram

The functional blocks of this device are shown below:

Figure 1: Functional blocks of AS7058



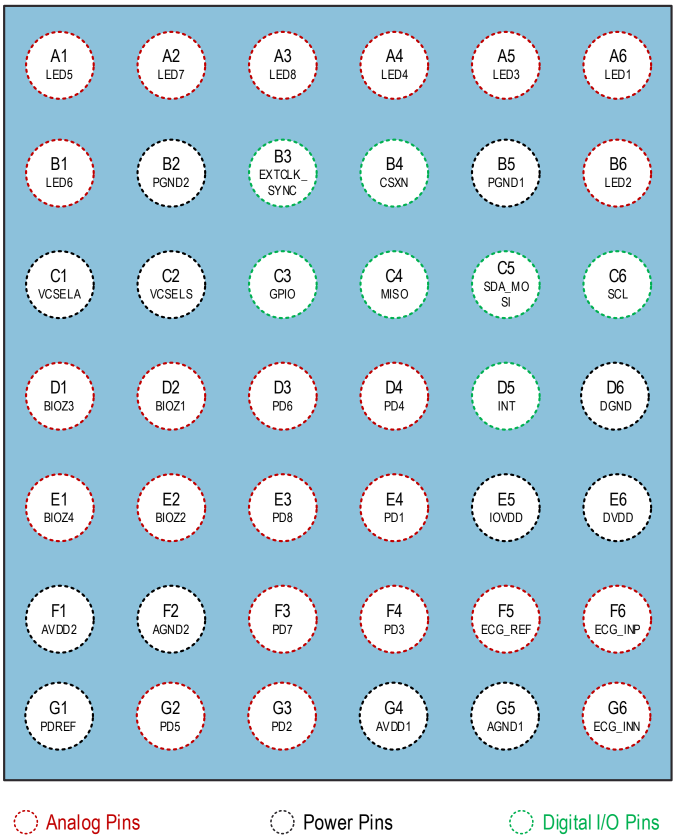
2 Ordering information

Ordering code	Package	Marking	Delivery form	Delivery quantity
Q65113A6621	WLCSP	AS7058	Tape & reel	500 pcs/reel
Q65113A6622	WLCSP	AS7058	Tape & reel	10000 pcs/tray
Q65113A6625	WLCSP	AS7058A	Tape & reel	500 pcs/reel
Q65113A6626	WLCSP	AS7058A	Tape & reel	10000 pcs/tray

3 Pin assignment

3.1 Pin diagram

Figure 2: Pin diagram of AS7058 / AS7058A (Top View)



3.2 Pin description

Table 2: Pin description of AS7058

Pin number	Pin name	Pin type[1]	Description
A1	LED5	AI	LED input number 5 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
A2	LED7	AI	LED input number 7 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
A3	LED8	AI	LED input number 8 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
A4	LED4	AI	LED input number 4 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
A5	LED3	AI	LED input number 3 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
A6	LED1	AI	LED input number 1 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
B1	LED6	AI	LED input number 6 which is connected internally to LED driver 2. In case input is not used in application pin can be left unconnected.
B2	PGND2	G	LED driver 2 power ground pin for LED inputs LED5, LED6, LED7 and LED8.
B3	EXTCLK_SYNC	DI	External Clock and synchronization input. This digital input can be used to feed in an external 2 MHz clock. Furthermore, pin can also be used for external host synchronization to trigger a measurement start based on signal level of the EXTCLK_SYNC pin.
B4	CSXN	DI	SPI Chip Select input pin. **In case I²C interface is used as device host communication interface, this pin requires an external pull up resistor.**
B5	PGND1	G	LED driver 1 power ground pin for LED inputs LED1, LED2, LED3 and LED4.
B6	LED2	AO	LED input number 2 which is connected internally to LED driver 1. In case input is not used in application pin can be left unconnected.
C1	VCSELA	AO	VCSEL Diode Anodes
C2	VCSELS	P	This is the power supply input pin for the LED driver and VCSEL circuit. **Pin must always be connected to LED supply voltage and must not be left unconnected.**
C3	GPIO	DO/DI	Digital General Purpose I/O which allows to assign various functions.
C4	MISO	DO	SPI Data Output pin
C5	SDA_MOSI	DO/DI	Data for I²C Interface/SPI data in
C6	SCL	DI	Clock input for I²C/SPI interface
D1	BIOZ3	AI/AO	Input/Output 3 for BIOZ
D2	BIOZ1	AI/AO	Input/Output 1 for BIOZ

Pin number	Pin name	Pin type(1)	Description
D3	PD6	AI	Photodiode input number 6
D4	PD4	AI	Photodiode input number 4
D5	INT	DO	Digital interrupt push/pull output pin. The polarity of the interrupt pin acting as active high or active low can be programmed via control register.
D6	DGND	G	Digital Ground
E1	BIOZ4	AI/AO	Input/Output 4 for BIOZ
E2	BIOZ2	AI/AO	Input/Output 2 for BIOZ
E3	PD8	AI	Photodiode input number 8
E4	PD1	AI	Photodiode input number 1
E5	IOVDD	P	This is the digital I/O supply pin. This supply is separated from the digital core supply of AS7058 and can for example be connected to a 1.2 V supply voltage to enable lower I²C or SPI interface voltages to eliminate the need of external level shifters.
E6	DVDD	P	Positive digital supply terminal of AS7058 which needs to be connected to a 1.8 V power supply.
F1	AVDD2	P	Positive analog supply terminal 2 which supplies all analog blocks of the device. Needs to be connected to a low noise 1.8V power supply.
F2	AGND2	G	Analog Ground
F3	PD7	AI	Photodiode input number 7
F4	PD3	AI	Photodiode input number 3
F5	ECG_REF	AO	ECG amplifier reference electrode terminal
F6	ECG_INP	AI	ECG amplifier positive input terminal
G1	PDREF	AO	Reference Potential for Photodiodes
G2	PD5	AI	Photodiode input number 5
G3	PD2	AI	Photodiode input number 2
G4	AVDD1	P	Positive analog supply terminal 1 which supplies all analog blocks of the device. Needs to be connected to a low noise 1.8V power supply.
G5	AGND1	P	Analog ground
G6	ECG_INN	AI	ECG amplifier negative input terminal

(1) Explanation of abbreviations:

DI	Digital Input
DO	Digital Output
AI	Analog Input
AO	Analog Output
P	Power Supply
G	Ground

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS7058

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V_{DVDD}	Digital supply voltage	-0.3	1.98	V	DVDD to DGND
V_{AVDD}	Analog supply voltage	-0.3	1.98	V	AVDD to AGND
V_{IOVDD}	IO supply voltage	-0.3	1.98	V	IOVDD to AGND
V_{VCSELS}	VCSELS supply voltage	-0.3	5.5	V	VCSELS to AGND
V_{VCSELA}	VCSELA pin voltage	-0.3	5.5	V	VCSELA to AGND
$V_{VCSELA-VCSELS}$	Voltage difference between pins VCSELA and VCSELS	-0.3	0.3	V	
V_{LED}	LED pin voltage	-0.3	5.5	V	LED1-LED8 to PGND1 or PGND2
$V_{IN-DIGITAL}$	Digital input pin voltage to ground	-0.3	V_{IOVDD}+0.3 V max. 1.98 V	V	Applicable to pins SCL, SDA_MOSI, CSXN, GPIO and EXTCLK_SYNC
$V_{IN-ANALOG}$	Analog input pin voltage to ground	-0.3	V_{AVDD}+0.3 V max. 1.98 V	V	Applicable to pins ECG_INP, ECG_INN, PD1/PD2, PD3, PD4, PD5, PD6, PD7, PD8, BIOZ1, BIOZ2, BIOZ3 and BIOZ4
$V_{PGND-AGND}$	Power to analog ground voltage difference	-0.3	0.3	V	
$V_{DGND-AGND}$	Digital to analog ground voltage difference	-0.3	0.3	V	
I_{LEDON}	Average LED ON Current		35	mA	
I_{SCR}	Input current (latch-up immunity)	± 100		mA	JEDEC JESD78E
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM	± 2		kV	JS-001-2017
ESD_{CDM}	Electrostatic discharge CDM	± 500		V	JS-002-2018
Temperature ranges and storage conditions					
T_A	Operating ambient temperature	-40	85	°C	
T_{STRG}	Storage temperature range	-40	125	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	

Symbol	Parameter	Min	Max	Unit	Comments
MSL	Moisture sensitivity level	1			According to JEDEC J-STD-020E Represents a max. floor life time of unlimited
$t_{STRG\ DOF}$	Storage time for DOF/die or wafers on foil		3	months	Refers to indicated date of packing

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.” The lead finish for Pb-free leaded packages is “Matte Tin” (100 % Sn).

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Conditions: T_A = 25 °C, V_{DVDD} = 1.8 V, V_{AVDD} = 1.8 V, V_{IOVDD} = 1.8 V

Table 4: Electrical characteristics of AS7058

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Digital supply voltage		1.70	1.80	1.98	V
V_{AVDD}	Analog supply voltage		1.70	1.80	1.98	V
V_{IOVDD}	IO supply voltage		1.08	1.80	1.98	V
V_{VCSELS}	VCSELS supply voltage	Voltage must not be below V_{AVDD}	1.75		5.50	V
Photodiode inputs						
C_{PD}	Total photodiode capacitance connected to MOD1 or MOD2	0 V reverse voltage			300	pF
I_{PD}	Photocurrent input				64	µA
MOD1 & MOD2 (PPG channels)						
MOD_{DAC_OFF}	DAC offset current full-scale range for MOD1 or MOD2 (X = 1 or 2)	**PPGMODX_IOS_FS** = 0		1		µA
		PPGMODX_IOS_FS = 1		2		
		PPGMODX_IOS_FS = 2		4		
		PPGMODX_IOS_FS = 3		8		
		PPGMODX_IOS_FS = 4		16		
		PPGMODX_IOS_FS = 5		32		
		PPGMODX_IOS_FS = 6		64		
		PPGMODX_IOS_FS = 7		128		
MOD_{RES}	ADC resolutions of MOD1 and MOD2			20		bit

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LED driver						
LED_{RES}	LED driver resolution			8		bit
I_{RANGE1}	Allowed operating input current for LED pin 1 to 4 (X = 1 to 4)	**LEDX_IRNG** = 0		25		mA
		LEDX_IRNG = 1		150		
		LEDX_IRNG = 2		225		
		LEDX_IRNG = 3		300		
I_{RANGE2}	Allowed operating input current for LED pin 5 to 8 (X = 5 to 8)	**LEDX_IRNG** = 0		25		mA
		LEDX_IRNG = 1		150		
		LEDX_IRNG = 2		225		
		LEDX_IRNG = 3		300		
V_{Compl1}	Compliance voltage for LED pin 1 to 4 (X = 1 to 4)	**LEDX_IRNG** = 0		0.3		V
		LEDX_IRNG = 1		0.4		V
		LEDX_IRNG = 2		0.55		V
		LEDX_IRNG = 3		0.75		V
V_{Compl2}	Compliance voltage for LED pin 5 to 8 (X = 5 to 8)	**LEDX_IRNG** = 0		0.3		V
		LEDX_IRNG = 1		0.4		V
		LEDX_IRNG = 2		0.55		V
		LEDX_IRNG = 3		0.75		V
ECG/BioZ channel						
$MOD3_{RES}$	ADC resolution of ECG and BioZ Modulator 3			20		bit
ECG amplifier						
V_{IN_SIG}	Input signal ECG		-10		10	mV
$V_{IN\_DC\_OFF}$	Input DC offset		-300		300	mV
$V_{Noise,\ p\text{-}v}$	Input peak to valley noise				50	µV
R_{IN}	Input impedance		1			GΩ
V_{ECG_REF}	ECG_REF voltage			0.8		V
CMRR	Common-mode rejection ratio	According to IEC60601-2-47		117		dB
ECG_{NOISE}	Input-referred noise	According to IEC60601-2-47			2	μV_{RMS}
ECG_{LEAK}	Input leakage current	At ECG_INN and ECG_INP		70		pA
ECG_{GAIN_ACC}	Gain accuracy	According to IEC60601-2-47		2.5		%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ECG_{GAIN}	Amplifier gain range		1		1024	
BioZ(1)						
$BIOZ_{P\_ERR}$	Phase-measurement error, at 50 kHz	Body impedance = 510 Ω		0.45		deg
		Body impedance = 1000 Ω		0.85		deg
$BIOZ_{M\_ERR}$	Magnitude-measurement error, at 50 kHz	Body impedance = 510 Ω		1.23		%
		Body impedance = 1000 Ω		0.96		%
$BIOZ_{EXC\_ERR}$	Excitation frequency error	Internal clock at 50 kHz		1		%
$BIOZ_{EXC\_FREQ}$	Excitation frequency		1		1000	kHz
$BIOZ_{EXC\_CURR}$	Excitation current		10		100	µA
GSR/EDA						
GSR_{EXC_CURR}	Excitation current		0.2		85	µA
GSR_{DR}	Dynamic range		0.1		3.3	MΩ
			0.3		100	µS
Lead-off detection (ECG)						
ECG_{LO_CURR}	Lead-off current	Set by **ECGAMP_LEADOFF_CURR**	1.5		400	nA
ECG_{LO_ACC}	Lead-off current accuracy	**ECGAMP_LEADOFF_CURR** = 400 nA	-5		5	%
ECG_{LO_FREQ}	Lead-off toggle frequency		0.25		2	kHz
Digital inputs (SDA_MOSI, SCL, EXTCLK_SYNC, CSXN, GPIO)						
V_{IH}	Input high		V_{IOVDD} × 0.7			V
V_{IL}	Input low				V_{IOVDD} × 0.3	V
f_{EXTCLK_SYNC}	External clock frequency	Input frequency at pin EXTCLK_SYNC; Only 2 MHz or 4 MHz is supported	2		4	MHz
Digital outputs (SDA_MOSI, MISO, INT, GPIO)						
V_{OH}	Output high towards GND	Current load ≤ 6 mA	V_{IOVDD} - 0.4			V
V_{OL}	Output low towards IOVDD	Current load ≤ 6 mA			0.4	V

(1) BioZ measurements are done with the ams OSRAM in-house calibration and measurement flow.

5.1 Power consumption

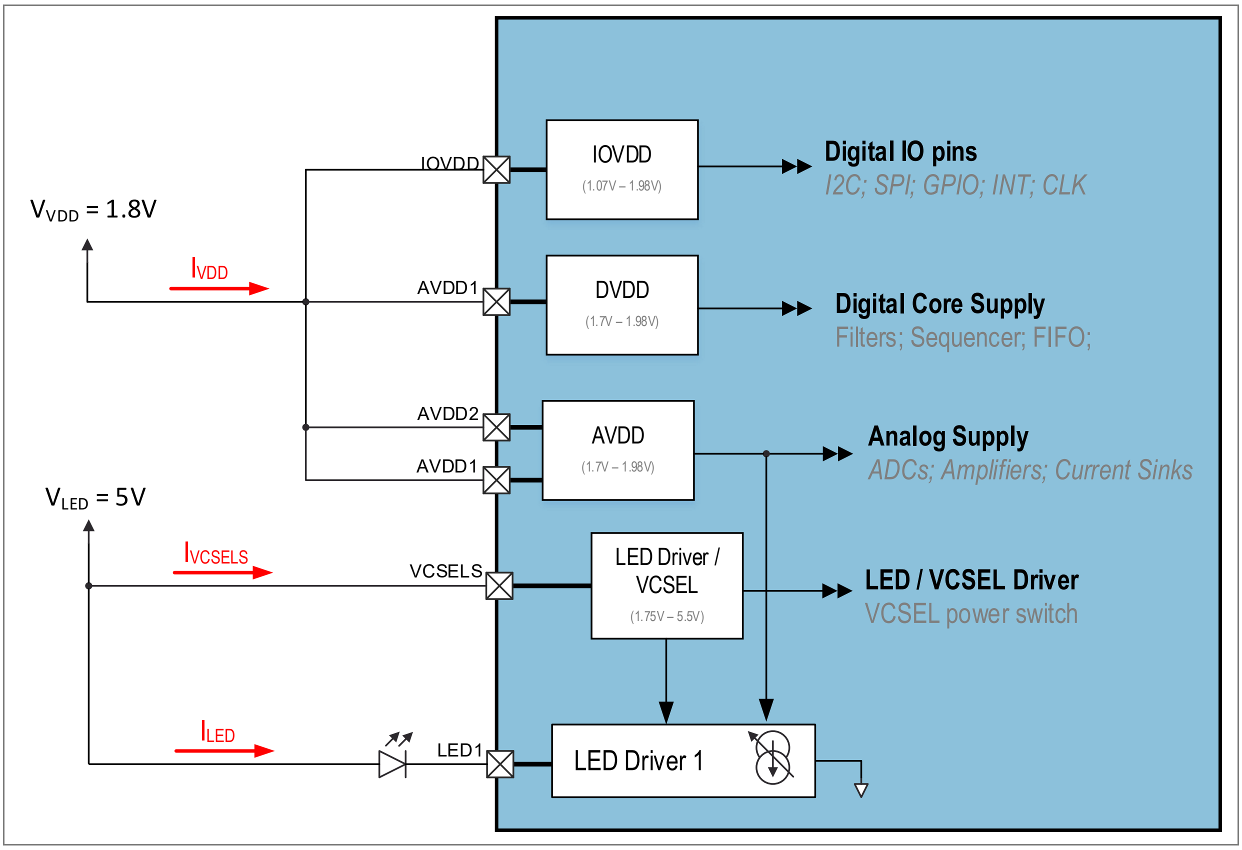
This chapter contains typical power consumption values for PPG and ECG measurements. The measurement setup is shown in Figure 3.

Conditions: T_A = 25 °C, V_{DVDD} = 1.8 V, V_{AVDD} = 1.8 V, V_{IOVDD} = 1.8 V; V_{VCSELS} = 5 V

Table 5: Typical power consumption

Symbol	Operation mode	Measurement conditions	Typ. I_{VDD}	Typ. I_{VCSELS}	Typ. I_{LED}	Unit
I_{DVDD}	Supply current in power down mode			1.80		µA
I_{AVDD}	Supply current in power down mode			0.15		µA
I_{IOVDD}	Supply current in power down mode			0.02		µA
I_{VCSELS}	Supply current in power down mode			0.01		µA
I_{PPG_25Hz}	PPG current consumption 25 Hz Sample Rate	Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=25 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=58 µs;	17	0.01	15	µA
		Standby Mode enabled; 1 LED driver active @ 150 mA current range; 10 mA LED active current; 1 ADC active; Single Normal Measurement; no postprocessing enabled; f_s=25 Hz; f_{MOD_CLK}=10 MHz; $t_{INTEGRATION}$=117 µs;	28	0.01	29	µA
I_{ECG_400Hz}	ECG measurement 400 Hz sample rate	Standby Mode enabled; High pass enabled; LP bypassed; Chopper INA1 enabled with 8 kHz; INA1 Gain=4; INA2 Gain = 64; IMUX Gain1, IIR filter enabled for on chip notch filtering; $t_{INTEGRATION}$=150 µs; f_s=400 Hz;	0.66	0.01	-	mA
I_{ECG_1kHz}	ECG measurement 1 kHz sample rate	High pass enabled; LP bypassed; Chopper INA1 enabled with 8 kHz; INA1 Gain=4; INA2 Gain=64; IMUX Gain1, IIR filter enabled for on chip notch filtering; $t_{INTEGRATION}$=150 µs; f_s= 1 kHz;	1.62	0.01	-	mA

Figure 3: Block diagram of power consumption measurement setup



6 Typical operating characteristics

Figure 4: SNR vs. PD current ADC range = 64 µA; f_S = 200 Hz

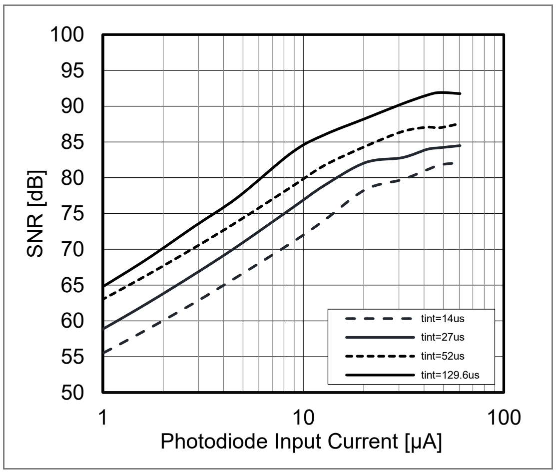


Figure 5: SNR vs. PD current; ADC range = 32 µA; f_S = 200 Hz

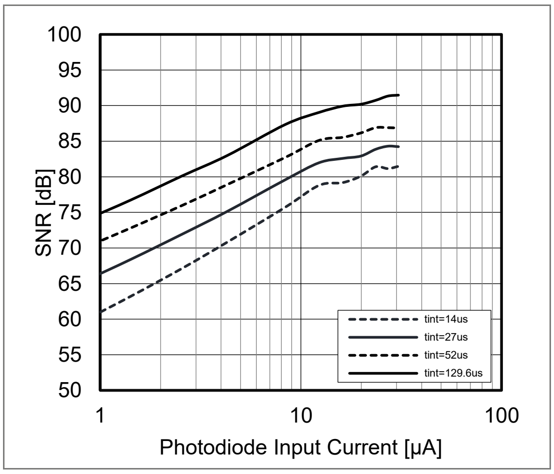


Figure 6: SNR vs. PD current 64 µA multi measurement = 16x, ADC range = 64 µA, t_{INT}=129.1 µs; f_S = 200 Hz

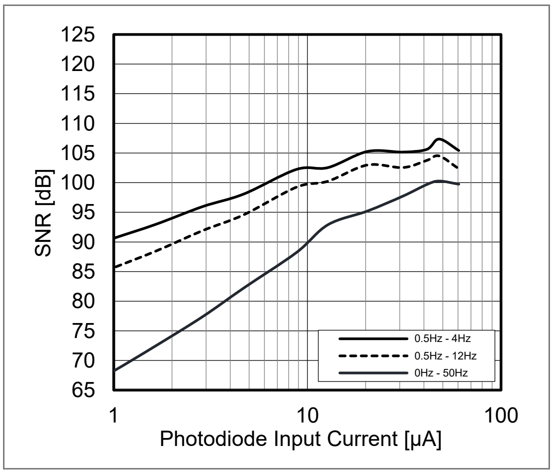


Figure 7: SNR vs. PD current 32 µA multi measurement = 16x, ADC range = 32 µA, t_{INT}=129.1 µs; f_S = 200 Hz

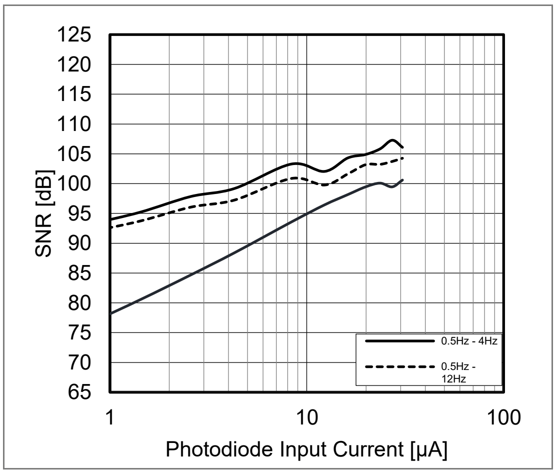


Figure 8: SNR vs. PD current ADC range=64 μA, t_{INT}=129.1 μs

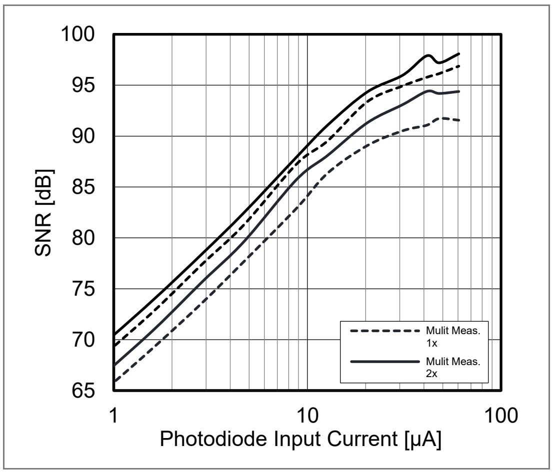


Figure 9: SNR vs. PD current ADC range=32 μA, t_{INT}=129.1 μs

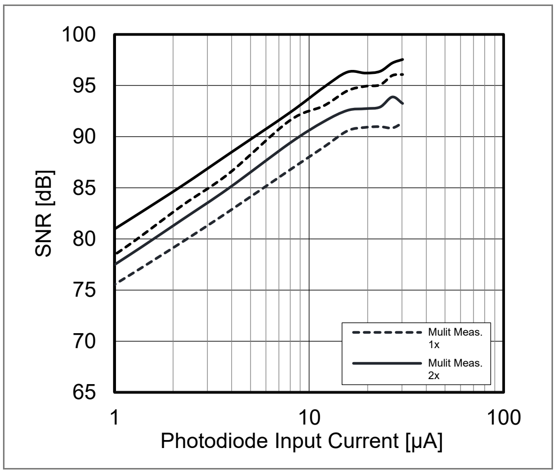


Figure 10: ECG CMRR vs. frequency gain=32x, sample rate = 2000sps RLD: low GM

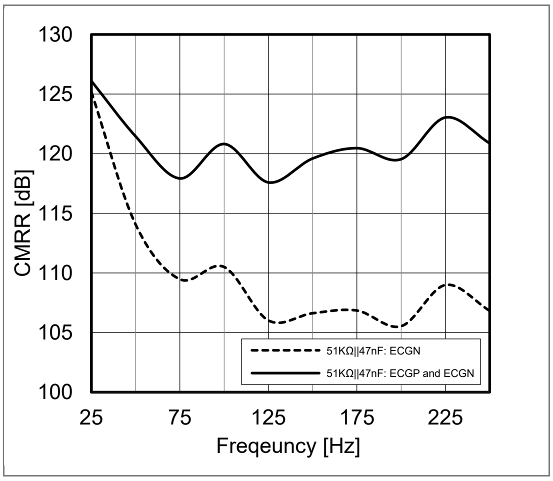


Figure 11: ECG CMRR vs. frequency gain=32x, sample rate = 2000sps RLD: high GM

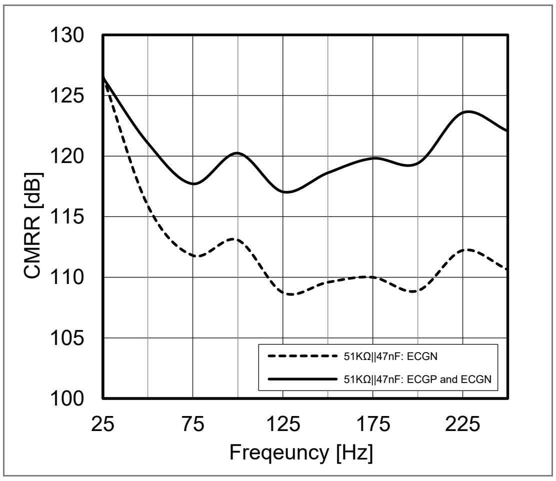


Figure 12: ECG CMRR vs. frequency gain=128x, sample rate=2000sps RLD: low GM

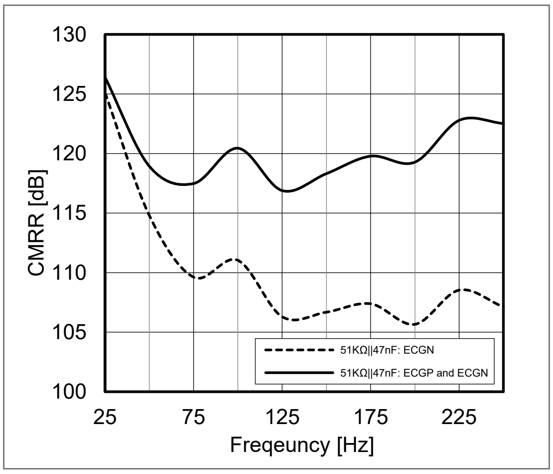


Figure 13: ECG CMRR vs. frequency gain=128x, sample rate = 2000sps RLD: high GM

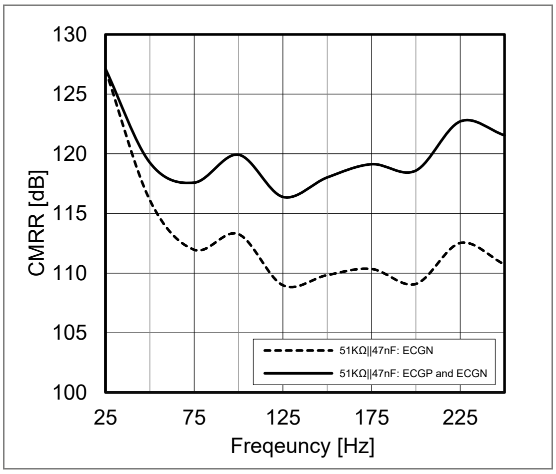


Figure 14: ECG noise vs. time inputs shorted: gain = 128, HPF enabled

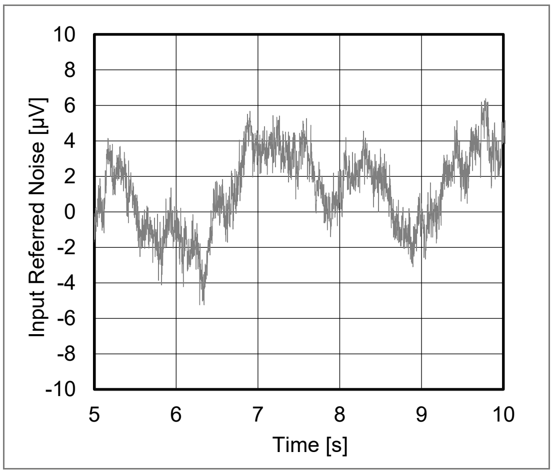


Figure 15: ECG noise spectrum vs. frequency inputs shorted, gain = 32, HPF disabled

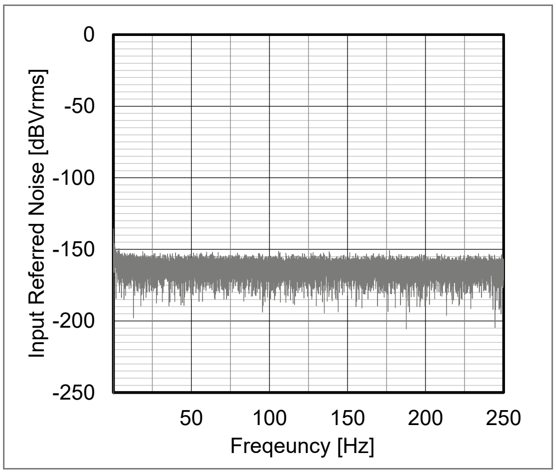


Figure 16: ECG noise spectrum vs. frequency inputs shorted: gain = 32, HPF enabled

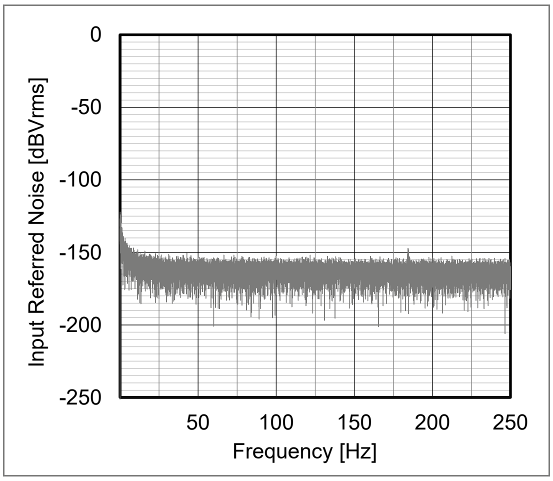


Figure 17: ECG noise spectrum vs. frequency inputs shorted: gain = 128, HPF disabled

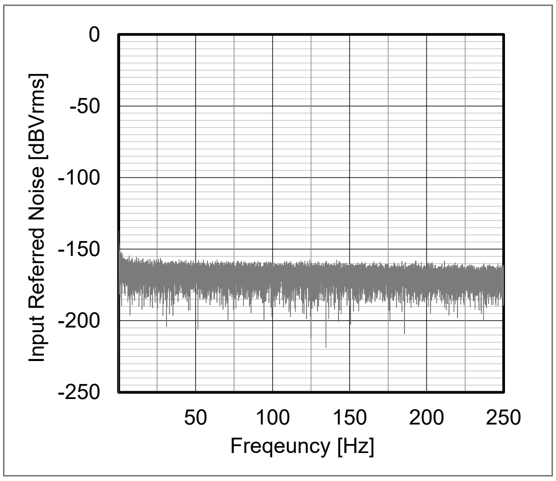


Figure 18: ECG noise spectrum vs. frequency inputs shorted: gain = 128, HPF enabled

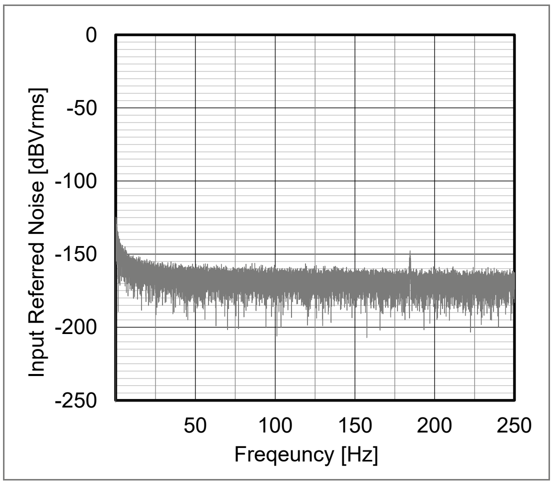


Figure 19: ECG noise vs. time inputs shorted: gain = 32, HPF disabled

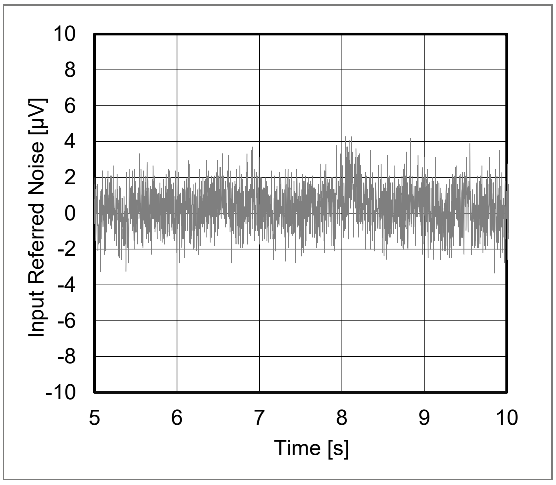


Figure 20: ECG noise vs. time inputs shorted: gain = 32, HPF enabled

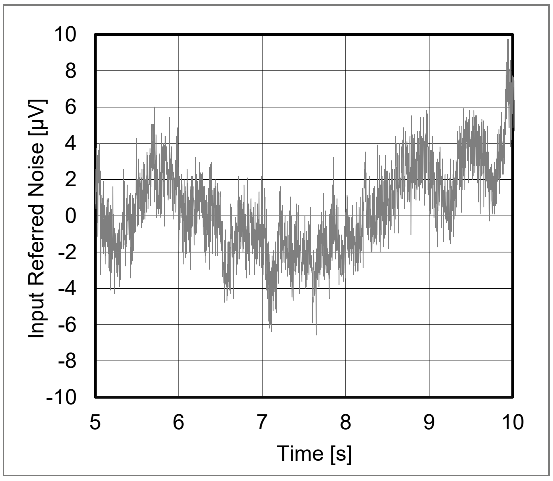
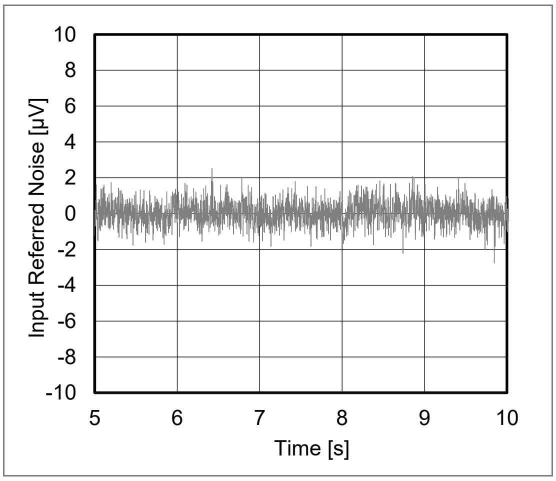


Figure 21: ECG noise vs. time inputs shorted: gain = 128, HPF disabled



7 Functional description

The AS7058 is an integrated data acquisition system ideal for several applications, including optical heart rate measurement and pulse oximetry, ECG, respiration rate calculation, body impedance analysis (BIA), and numerous other applications. It is designed to fulfill the requirements of the consumer healthcare market and the medical industry.

The PPG data acquisition system supports up to eight LEDs and eight photodiode inputs and includes two high-resolution optical readout channels with a new ambient light cancelation feature and two high-current LED drivers to complete the system.

The ECG channel has high input impedance, low noise, high CMRR, programmable gain, right-leg drive, lead-off detection, and a high-resolution channel.

The BioZ channel has an independent circuit to inject current into the body and to measure voltage in return. The system contains four pins, which can be freely combined for two-electrode current injection and two-electrode voltage measurement. The injected current is programmable and available over a wide frequency range (1 kHz to 1 MHz) and a wide range of current magnitudes (200 nA up to 100 µA). These ranges support GSR (galvanic skin response), electrodermal activity (EDA) measurements, and BIA applications.

The BioZ Channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, a high-resolution ADC, and I and Q measurement capability to provide magnitude and phase measurements for BIA applications. A calibration routine to lower the external components needed is also available.

The AS7058 is fully programmable by the registers, and the digital output data is stored in a 512-word FIFO. The FIFO allows the device to be connected to a microcontroller or processor on a shared I²C or SPI bus. They both operate in fully autonomous mode for low-power battery applications.

The device works on a 1.8 V main supply voltage and up to 5.5 V at the LED pins. They both have flexible timing and shutdown configurations, as well as control of individual blocks to minimize the total power consumption during downtime to optimize the measurement with securing a high accuracy.

7.1 LED driver

The PPG block in the AS7058 features two independent LED current drivers connected to eight LED input pins via two multiplexers. The two LED current sinks have 8-bit resolution with four programmable full-scale range settings of 25 mA, 150 mA, 225 mA, and 300 mA (typ.). The lowest range with 25 mA is supposed to be used in combination with the VCSEL emitter technology. Both drivers include their protection block to supervise the power supply and interrupt when a malfunction is detected, which would violate laser safety regulations. The configuration of the LED drivers can be uniquely set for each measurement. The **SUBY_DRVX_SEL** defines which LED is selected for each sub sample measurement.

Table 6: LED driver and MUX configuration

Register value	SUBy_DRV1_SEL	SUBy_DRV2_SEL
0	LED1	LED5
1	LED2	LED6
2	LED3	LED7
3	LED4	LED8

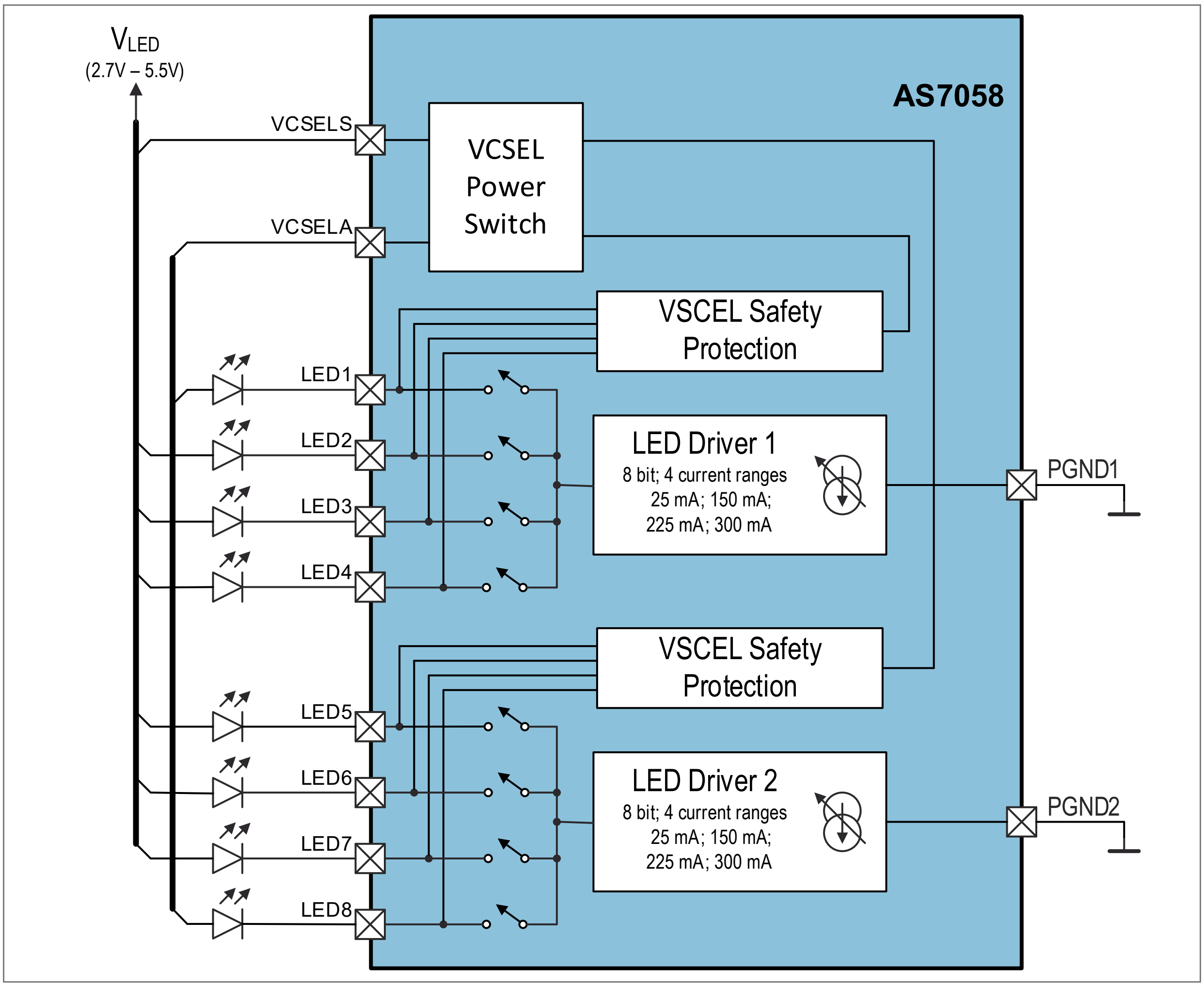
Figure 22 shows how the two LED drivers are connected to the eight LED pins and how the VCSEL protection block is integrated. The minimum LED supply voltage V_{LED} depends on the forward voltage of the selected LEDs and the minimum driver headroom voltage which is shown in Table 7. Since AS7058 current sinks support up to four different current operation ranges the minimum driver headroom voltage is also dependent on the selected LED driver full-scale range. Therefore, the minimum voltage that needs to be applied is the sum of the forward voltage of the LED and the LED driver headroom voltage depending on the selected LED driver full scale range.

Table 7: LED driver full-scale range headroom voltage

LED driver full-scale range (mA)	LED driver headroom voltage (mV)
25	300
150	400
225	550
300	750

The V_{LED} supply voltage must be above the sum of both voltages to enable proper regulation of the LED driver and to guarantee the configured LED current for each driver. A lower supply voltage can result in increased noise behavior and not reaching target LED currents.

Figure 22: LED driver block diagram



The LED driver includes a VCSEL safety protection. This block consists of a PMOS VCSEL supply switch, a watchdog, and two comparators for short circuit detection. The block is activated if the current range for the LED driver is set to 25 mA (**LED_IRNGX** = 0). The **VCSEL_MODE** register provides the selection of the monitored LED pad.

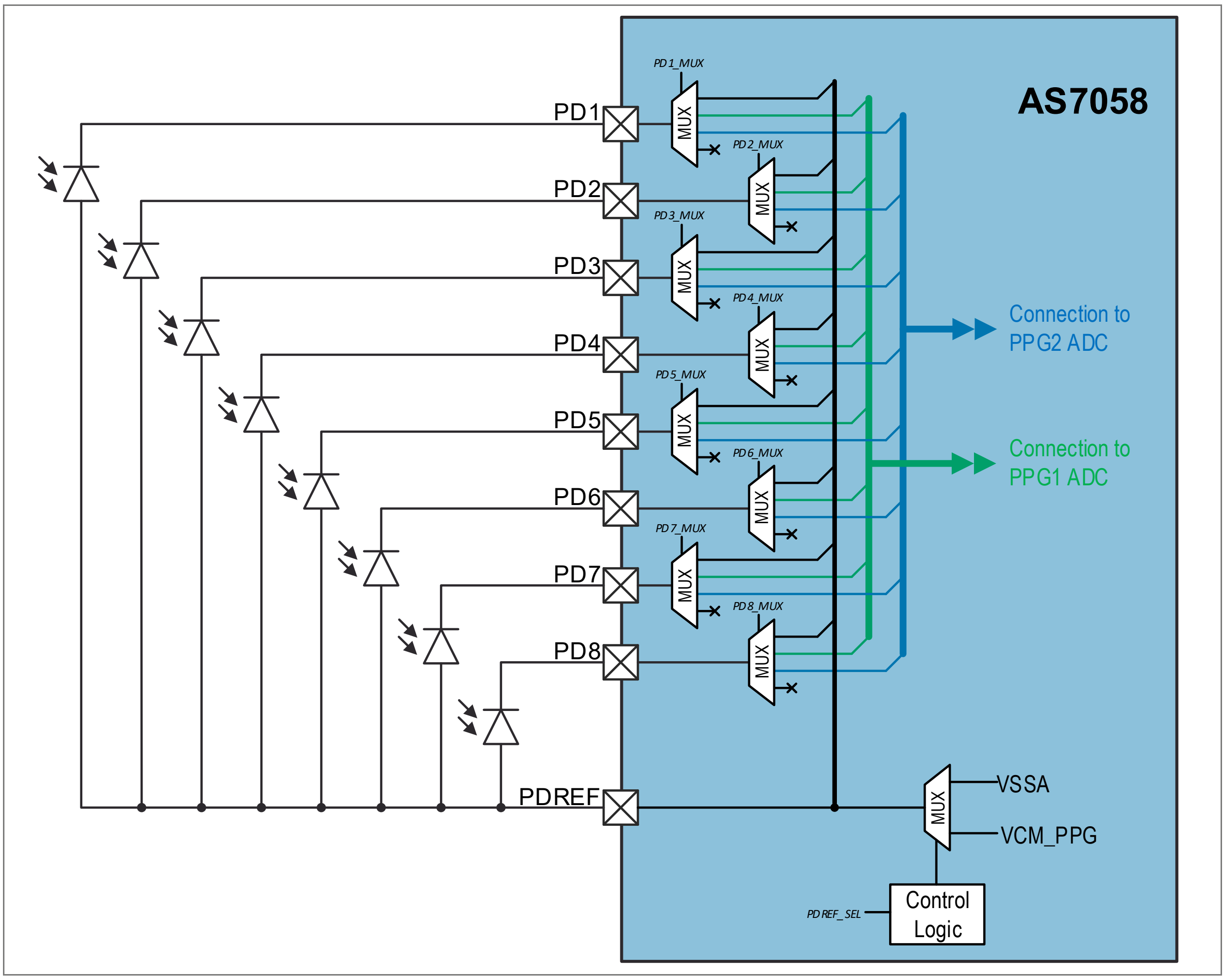
The major events monitored by the protection block are short circuits to VSS and VCSELS pins as well as monitoring the on-time. If the LED on-time is larger than the watchdog time, an interrupt is generated, and the VCSEL power switch is switched off automatically.

In case the block detects any error, the measurement is immediately stopped (e.g. watchdog event) and an interrupt is released. The **STATUS_VCSEL** status register shows the source of the error (a short to VSS, a short to VCSELS, or a watchdog event). If no VCSEL is used, the protection feature can be switched off with the **VCSEL_CFG** register.

7.2 Photodiode inputs

The AS7058 supports up to eight photodiode inputs which can be routed to both PPG modulators for highest design flexibility. A simplified block diagram which shows the input structures of the photodiode inputs is shown in Figure 23. Each photodiode input features a dedicated multiplexer that allows each photodiode to be connected to PPG1 ADC, PPG2 ADC or to PDREF pin which is the default connection to short circuit the photodiodes when not in use. This is also the reset state after power-up and when no measurement is ongoing. The input multiplexers are controlled automatically with the built in measurement sequencer and get connected and disconnected while a measurement is ongoing, according to the device configuration.

Figure 23: Photodiodes input selection



It is also possible to change the PDREF voltage level from typ. 0.8 V to 0 V via register **PDREF_SEL** register.

7.3 PPG ADC1 and ADC2

The PPG data acquisition signal path of AS7058 features two parallel synchronous current input analog to digital converters. Both ADC channels shown in Figure 24 and Figure 25 do provide same functionality and support true synchronous sampling of the assigned photodiode inputs. Therefore, it is possible to read out two photodiodes in a single PPG subsample measurement.

Figure 24: PPG ADC 1 signal path

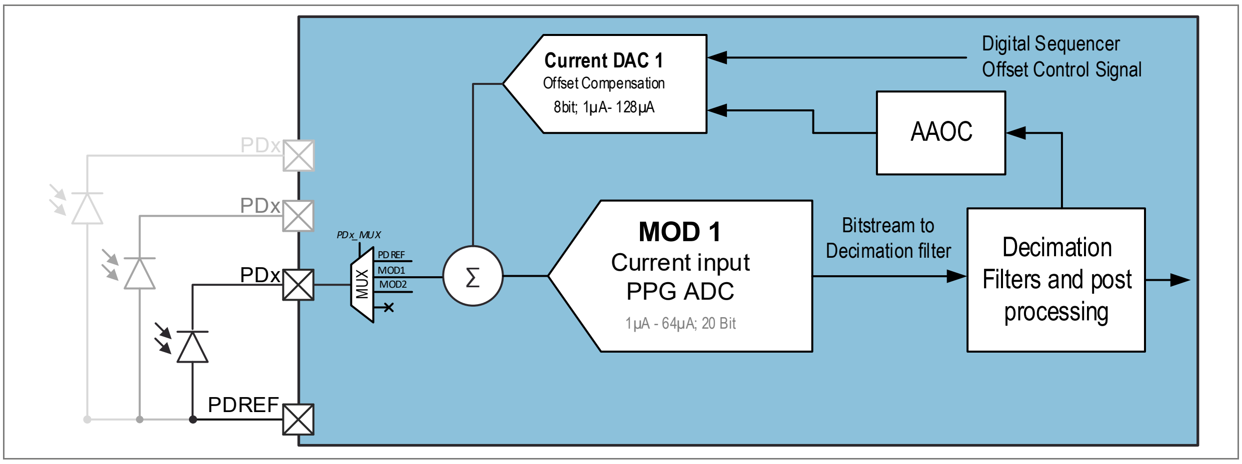
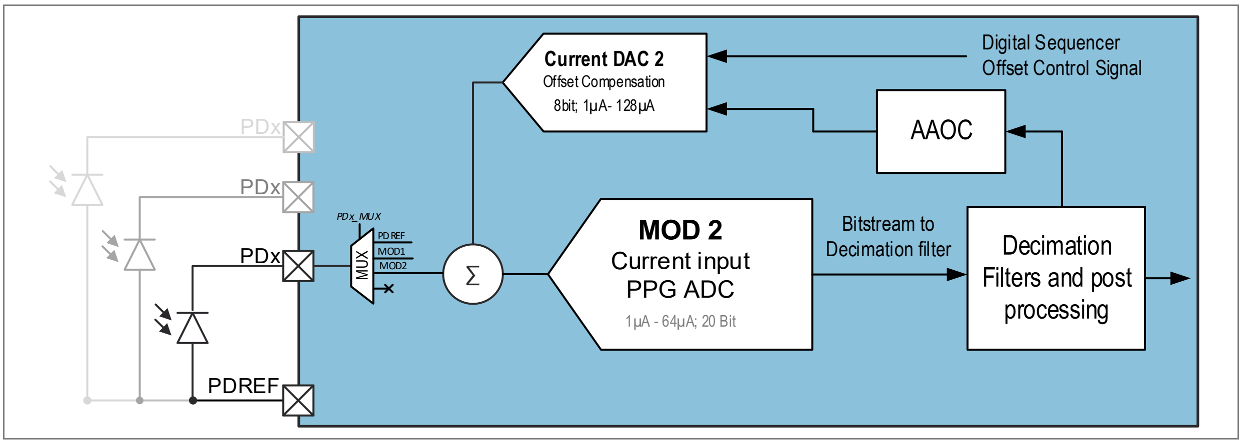


Figure 25: PPG ADC 2 signal path



For applications requiring only one signal path to be active, one of the two channels can certainly be powered down via simple register control to reduce overall system power consumption. Each PPG Modulator signal path supports seven full-scale range settings of 1 µA, 2 µA, 4 µA, 8 µA, 16 µA, 32 µA, and 64 µA which can be configured in register **PPGMOD1_IOS_FS** and **PPGMOD2_IOS_FS** for each ADC independently. In addition to the full-scale settings both modulators have additional configuration registers **PPG_SINC_CFGA**, **PPG_SINC_CFGB** and **PPG_SINC_CFGC** which allow the configuration of the decimation filters and filter order to control the desired integrations times which are the determining factor for signal integrity as well as noise behavior for the target application.

Each PPG signal path also includes an 8-bit offset current DAC for extending the optical dynamic range by sourcing some of the exposure current to the offset DAC. This feature helps to avoid the saturation of the ADC under high ambient light exposure. The current of the offset DAC can be directly controlled via a dedicated registers IOS_PPG1_SUBx and IOS_PPG2_SUBx for each subsample and each modulator separately. This allows engineers to utilize their own offset compensations algorithms running on the host signal-processing unit. However, in case customers do not have an algorithm in place, AS7058 features also an Advanced Automatic Offset Cancellation (AAOC) function which is also shown in Figure 24 and Figure 25 which automatically controls the DC offset compensation DAC eliminating the latency effect caused by I²C configuration of an external host MCU.

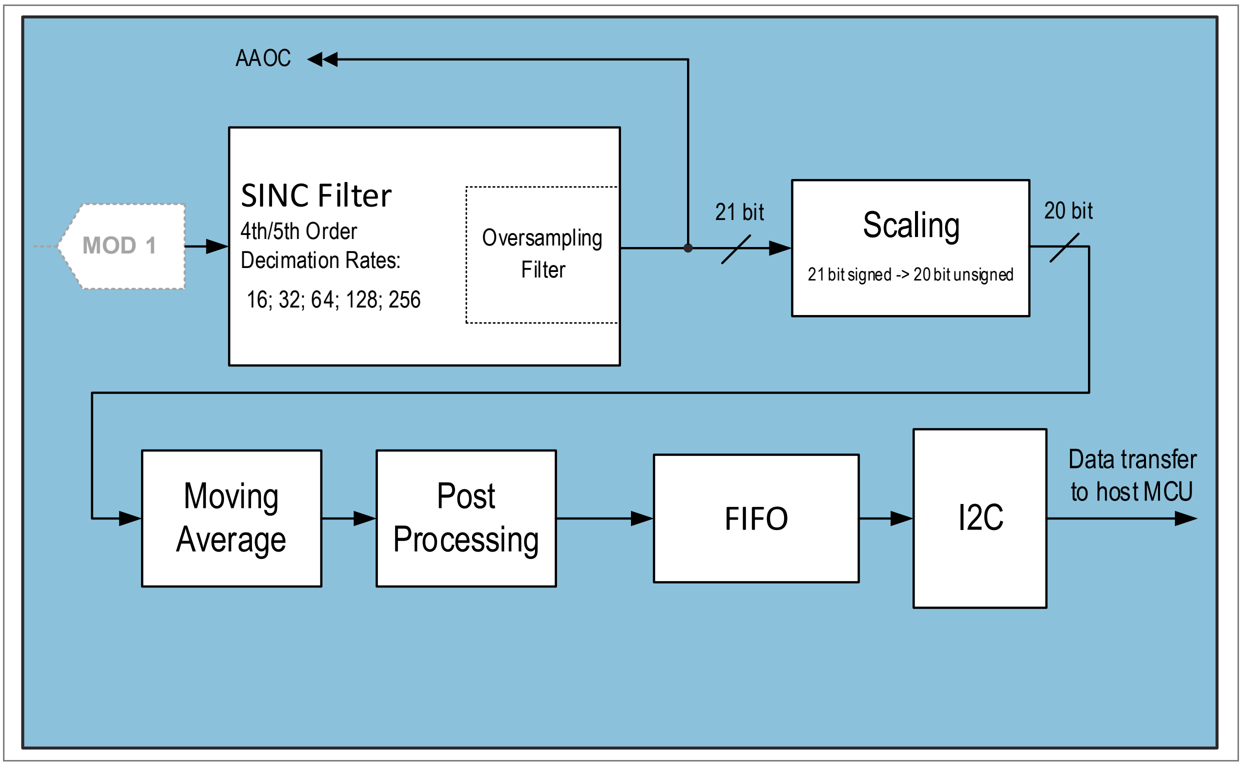
7.3.1 PPG signal processing overview

As indicated in the previous chapters and drawings, AS7058 supports various different post-processing options. An overview of all options and device signal flow is shown in Figure 26. Please note that the processing options shown in Figure 26 are for ADC Modulator 1 and ADC Modulator 2 the same.

The output of each modulator is connected to the SINC filter block, which acts as down sampling filter. It is possible to select between 4th and 5th filter order via register **PPG_SEL_ORDER** as well as decimation rates between 16, 32, 64, 128 and 256 via register **PPG_SINC_DEC**. In order to further improve SNR of the system there is an oversampling filter function, which is part of the down sampling filter, that can be enabled via register **PPG_SINC_OVS**. The three-bit register allows to enable 7 different oversampling filter ratios from factor 2 up to 128. The oversampling filter function is disabled in default configuration. Please mind that enabling the oversampling filter function the active ADC modulator time is increased influencing power consumption with the benefit of better noise behavior. Once the signal passed the SINC decimation and optional oversampling filter the PPG signal is feed into a scaling block which converts the signal in to 20-bit unsigned signal. The next post-processing block, which can be enabled via register **MOVING_AVERAGE_ON** is an on-chip moving average filter.

The number of samples used for the moving average filter varies from 2 samples up to 16 samples and can be configured with register **MOVING_AVERAGE_VAL**. The last processing block, before that data is written to the FIFO memory, is a simple post-processing block. It enables the detection of modulator saturation and manipulation of the saturated data with fixed values. This function can be enabled via register **ASAT_ON**.

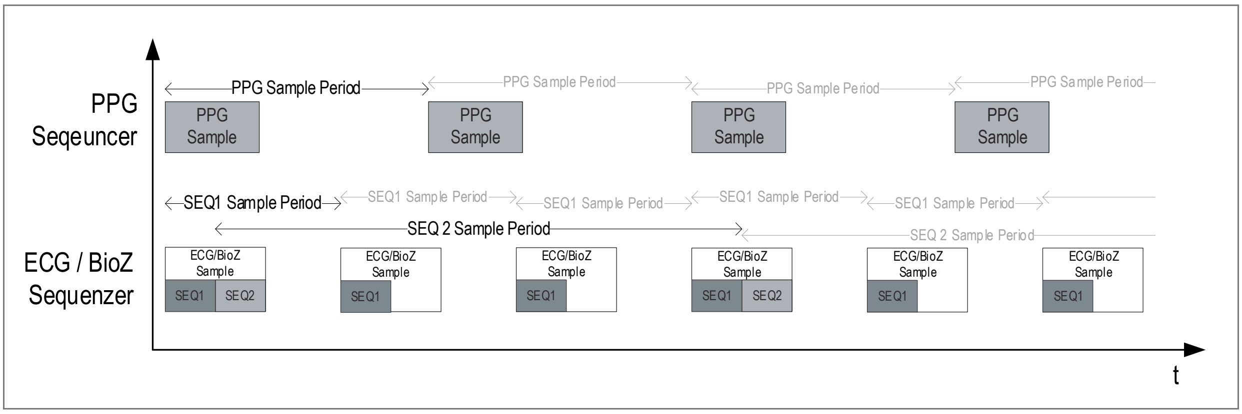
Figure 26: PPG signal processing overview



7.4 PPG/ECG sequencer

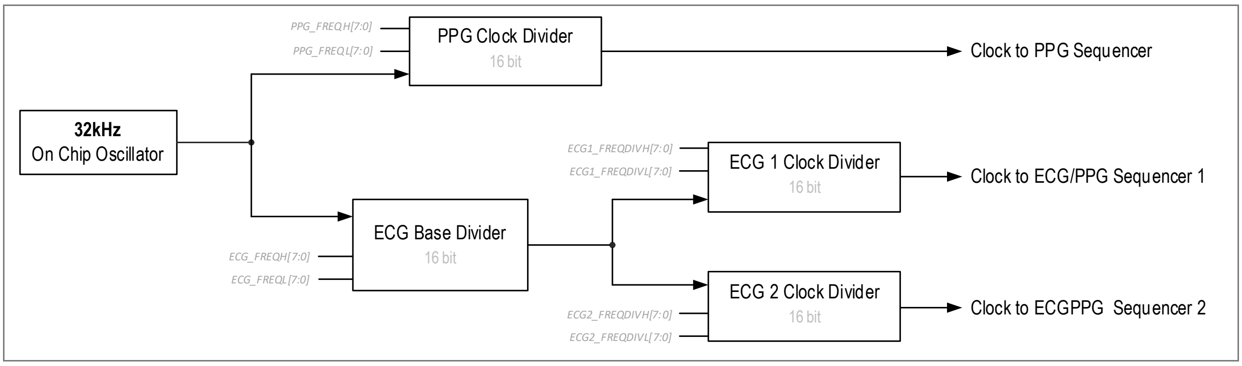
In order to unload MCU with re-occurring measurement tasks to be triggered and its related timing constraints, AS7058 has a built in measurement sequencer which controls all relevant PPG and ECG/Bioimpedance blocks with its corresponding timings. An overview of the sequencer timing diagram is shown in Figure 27.

Figure 27: PPG/ECG sequencer timing diagram



The sequencer basically supports three different sample rates which can be configured independently from each other. All timings for the sequencer are derived from the on-chip 32 kHz oscillator. The PPG measurement channel can be configured independently from the ECG/BioZ sampling periods. Whereas the PPG channel allows for one sample rate for each PPG sample measurement the ECG/BioZ sequencer supports two different sample rates which are called SEQ1 Sample Period and SEQ2 Sample Period. The benefit of having two different sample rates as part of the ECG/BioZ sequencer, like it is shown in Figure 27, is that an ECG measurement can for example run with SEQ2 at a sample rate of e.g. 400 Hz and the AC lead off detection can run with SEQ1 at a much higher frequency.

Figure 28: Sequencer clock generation

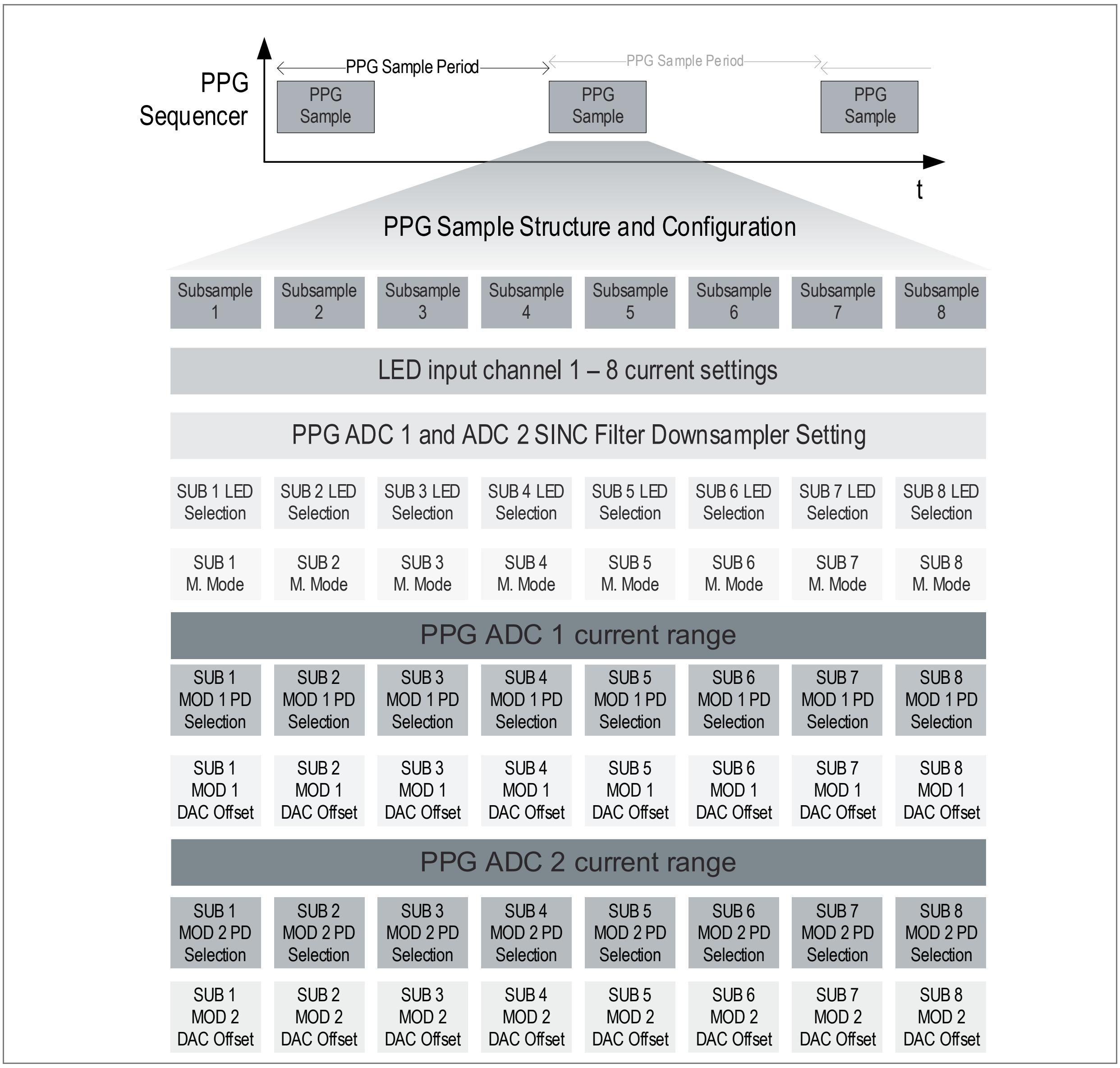


The clock which is used to derive the PPG sample period for the PPG Sequencer is configured with the 16-bit PPG clock divider registers **PPG_FREQH** and **PPG_FREQL**. The clocks and its related sample periods for the ECG/BioZ Sequencer are configured with three additional clock dividers. There is an ECG base divider which is configured with **ECG_FREQH** and **ECG_FREQL** register. The output of the ECG Base Divider is fed into the ECG1 Clock Divider and ECG2 Clock Divider, which define the sampling period for ECG/BioZ Sequencer 1 and Sequencer 2. ECG1 Clock Divider is controlled via register **ECG1_FREQDIVH** and **ECG1_FREQDIVL**. ECG2 Clock Divider is controlled via register **ECG2_FREQDIVH** and **ECG2_FREQDIVL**. An overview of the sequencer clock generation unit is shown in Figure 28.

7.5 PPG sample structure

The AS7058 offers high flexibility in programming all the different combinations of the photodiode and LED pins. The PPG sequencer divides a PPG measurement into PPG samples according to the programmed PPG Sample Period time like it is shown in Figure 27. Each PPG Sample can be divided into a maximum of eight subsamples, which allow for individual configuration. An overview of the configuration options for a PPG Sample is shown in Figure 29. There are general settings and like which LED is assigned to which LED input channel which are the same for each subsample. The LED input channel current settings can be configured with **LEDx_ICTRL** along with the LED current range **LEDx_IRNG** for each LED.

Figure 29: PPG sample structure and configuration options



The second parameter which applies to all enabled subsamples are the settings for the SINC decimation filter and oversampling settings for ADC1 and ADC2 which can be configured in **PPG_SINC_DEC**, **PPG_SINC_OVS** and **PPG_SEL_ORDER**. In addition to the oversampling and LED current settings the LED assignment (**LED_SUBx**) as well as the measurement mode (**PPG_MODE_x**) for each subsample is a setting which is used for both ADC channels like it is shown in Figure 29. In order to maintain best dynamic range and noise behavior it is also important that the current range for ADC1 and ADC2 is configured accordingly. The current range configuration for each ADC applies also to all subsamples in a PGG measurement and can be configured with registers **PPGMOD1_IOS_FS** and **PPGMOD2_IOS_FS**.

Individual configurations for each PPG ADC are the photodiode assignments via register **PPG1_PDSELx** and **PPG2_PDSELx** as well as the offset DAC currents for ambient light rejection which can be configured via **IOS_PPG1_SUBx** and **IOS_PGG2_SUBx** registers.

7.5.1 PPG measurement modes

AS7058 does support three basic measurement modes which are:

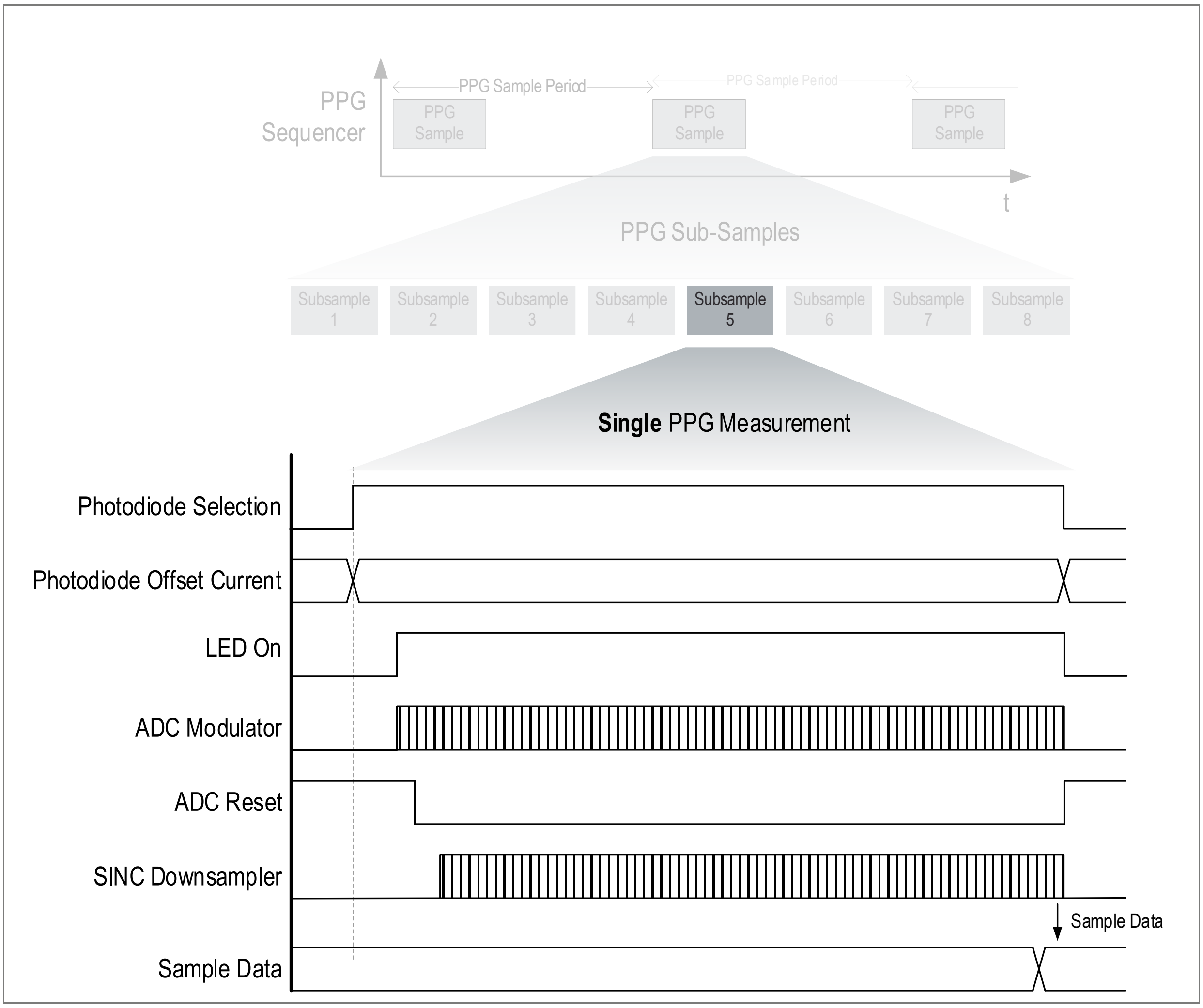
- Single Measurement Mode
- Multi Measurement Mode
- Interleaved Measurement Mode

The three measurement modes covered in this chapter are basic measurement modes which do not support any kind of ambient light compensation. If ambient light compensation measurement modes are desired please refer to chapter 7.5.2 Ambient light compensation. However, it's worth mentioning that all measurement modes for ambient light compensation to rely on the basic principle and timing of the Single Measurement mode which is described in this chapter and illustrated in Figure 30.

7.5.1.1 Single measurement

The Single Measurement mode is the simplest measurement which can be selected and assigned to a subsample as a measurement. A simplified timing diagram to explain the operation mode and working principle of the Single Measurement is shown in Figure 30. Once a Single measurement is executed, the first step in the measurement procedure is that the assigned photodiode is connected via the internal multiplexers to the selected ADC channel. At the same time a DAC offset current, which is setup in the **IOS_PPG1_SUBx** for, is applied to the summing node of the selected ADC and the photodiode input. After a short delay, which can be configured as part of the chip configuration, the LEDs with the configured LED currents are enabled for the measurement and in parallel, the ADC modulator is started. After a configurable modulator reset time, the SINC down-sampler filter is fed with data. The measurement time depends now very much on the configuration of the SINC filter, filter order and internal clock speed of AS7058. Once the measurement time has elapsed the sample data is written to the FIFO memory and ready for readout by a host MCU.

Figure 30: Single measurement mode – simplified timing diagram



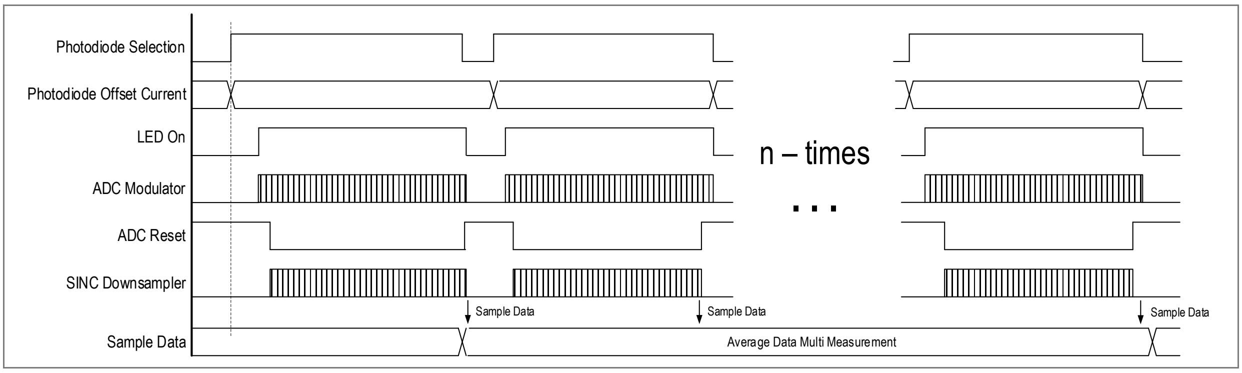
7.5.1.2 Multi measurement

The Multi Measurement operation mode is used to further enhance signal quality and allows for on-chip averaging over a predefined number of measurements. At the end of the measurement, one average value is stored to the FIFO memory.

The advantage compared to a standard moving average filter is the reduction of the time difference between the used sub-samples for averaging. The multi measurement uses multiple subsample timings with close to 0-time difference in comparison when a moving average filter is used. The used data is one sub-sample out of one sampling period. This is stacked over time to achieve the average. Therefore, the overall time until an averaged value is available is shortened with multi measurement in comparison to a standard moving average filter approach.

The total measurement time is then related to the amount of multi measurements, which can be set in the **PPG_MODEx** register. This functionality can also be used with the Ambient Light Compensation Measurement modes described in chapter 7.5.2. A simplified timing diagram for a Single Measurement with activated Multi Measurement is shown in Figure 31.

Figure 31: Multi measurement mode – simplified timing diagram



7.5.2 Ambient light compensation

AS7058 offers up to three different options to compensate for ambient light influences while a measurement is ongoing. This chapter provides a detailed description of Double Measurement, Tripple Measurement and the Advanced Automatic Offset Compensation (AAOC).

7.5.2.1 Double measurement

The double sampling function measures two values within a subsample. The first measurement is the same like a single measurement with the LED enabled and the configured offset current is applied to the ADC input channel. The sample data is stored temporarily in the memory. The second part of the measurement is done with the LED disabled which represents an ambient light measurement. The difference between the first measurement and the ambient light measurement is stored in the FIFO memory.

Equation 1: Double measurement result calculation

$$C_{DOUBLE} = C_{LED_{ON}} - C_{LED_{OFF}}$$

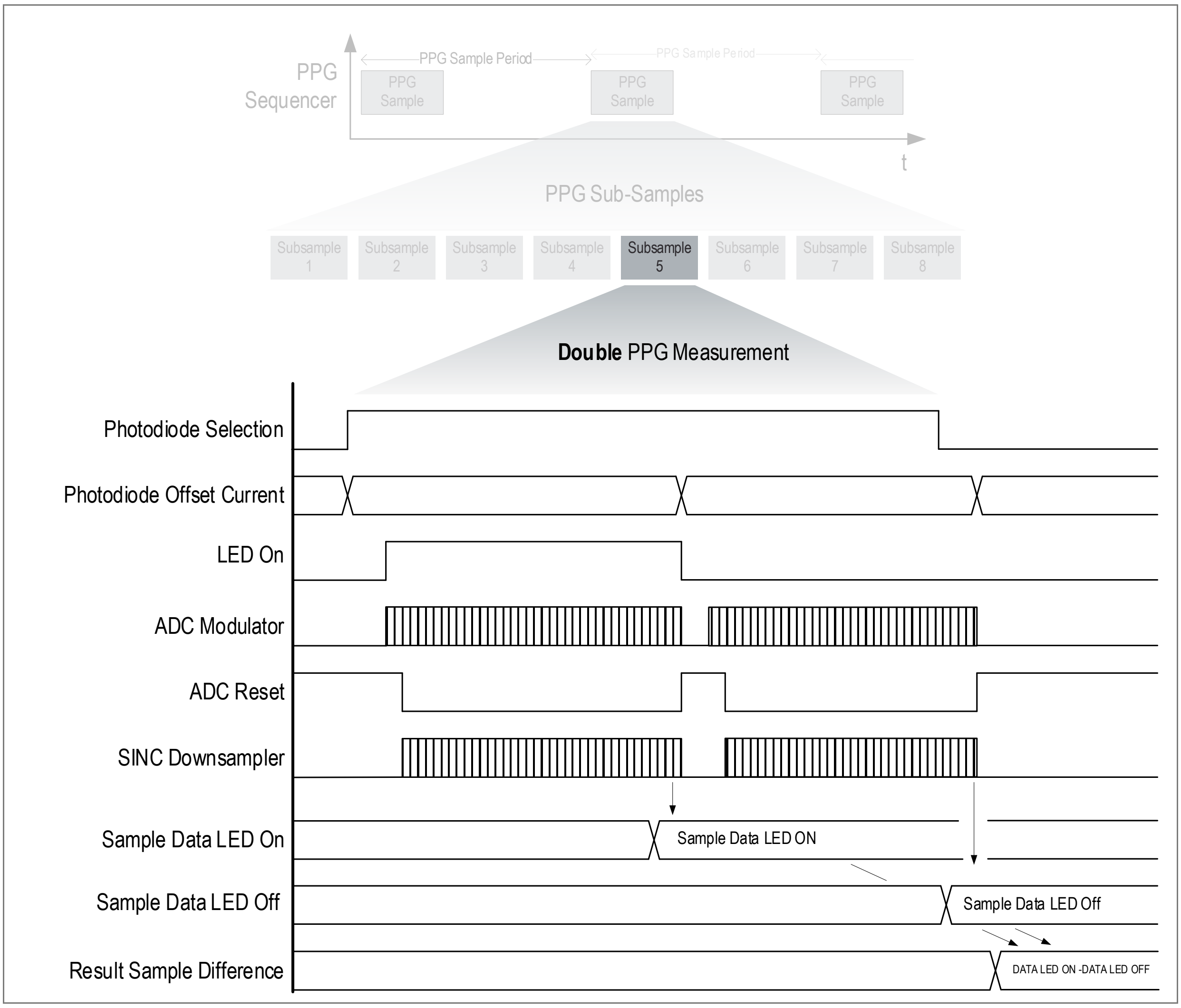
C_{DOUBLE} ... $Double\ Measurement\ result\ stored\ to\ FIFO$

$C_{LED_{ON}}$ ... $ADC\ count\ value\ during\ LED\ on\ phase$

$C_{LED_{OFF}}$ ... $ADC\ count\ values\ during\ LED\ off\ phase$

The assignment of the photodiodes is for both measurements the same. The programmed DAC offset current is used for the first measurement and can also be used for the second measurement (**DIS_LEDOFF** = 1). Alternatively, it is possible to use also a different value, which is stored to **IOS_LEDOFF** register, for all subsamples if register **DIS_LEDOFF** bit is cleared.

Figure 32: Double measurement mode – simplified timing diagram



7.5.2.2 Tripple measurement

The Tripple Measurement function measures three different values within a subsample. The first measurement is an ambient light measurement with the LED disabled. The result of this sampling is stored temporarily to the device. The ambient light measurement is followed then by a measurement where the LED is enabled with the predefined LED current. Its measurement results is again stored temporarily to the device memory. The last part of a Tripple Measurement is again an ambient light measurement where the LEDs are disabled. Its result is also stored temporarily to the device memory and used for the calculation for the final measurement value which is stored to the FIFO memory. The calculation of the value stored to the FIFO memory is shown in Equation 2.

Equation 2: Tripple measurement result calculation

$$C_{TRIPPLE} = C_{LED_{ON}} - \frac{C_{LED_{OFF_1}}}{2} - \frac{C_{LED_{OFF_2}}}{2}$$

$C_{TRIPPLE}$ … FIFO Tripple Measurement result

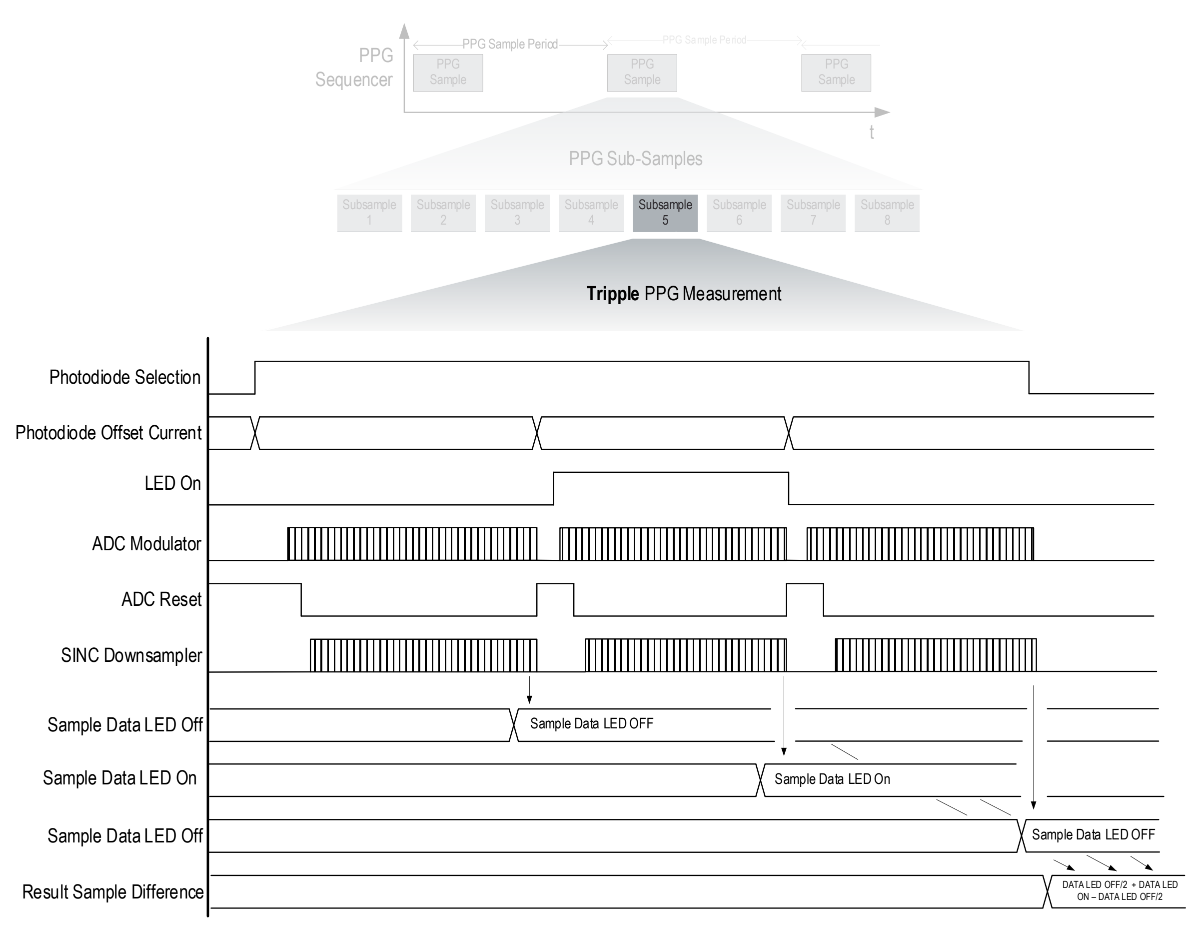
$C_{LED_{ON}}$ … ADC count value during LED on phase

$C_{LED_{OFF1}}$ … ADC count values during first LED off phase

$C_{LED_{OFF2}}$ … ADC count values during second LED off phase

The assignment of the photodiodes is for all three measurements the same. The programmed DAC offset current is used for the second measurement but can also be used for the first and third measurement (**DIS_LEDOFF** = 1). Alternatively, it is possible to use also a different value during the LED off measurement phases which is stored to **IOS_LEDOFF** register if register **DIS_LEDOFF** bit is cleared.

Figure 33: Tripple measurement mode – simplified timing diagram

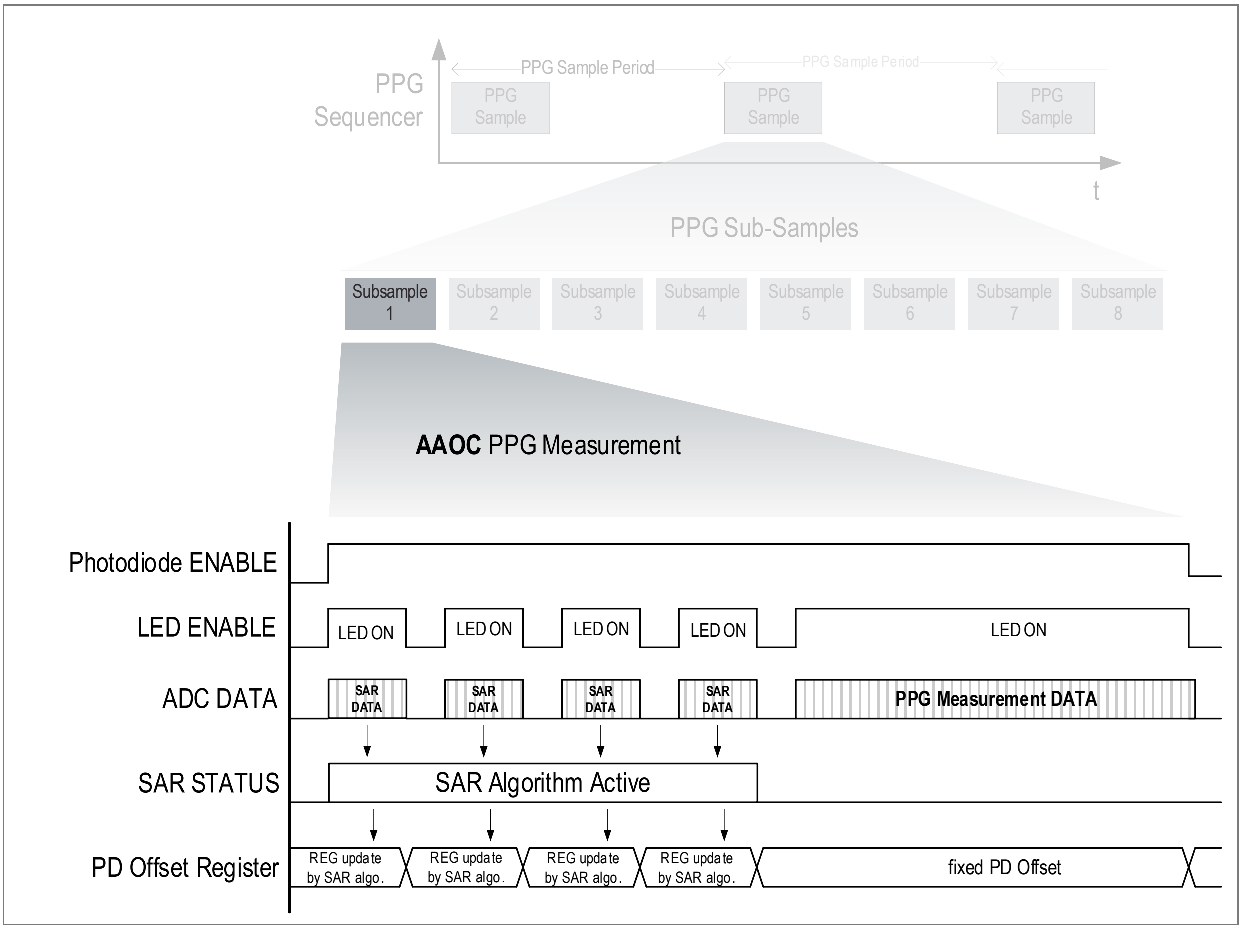


7.5.2.3 Advanced automatic offset compensation (AAOC)

The built in AAOC is an advanced ambient light compensation solution which does not require an external host to adjust the DAC offset current. In conventional approach with Double Measurement and Tripple Measurement the DAC offset current registers need to be controlled and adjusted by a host MCU via I²C or SPI interface. This approach might require several measurement iterations until an appropriate offset value is found. The AAOC function eliminates the need of MCU interaction to find the correct photodiode offset current. It is based on a successive approximation approach to determine the upper 4 bits of the photodiode offset register. In order to achieve this and adjust the 4 bits accordingly. AS7058 does four short measurements prior to the actual PPG measurement like it is shown in Figure 34. During each pre-measurement cycle the LED is also switched on and the ADC data read is feed into the SAR algorithm which adjusts the photodiode current.

Once all four pre-measurements are done the offset current is adjusted correctly to avoid saturation of the ADC due to ambient light. The upper 4 bits of **IOS_PPGx_SUBx** registers are determined automatically with the first four samplings, the lower 4 bits correspond to the programmable bits. The FIFO stores the AAOC data and the ADC results to simplify signal reconstruction for algorithm developers. The programmed current values for the LEDs are used for all five measurements. The assignment of the photodiodes is also fixed for all 5 measurements.

Figure 34: AAOC – simplified timing diagram



7.5.3 Parameter

This chapter contains the detailed timing diagrams and parameters for the PPG samples.

Figure 35: Single measurement timing diagram

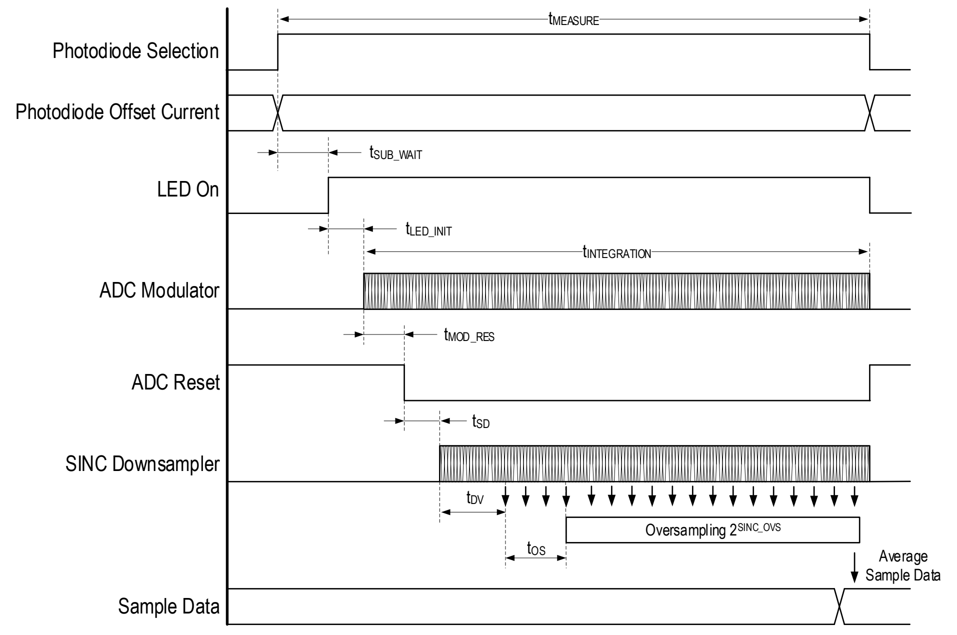


Figure 36: Double measurement timing diagram

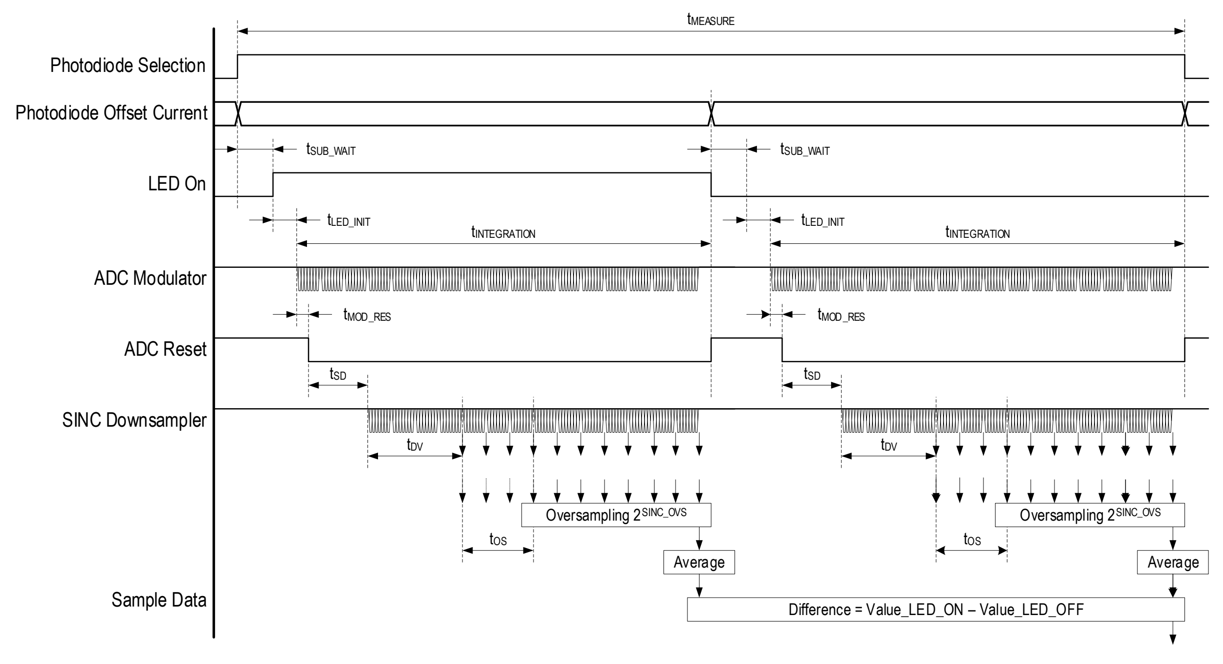


Figure 37: Tripple measurement timing diagram

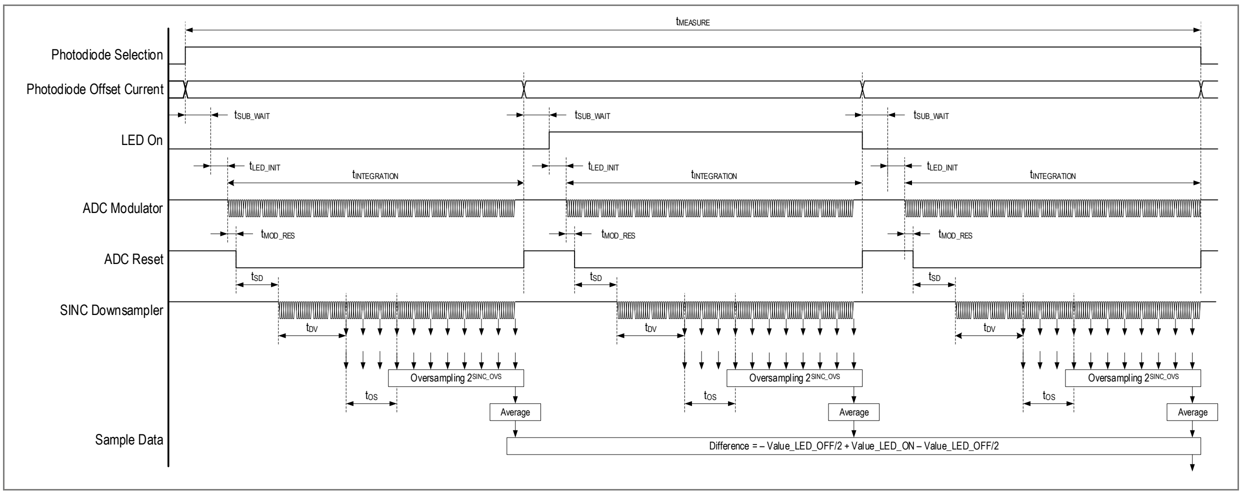


Figure 38: AAOC timing diagram

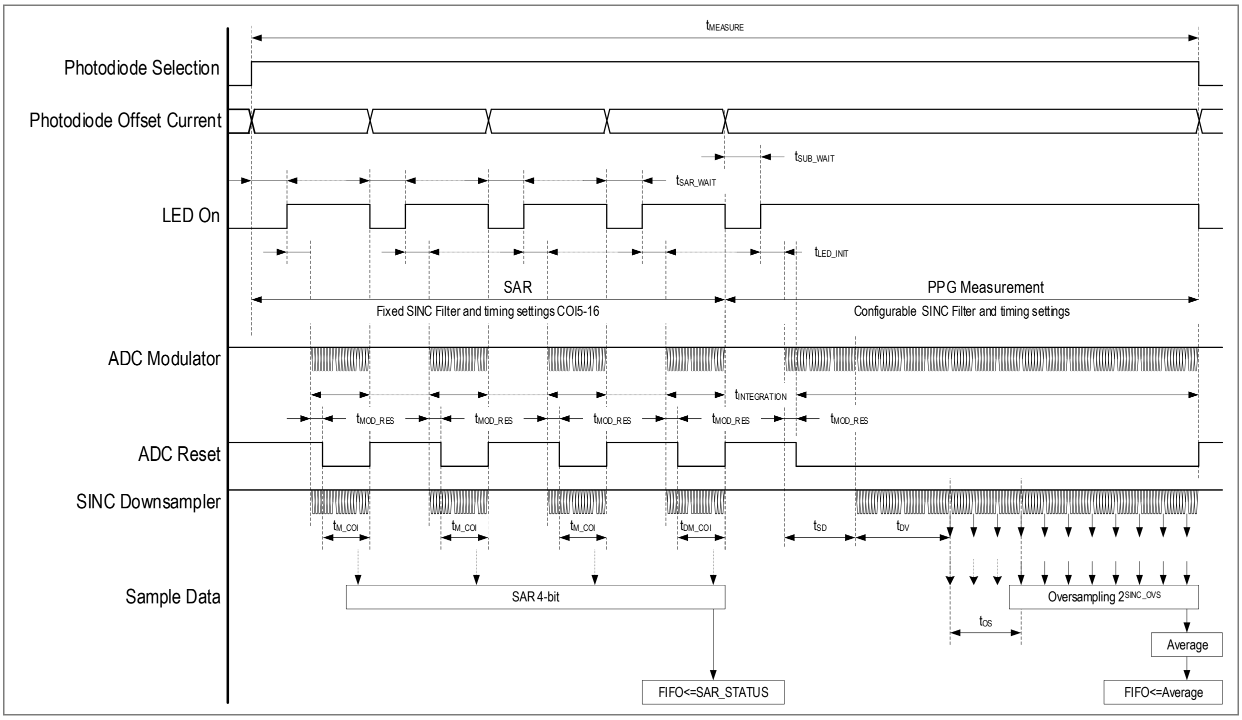


Table 8: Timing parameter measurement modes

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SUB_WAIT}	subsample wait time	Parameter controlled via *sub_wait* register	0		255	µs
t_{LED_INIT}	LED initialization time	Parameter controlled via *led_init* register	0		255	µs
t_{MOD_RES}	ADC modulator reset time	Parameter controlled via *ppgmod_reset_delay* register; *ppgmod_clk* = 0;	0.4		25.5	µs
t_{SD}	SINC downsampler start delay	Parameter controlled via *ppg_start_delay* register; *ppgmod_clk*=0;	0		25.5	µs
t_{SAR_WAIT}	AAOC SAR wait time	Parameter controlled via *sar_wait* register	0		255	µs
t_{M_COI}	SAR modulator on time	*ppgmod_clk=0*		2.7		µs
		ppgmod_clk=1		5.4		µs
		ppgmod_clk=2		10.8		µs
		ppgmod_clk=3		21.6		µs

The measurement time $t_{MEASURE}$ is influenced by many parameters like modulator clock, filter order and decimation filter setting. Table 9 provides example register configurations with the resulting measurement times $t_{MEASURE}$ depending on the modulator clock settings. In case additional information about different register settings are required please do consult your local ams OSRAM support team for assistance.

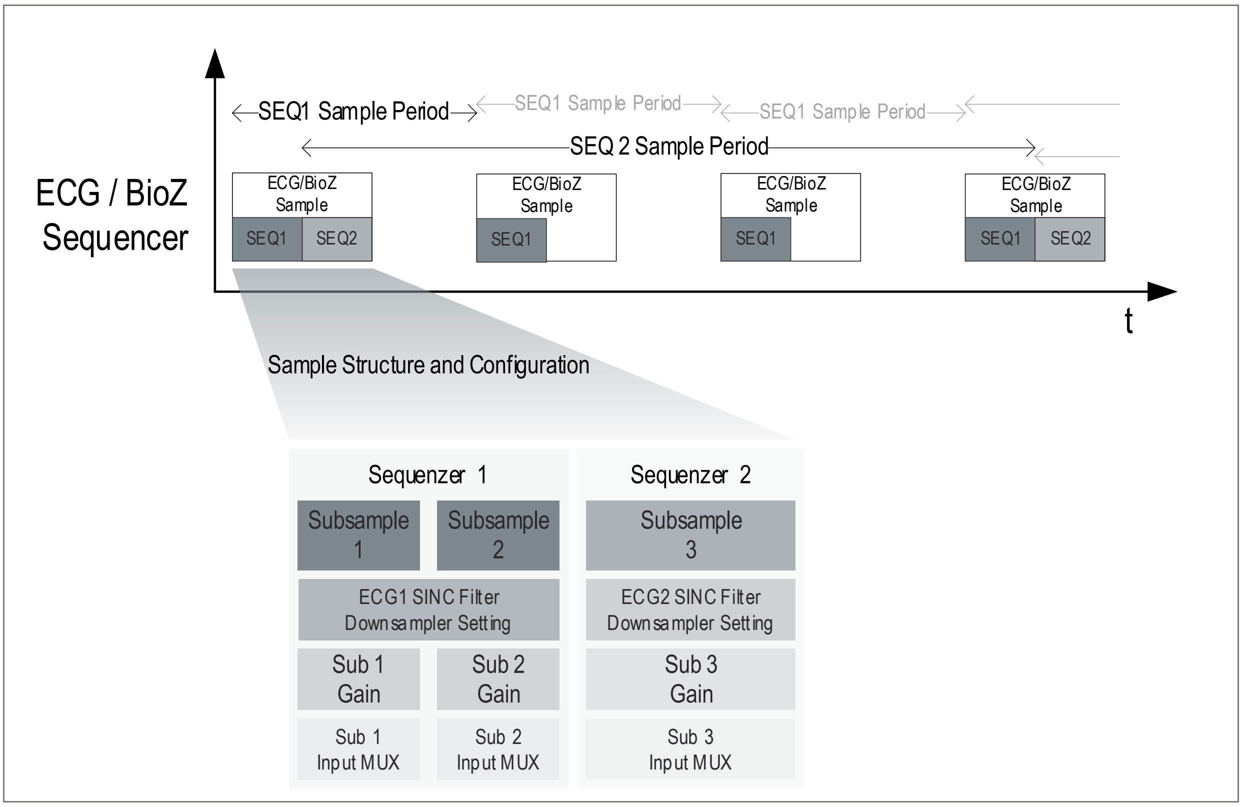
Table 9: $t_{MEASURE}$ examples for different register settings

Register	**Register example configurations**								
filter_mode	1	1	1	1	1	1	1	1	1
sel_order	1	1	1	1	1	1	1	1	1
seset_delay	0	0	0	0	0	0	0	0	0
start_delay	0	0	0	0	0	0	0	0	0
sinc_dec	0	1	2	3	4	1	2	3	4
os_delay	0	0	0	0	0	0	0	0	0
sinc_ovs	0	0	0	0	0	1	2	4	7
PPG modulator clock (f_{MOD_CLK})	**$t_{MEASURE}$ [µs]**								
10 MHz	9.1	17.1	33.1	65.1	129.1	20.3	52.3	257.1	3380.3
5 MHz	18.2	34.2	66.2	130.2	258.2	40.6	104.6	514.2	6760.6
2.5 MHz	36.4	68.4	132.4	260.4	516.4	81.2	209.2	1028.4	13521
1.25 MHz	72.8	136.8	264.8	520.8	1032.8	162.4	418.4	2056.8	27042

7.6 ECG/BioZ sample structure

The ECG/BioZ sequencer supports two sequencers (Sequencer 1 and Sequencer 2) which can run with two different sample periods. Sequencer 1 has the option to enable two sub-samples which is typically used for bioimpedance measurements where in subsample 1 the amplitude and in subsample 2 the phase is measured. Sequencer 2 supports only one subsample which is called subsample 3 shown in Figure 39. This subsample can be used to support AC lead off detection which would require a different sample rate than an ECG measurement which can be assigned to Sequencer 1.

Figure 39: ECG/BioZ sample structure and configuration options



The sample frequency, which can be programmed, uses a 32 kHz clock as the base frequency. An overview about the clock generation of the ECG/BioZ Sequencer is shown in Figure 28. Typical ECG sampling frequencies and the necessary register configuration for the clock dividers is shown in Table 10.

Table 10: ECG sample frequencies with CGU register settings

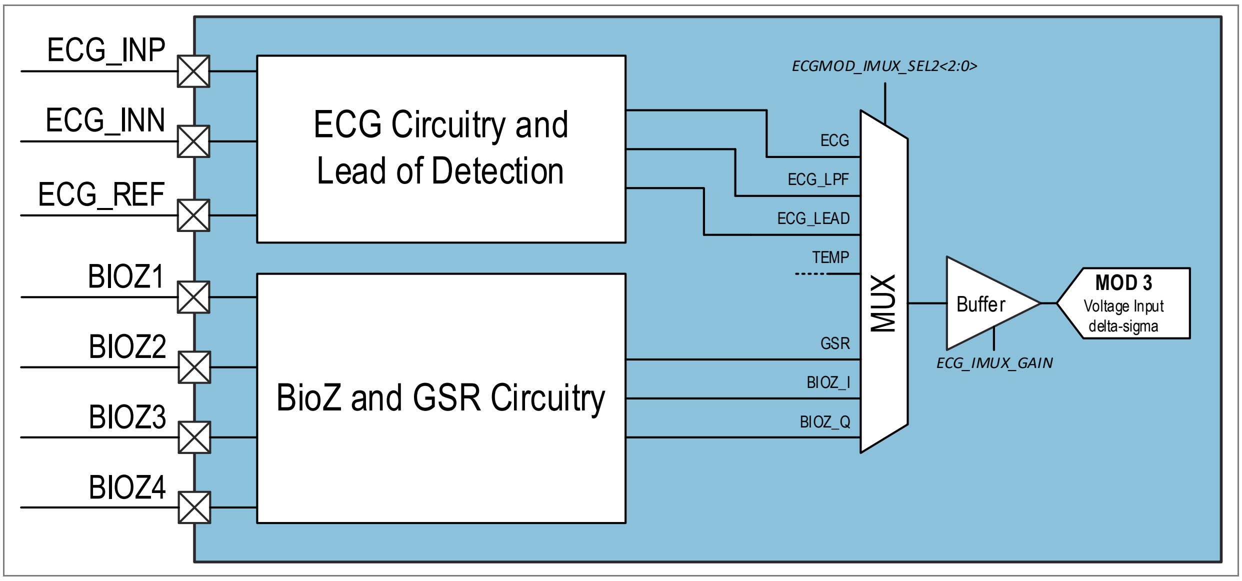
Sample frequency (Hz)	Register ECG_FREQ[7:0]	ECG1_FREQDIV[7:0] ECG2_FREQDIV[7:0]
400	‘d’79	‘d’0
500	‘d’63	‘d’0
1000	‘d’31	‘d’0
2000	‘d’15	‘d’0
4000	‘d’7	‘d’0

In addition to the correct clock configuration Sequencer 1 and Sequencer 2 do have dedicated registers for the SINC down-sampler filters to be configured. Different measurements assigned to the subsamples might require different filter configuration. Another important parameter which can be configured individually is the gain of the modulator preamplifier which can be either 1 or 2 and be configured with register **SUBx_IMUX_GAIN**. Since modulator 3 which is assigned to ECG/BioZ Sequencer can measure different features like ECG, BioZ or temperature it is also necessary to configure the correct input source to the ADC via input multiplexer register **SUBx_IMUX_SEL2**. A more detailed description of the ECG/BioZ modulator and its input structure is described in 7.7.

7.7 ECG/BioZ ADC3

The third build in ADC of AS7058 is used to serve ECG, Bioimpedance and Galvanic Skin Response (GSR) applications. The ECG and BioZ/GSR measurement pins are feed into the corresponding measurement hardware like it is shown in Figure 40. The output signals of these blocks are connected to a common multiplexer which can be configured via **ECG_IMUX_SEL2** register. Depending on what should be measured the multiplexer configuration register has to be configured accordingly to address ECG or Bioimpedance measurements. The multiplexer is then followed by a buffer whose gain can also be configured via **ECG_IMUX_GAIN** register. Both registers, **ECG_IMUX_SEL2** and **ECG_IMUX_GAIN**, are also part of the subsample configuration as part of the ECG/BioZ sequencer described in chapter 7.6.

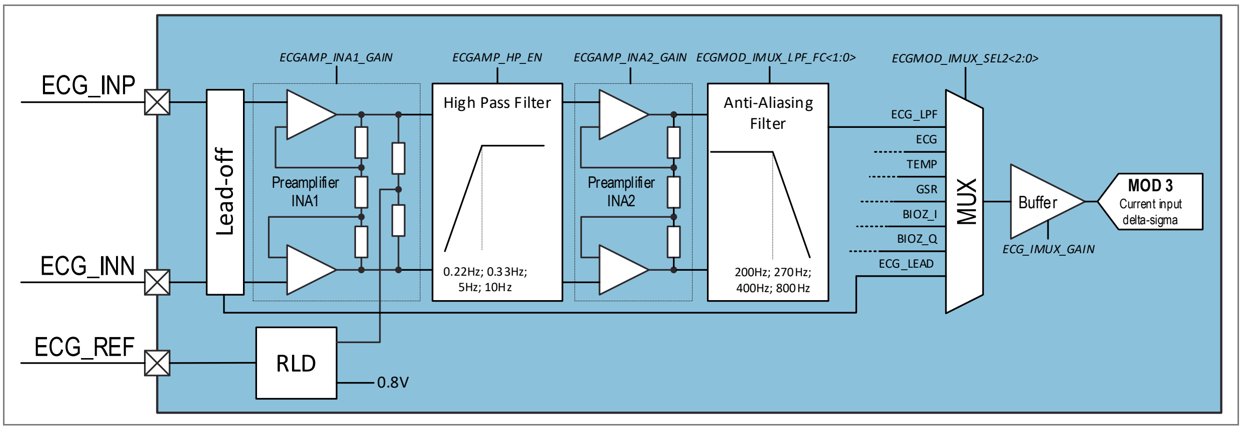
Figure 40: ECG/BioZ ADC3 signal path



7.7.1 ECG measurement system

The ECG (electrocardiogram) amplifier is a high impedance, low noise instrumentation amplifier with a configurable integrated high-pass filter. It also includes circuitry to apply a stimulus to the inputs to detect lead-off conditions by post-processing the input signals in the digital domain. In order to further improve noise performance, it is recommended to enable digital post processing filters to attenuate 50 Hz and 60 Hz noise signals. Please refer to chapter 7.7.2 for on-chip signal processing options.

Figure 41: ECG amplifier block diagram



The ECG signal amplification is obtained from two stages of amplification which are INA1 and INA2 like it is shown in Figure 41. The first amplifier stage INA1 does support 4 different gain settings which can be configured via register **ECGAMP_INA1_GAIN**. The second preamplifier INA2 features a gain range from 1 to 128 which can be configured via **ECGAMP_INA2_GAIN** register. Both amplifiers can enable the chopper operation mode via registers **ECGAMP_CHOP1_EN** and **ECGAMP_CHOP2_EN**. They also have separate chopper clock signals whose chopper frequency can be controlled via **ECGAMP_CHOP1_CLK** and **ECGAMP_CHOP2_CLK** register.

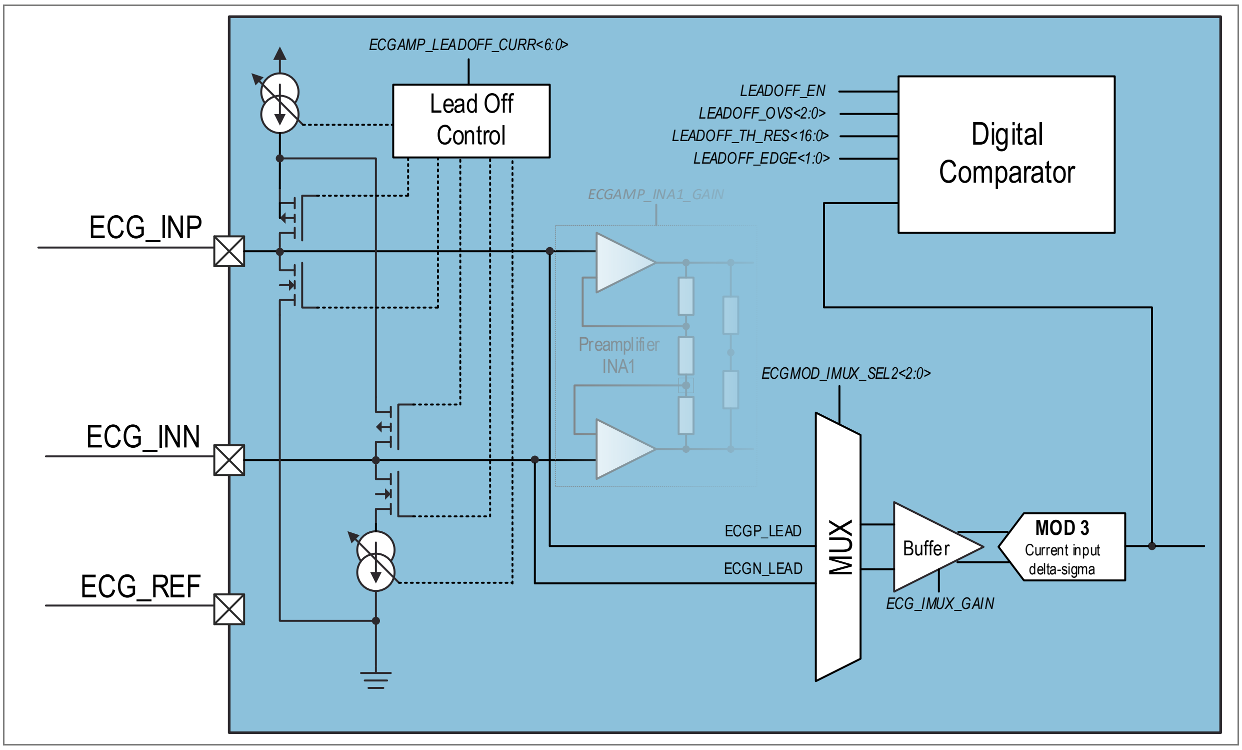
The integrated high pass filter does support four different cutoff frequencies with 0.22 Hz, 0.33 Hz, 5 Hz and 10 Hz which can be enabled with register **ECGAMP_HP_EN**. The cut of frequency is a function of the filter clock and internal filter capacity and can be configured via registers **ECGAMP_HP_CSEL** and **ECGAMP_HP_CLK_FREQ**. In case a high pass filter function is not desired in the target application the filter can also be bypassed by enabling register **ECGAMP_HP_BYP**. In order to avoid aliasing effect, when sampling the ECG input signal, the ECG block incorporates also an anti-aliasing filter block. The cut off frequency can be configured to 200 Hz, 270 Hz, 400 Hz and 800 Hz via register **ECGMOD_IMUX_LPF_FC** register. In case the anti-aliasing filter is not needed in the ECG signal chain, it is also possible to bypass the anti-aliasing filter via the ADC input multiplexer.

The multiplexer can be configured via register **ECGMOD_IMUX_SEL2** register by selecting ECG input instead of ECG_LPF setting.

7.7.1.1 Lead off detection

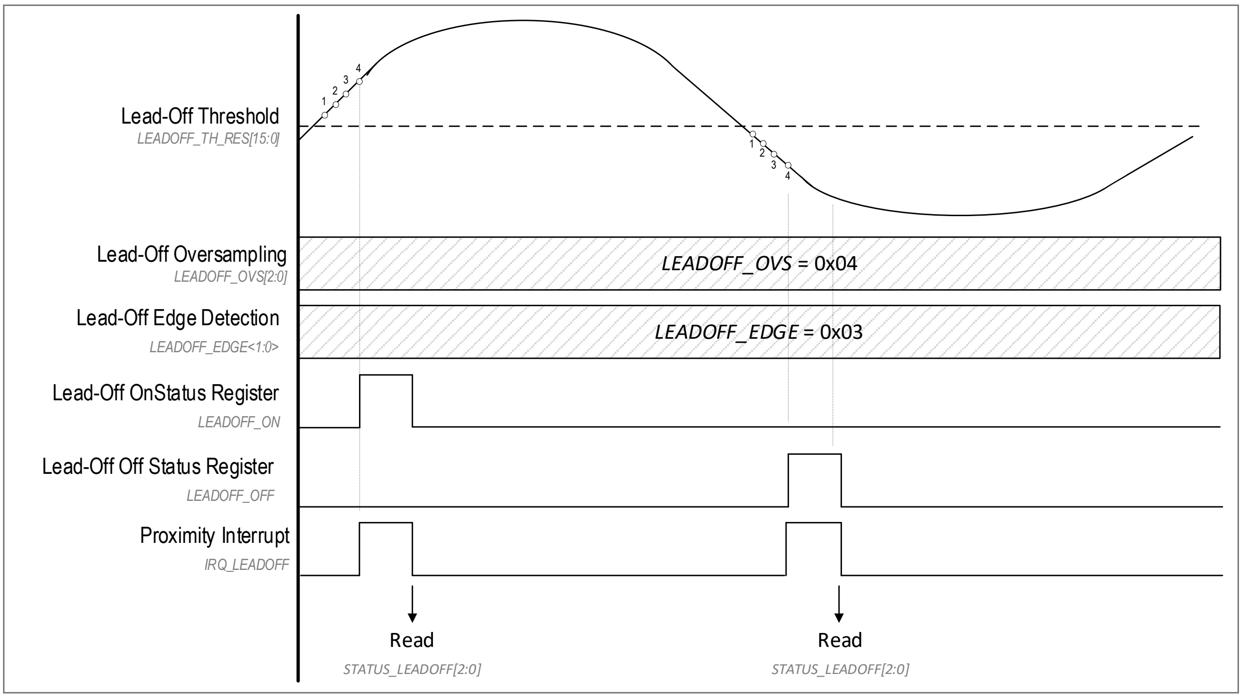
The ECG Lead Off circuit is a differential current source intended to apply a stimulus for lead off detection to the ECG inputs. A simplified block diagram is depicted in Figure 42 below. The square waved stimulus current can be configured via register **ECGAMP_LEADOFF_CURR** register. The lead off clock which controls the lead off transistors is linked to the ECG/PPG Sequencer and half the sequencer clock frequency. With each clock cycle of the sequencer the polarity of the lead off current is changing resulting in a stimulus signal which is half the frequency of the ECG/PPG Sequencer clock.

Figure 42: ECG lead off detection block diagram



In response to that stimulus, the voltages at the ECG input will change and depend on the impedances between electrodes and skin. These voltages can be measured by MOD3 directly via the modulator input multiplexer that can be configured via **ECGMOD_IMUX_SEL2** register like it is shown in Figure 42. The output of MOD3 is connected to a digital comparator which can be programmed with a certain threshold (**LEADOFF_TH_RES**) for the leadoff detection to create an interrupt for host notification. There is also an oversampling function implemented which can be configured via **LEADOFF_OVS** register. Its value defines how many ADC readings must be above or below the defined threshold that a lead off condition is detected and an interrupt is generated. In addition to the oversampling function it is also possible to configure if the comparator triggers on the positive and negative edge of the lead off signal. This function can be configured with the register **LEADOFF_EDGE**. A simplified timing diagram which shows the use of the oversampling function is shown in Figure 43. In case of a rising edge of the ECG input signal voltage which is four times above the threshold value the **LEADOFF_ON** register bit is set and an interrupt (**IRQ_LEADOFF**) is released. The interrupt as well as the lead off status bits are cleared once the **STATUS_LEADOFF** register is read.

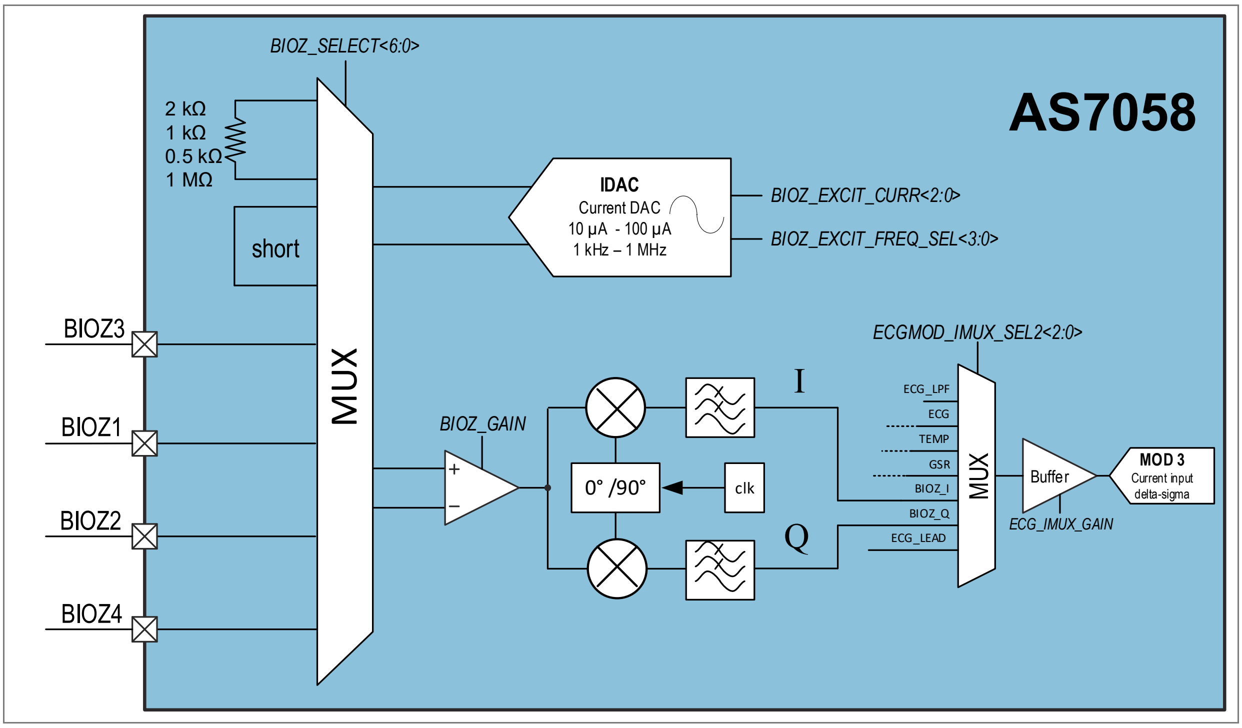
Figure 43: Lead off detection timing diagram



7.7.2 BioZ/GSR measurement system

Bioelectrical impedance analysis is a method of assessing body composition, such as body fat, fluid levels, and tissue mass. A small AC current is applied, which flows through the body, and the voltage is measured so the bioimpedance can be calculated. The bioimpedance channel consists of an input MUX, a capacitive-coupled amplifier, I/Q demodulation mixers, two anti-aliasing filters, a pseudo-sine current DAC, and an internal reference resistor that is used to calibrate the errors in the signal path and used as a measuring scale. A simplified system block diagram of the BioZ/GSR measurement system is shown in Figure 44.

Figure 44: BioZ/GSR block diagram



The included MUX can freely combine the BIOZ1 pin to BIOZ4, as well as the input and output of the current DAC and the BioZ amplifier. The selection can be set with **BIOZ_SELECT** (see chapter 8.1 Register overview).

Two different modes can be chosen:

- Body impedance measurement (BioZ)
- Galvanic skin response (GSR)/Electro Dermal Activity (EDA)

The chosen mode influences which excitation waveform, sine wave for the BioZ, and square wave for GSR, is used. Furthermore, the applied current range and excitation frequency are different. The choice between the two modes can be done in **BIOZ_CFG** register (see chapter 8.1 Register overview). Important to mention is that **BIOZ_EN** and **GSR_EN** must not be set to 1 at the same time. When BioZ is activated, the excitation frequency can be chosen in steps from 1 kHz to 1 MHz on a sine waveform, and the current can be controlled from 10 µA to 100 µA. These settings can be chosen in **BIOZ_EXCIT** register. The settings will only be applied when **BIOZ_EN** bit is set to one. The operating gain of the BioZ/GSR preamplifier can also be extended to gain 2 via register bit **BIOZ_GAIN**.

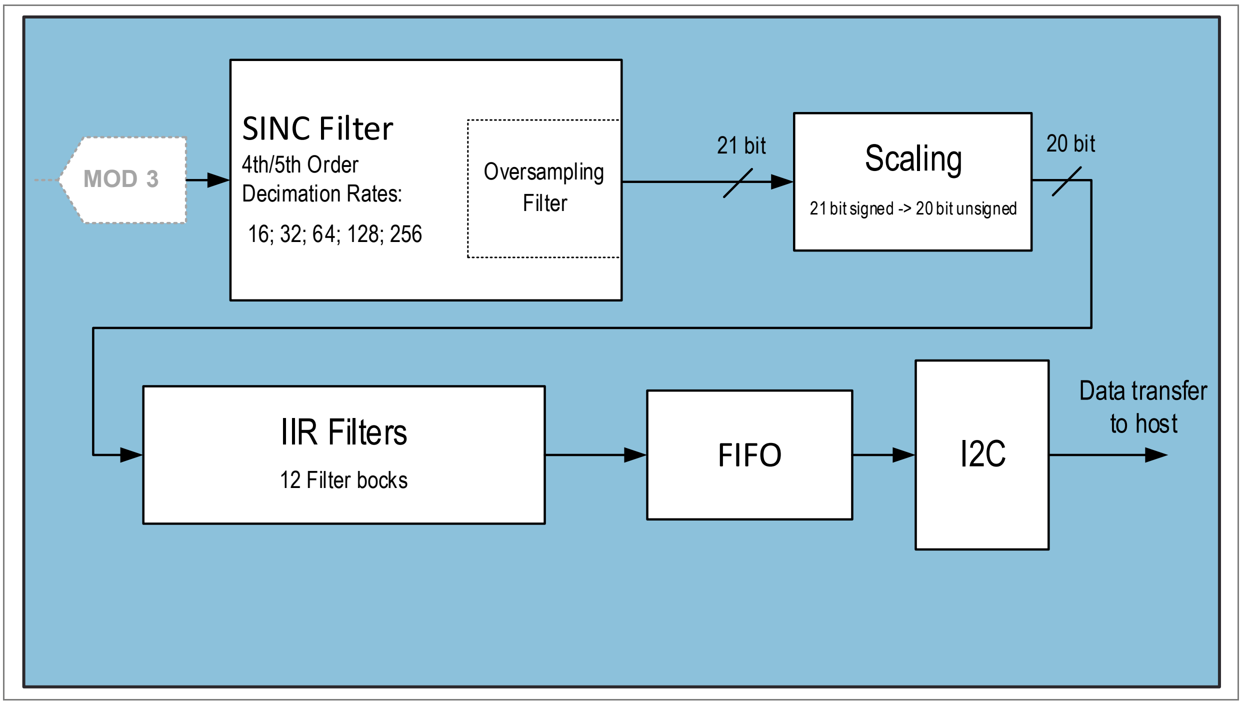
When GSR is activated, the excitation frequency is half of the ECG sample frequency chosen in a square waveform, and the current can be controlled from 200 nA to 85 µA. These settings can be chosen in **BIOZ_EXCIT**. The settings will only be applied when **GSR_EN** bit is set to one. The dynamic range that can be achieved is between 300 nS to 100 µS with 1 nS step size.

7.7.3 ECG/BioZ signal processing overview

Similar to the PPG signal processing the ECG and BioZ data acquisition path supports also various signal processing options. An overview of all options and a device signal flow is shown in Figure 45.

The output of ADC modulator 3 is connected to the SINC filter block which acts as down sampling filter. It is possible to select between 4th and 5th filter order via register **ECG1_SEL_ORDER** and **ECG2_SEL_ORDER** as well as decimation rates between 16, 32, 64, 128 and 256 via register **ECG1_SINC_DEC** and **ECG2_SINC_DEC**. In order to further improve SNR of the system there is an oversampling filter function, which is part of the down sampling filter that can be enabled via register **ECG1_SINC_OVS** and **ECG2_SINC_OVS**. The three-bit register allows for 7 different oversampling filter ratios to be enabled from factor 2 up to 128. The oversampling filter function is disabled in default configuration. Please mind that by enabling the oversampling filter function the active ADC modulator time is increased influencing power consumption with the benefit of better noise behavior. Once the signal passed the SINC decimation and optional oversampling filter the ECG/BioZ signal is feed into a scaling block which converts the signal into 20-bit unsigned signal. The on-chip IIR filter block is the last processing block which can be enabled to implement post processing filter characteristics before the data is written to the FIFO memory. Please refer to chapter 7.8 for more detail information regarding the IIR filter block.

Figure 45: ECG/BioZ signal processing overview



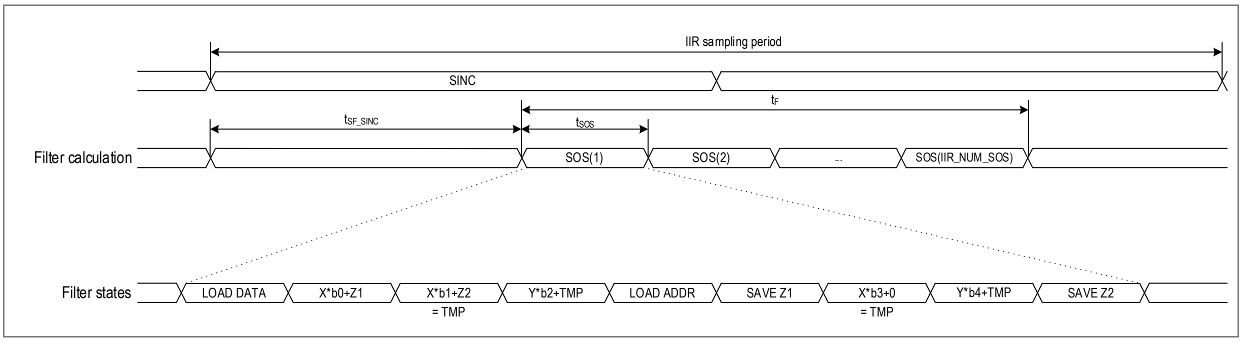
7.8 IIR filter

An IIR filter with the parameters shown below in Table 11 is used to realize the notch filter functionality. It is possible to implement other filters by reprogramming the filter coefficients and using two’s complement for math operations. The clock frequency should be 10 MHz.

Table 11: IIR filter parameters

IIR filter parameter	Value
MAX_NUM_OF_SOS	12
SAMPLE_BIT_WIDTH	21
COEFF_BIT_WIDTH	16
SCALE_SHIFT	14
RAM_WIDTH	8

Figure 46: IIR filter timing diagram



Equation 3:

$$t_{SF\_ECG} = t_{SD\_ECG} + t_{DV\_ECG} + t_{OS\_ECG}$$

Equation 4:

$$t_{SOS\_ECG} = t_{MODCLK} * 51$$

Equation 5:

$$t_{F\_ECG} = \mathrm{IIR\_NUM\_SOS} * t_{SOS\_ECG}$$

Figure 47: Memory map of filter parameters and data for ECG

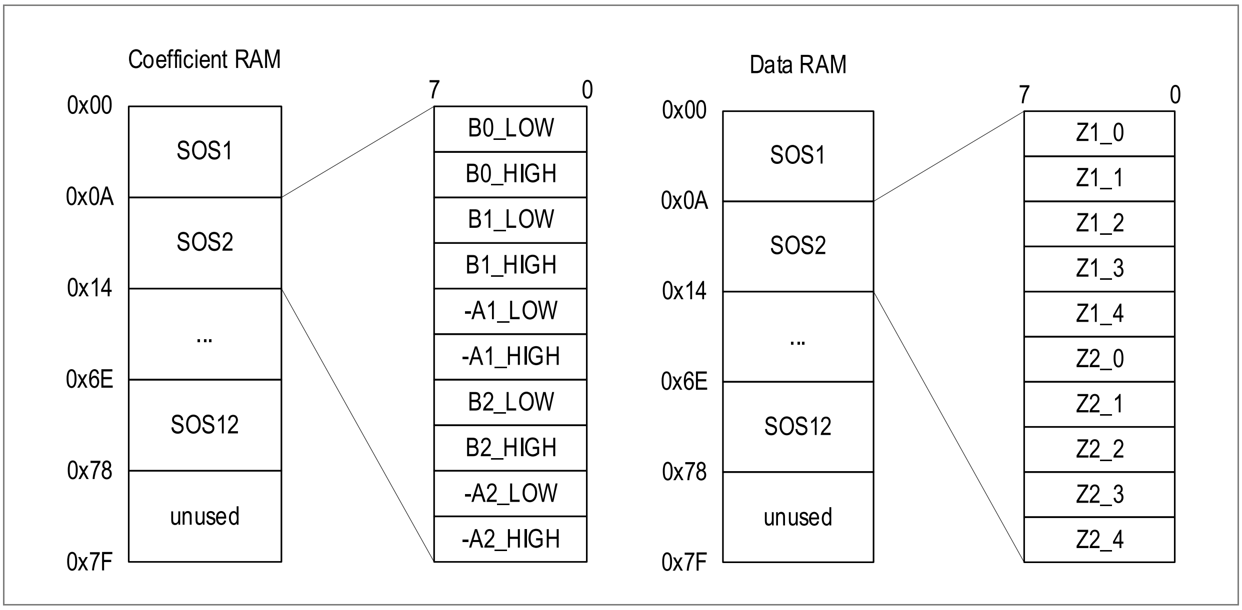
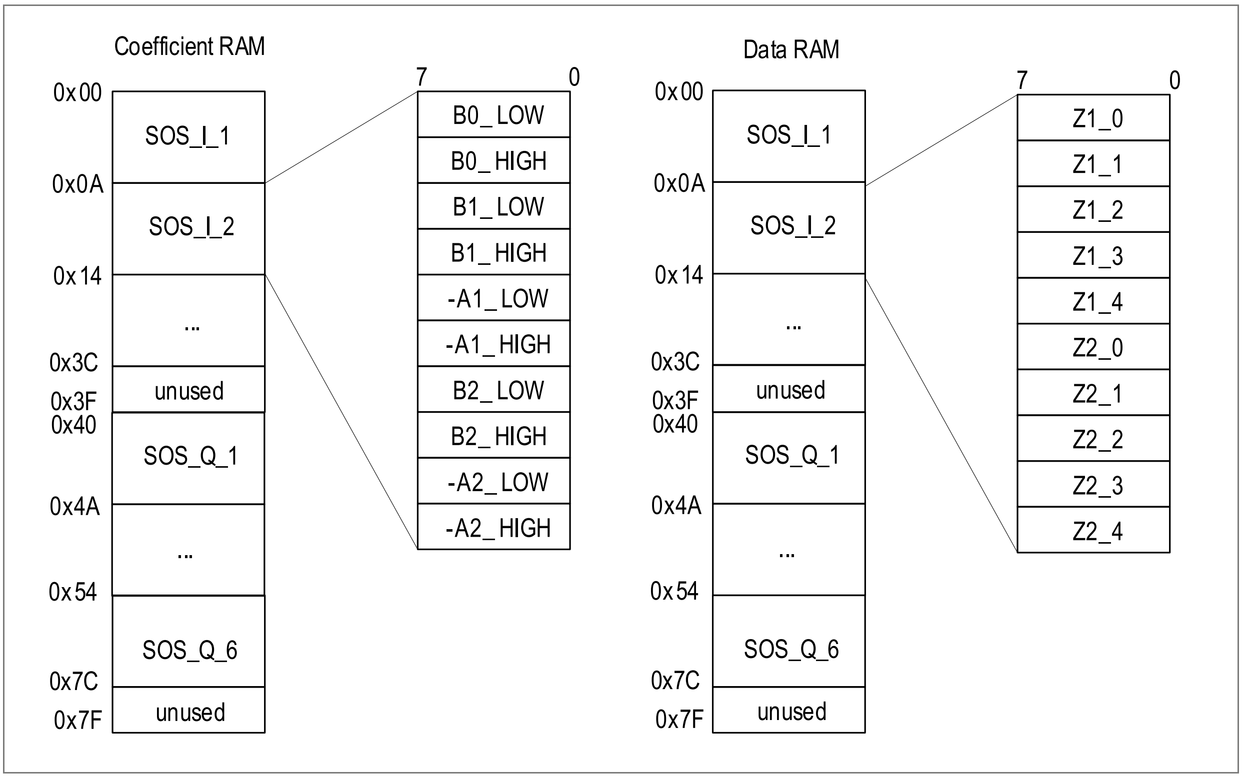


Figure 48: Memory map of filter parameters and data for BIOZ



7.9 FIFO description

The AS7058 contains a 1.5 kB FIFO register for buffering the measurement data output to an external microcontroller via the I²C or SPI interface. The FIFO buffering allows the external MCU to stay in idle mode during energy-saving measurements.

The measurement data of the three channels and possible status information from the AAOC will be collected in a common data stream and written to the FIFO. The coding of the data stream is described below in Figure 49.

Figure 49: FIFO data format

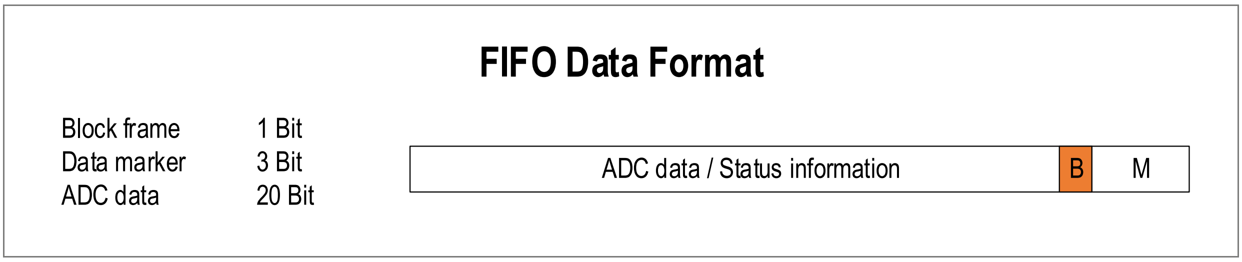
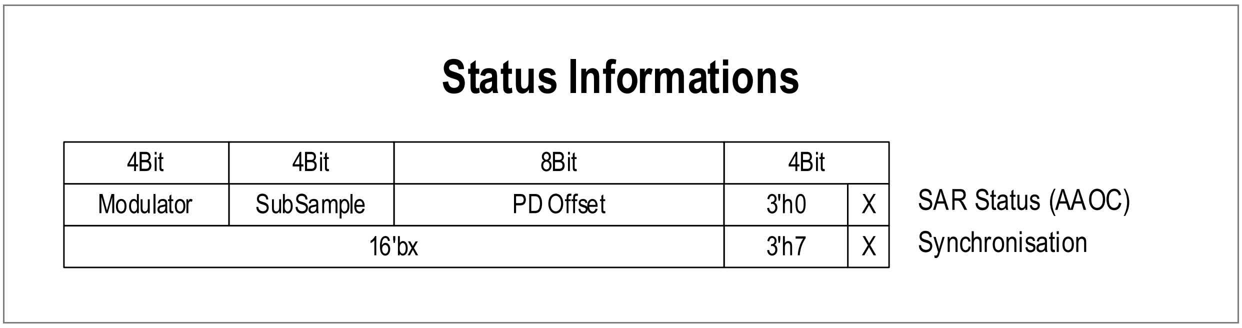


Table 12: FIFO data marker bit description

Data marker bits <2:0>	Description
‘b’000	First ADC value of modulator 1 (PPG1)
‘b’001	Other ADC value of modulator 1 (PPG1)
‘b’010	First ADC value of modulator 2 (PPG2)
‘b’011	Other ADC value of modulator 2 (PPG2)
‘b’100	ADC data sequence 1/Sub 1 MOD3 (ECG)
‘b’101	ADC data sequence 1/Sub 2 MOD3 (ECG)
‘b’110	ADC data sequence 2 ECG channel
‘b’111	Status information

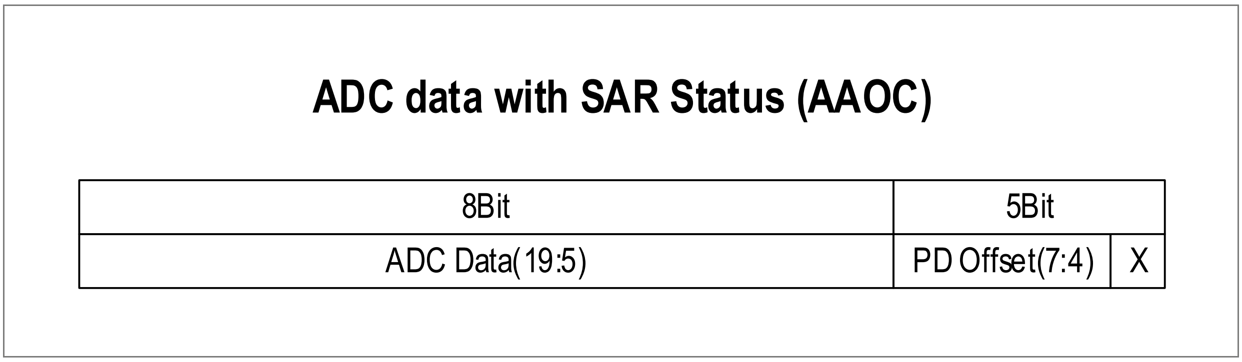
Figure 50: Status information



Status Informations

4Bit	4Bit	8Bit	4Bit		
Modulator	SubSample	PD Offset	3'h0	X	SAR Status (AAOC)
16'bx			3'h7	X	Synchronisation

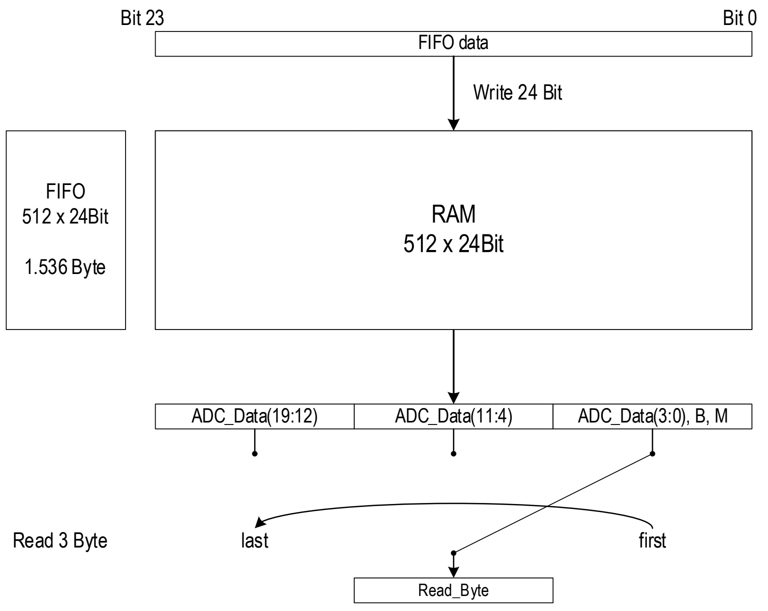
Figure 51: AAOC status information



ADC data with SAR Status (AAOC)

8Bit	5Bit	
ADC Data(19:5)	PD Offset(7:4)	X

Figure 52: FIFO data structure and organization



FIFO RAM Structure

RAM block	Number of RAMs	Number N	FIFO size
128 x 8 Bit	12	512	1.536 Byte

7.10 Communication interfaces

7.10.1 Interrupt

The interrupt manager processes the interrupt events. These interrupt events must be released for processing via an interrupt enable register **IRQ_ENABLE**. The dedicated interrupt status bit is automatically reset when the corresponding sub-status register is read (auto-zero register). For the FIFO threshold reset, the FIFO must be read or cleared. In this way, no interrupt events may be lost.

7.10.2 GPIO

The GPIO pin can be used as an input or output. In default configuration the GPIO pin is configured as an input. Since the internal pull up/down resistors are disabled it is recommended to connect an external pull up or pull down resistor to define the logic input level of the pin. Alternatively, it is also possible to enable the internal pull up or pull down resistors via register **GPIO_PU** or **GPIO_PD** to avoid an external resistor as part of the initialization routine of AS7058. The logic input level can be read back via register **GPIO_IN** register. Once the GPIO pin is configured as an output via **GPIO_OEN** register there are various internal status signals which can be routed to the GPIO pin. The register **GPIO_PINMAP_SEL** in its default configuration configures the pin as normal output pin whose output signal level can be controlled via **GPIO_OUT** register. However, if the register is reconfigured it is also possible to indicate if the LEDs are enabled or if standby mode is active. Please mind that when the GPIO pin is configured as an output the **GPIO_IN** register is always set to one independent of the actual output signal level.

7.10.3 I²C/SPI interface

The AS7058 supports I²C and SPI as host communication and control interfaces. In both operation modes (I²C or SPI), AS7058 works as a slave device. The interface selection is handled via the CSXN pin during startup of the device. In case AS7058 is supposed to work in I²C operation mode it is mandatory to pull the CSXN pin high with an external pull up resistor. In case SPI operation mode should be used the CSXN pin has to be connected to the chip select pin of the SPI master device.

7.10.3.1 I²C interface

The AS7058 I²C slave uses an I²C address of 0x55 (7-bit format; R/W bit has to be added) - AAh (8-bit format for writing) and ABh (8-bit format for reading) respectively. It expects external pull-up resistors on the SDA_MOSI and SCL pins. Furthermore, it is mandatory to connect and external pull up resistors to CSXN pin for I²C interface selection. The interface supports the following features:

- Fast mode plus (1 MHz)
- Fast Mode (400 kHz)
- Standard Mode (100 kHz)
- 7+1-bit addressing mode
- Write formats
  - Single-Byte-Write
  - Burst-Write
- Read formats
  - Current-Address-Read
  - Random-Read
  - Sequential-Read.
- IEEE standard requirements regarding filtering and timing are implemented.

7.10.3.2 I²C protocol

The Table 13: I²C symbol definition table shows the symbols used in the coming mode descriptions.

Table 13: I²C symbol definition

Symbol	Definition	R/W	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start	R	1-bit
DW	Device address for write	R	1010 1010b (AAh)
DR	Device address for read	R	1010 1011b (ABh)
WA	Word address	R	8-bit
A	Acknowledge	W	1-bit
N	No acknowledge	R	1-bit
reg_data	Register data/write	R	8-bit
data (n)	Register data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Increment word address internally	R	During acknowledge

7.10.3.3 I²C write access

Byte Write and Burst Write formats are used to write data to the slave.

Figure 53: I²C byte write format

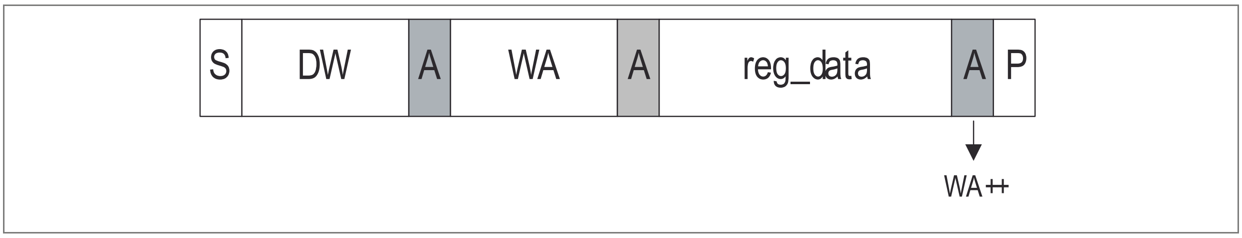
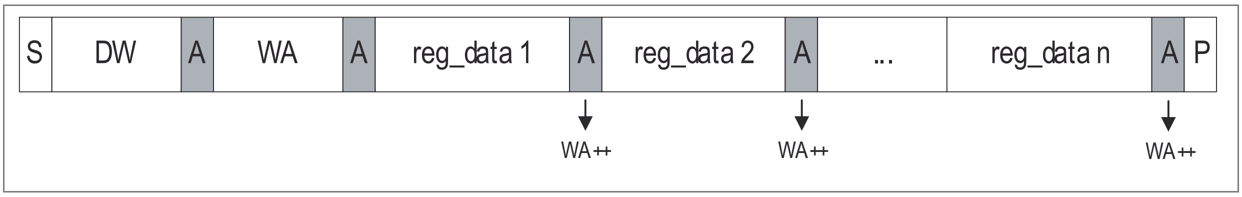


Figure 54: I²C burst write format

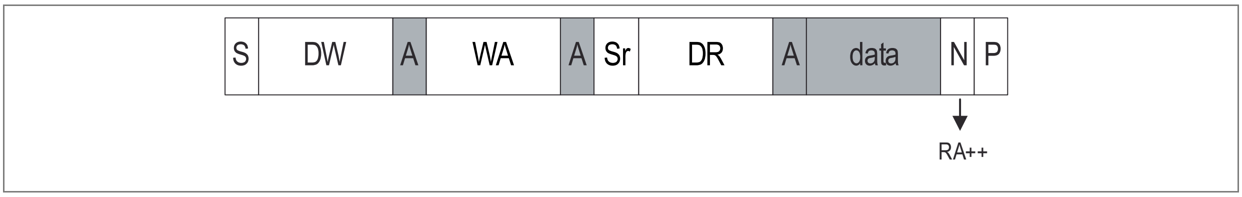


The transmission begins with the START condition, which is generated by the master when the bus is in an IDLE state (the bus is free). The device-write address is followed by the word address. After the word address, any number of data bytes can be sent to the slave. The word address is incremented internally to write subsequent data bytes on subsequent address locations.

7.10.3.4 I²C read

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address or with a new transmission START followed by the device-read address when the bus is in an IDLE state. The device-read address is always followed by the first register byte transmitted from the slave. In Read mode, any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 55: I²C random read format

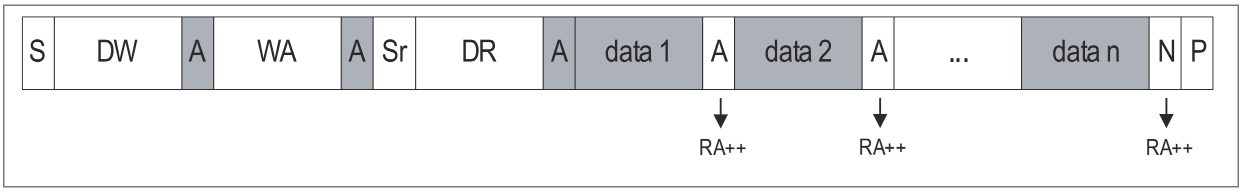


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

To change the data direction, a repeated START condition is issued on the first SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state, the slave transmits register data located by the previously received word address vector. The master responds to the data byte with a “not-acknowledge” and issues a STOP condition on the bus.

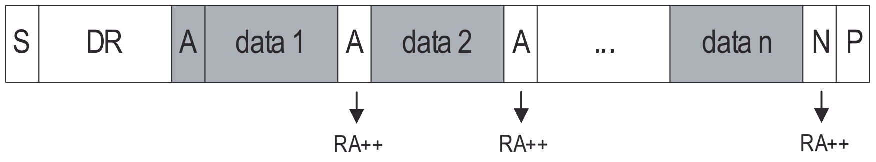
Figure 56: I²C sequential read format



Sequential Read is the extended form of Random Read, as more than one register-data byte is subsequently transferred. In contrast to the Random Read, an acknowledge from the master is the response for the transferred register-data bytes for a sequential read.

The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission, the master must send a “not-acknowledge” following the last data byte and subsequently generate the STOP condition.

Figure 57: I²C current address read format

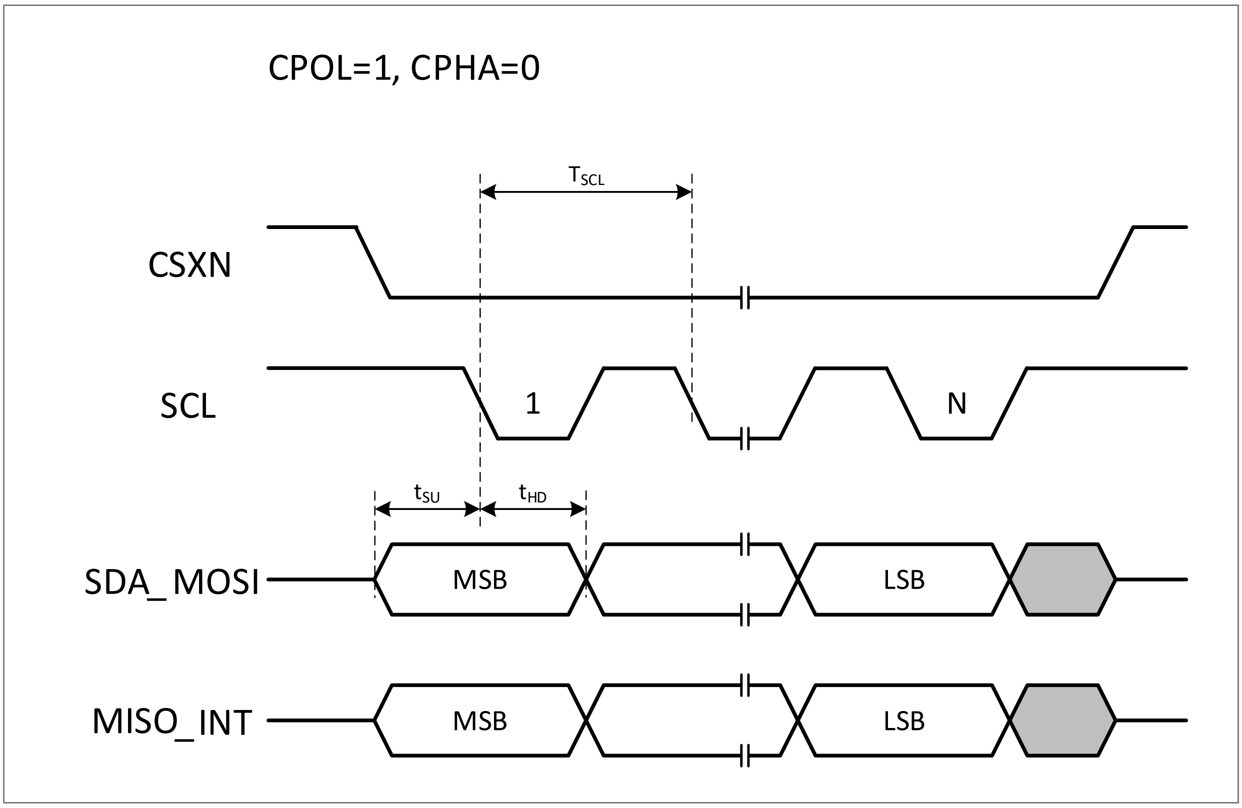


To keep the access time as small as possible, this format allows read access without the word address transfer in advance of the data transfer. The bus is idle, and the master issues a START condition, followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a “not-acknowledge” after the first register byte. Analogous to Sequential Read, an unlimited number of data bytes can be transferred – where an acknowledge from the master must be the response to the data bytes. For termination of the transmission, the master sends a “not-acknowledge” following the last data byte and a subsequent STOP condition.

7.10.3.5 SPI

SPI mode should be used: CPOL = 1, CPHA = 0 (see Figure 58).

Figure 58: SPI timing



SPI access protocols:

- Single Write RW=0, Address, Write Data Byte
- Single Read RW=1, Address, Read Data Byte
- Burst Read RW=1, Address, Read n Data Byte

Figure 59: SPI single access with address space of 256 Byte

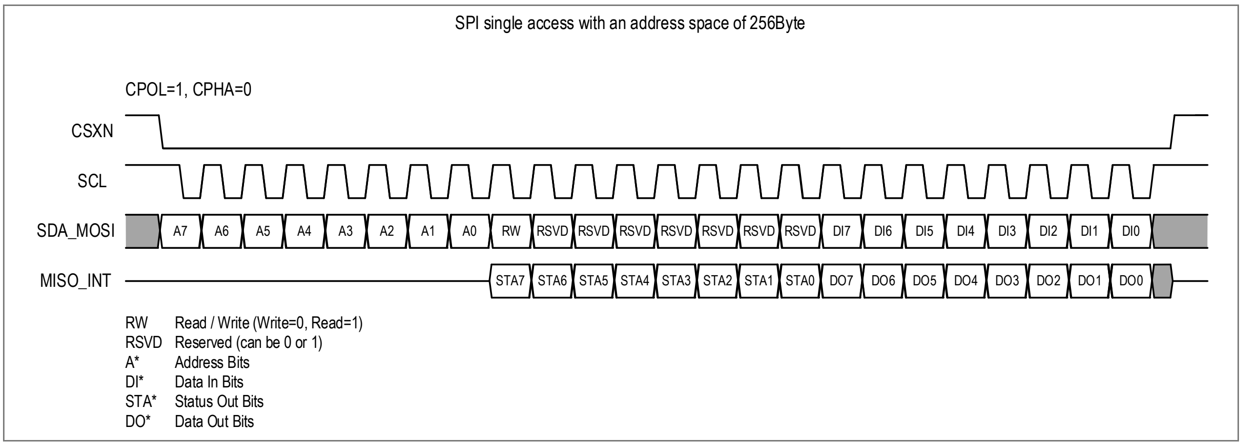
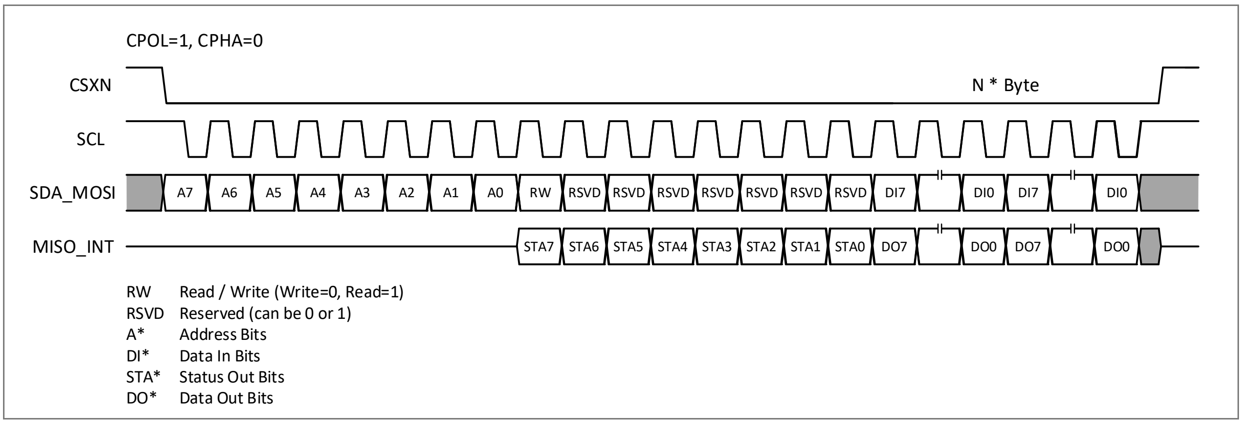


Figure 60: SPI burst access with address space of 256 Byte

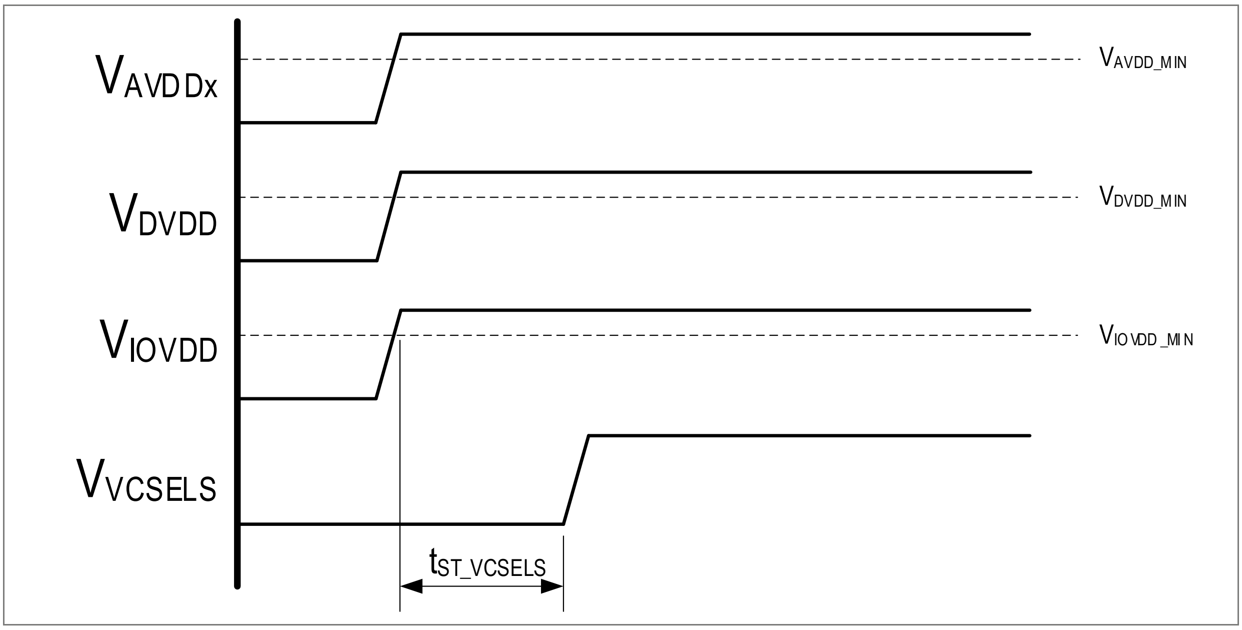


If a clock rate other than n*8 clocks is detected during data transmission in SPI mode, an error is displayed in the SPI status register.

7.11 Startup information

To guarantee proper startup of AS7058 it is recommended to follow a defined startup timing of the power supply reels. It is important that V_{VCSELS} supply voltage is delayed compared to V_{DVDD}, V_{AVDD} and V_{IOVDD} supply voltage like it is shown in Figure 61. However, if the suggested timing cannot be fulfilled and all supply voltages do start in parallel (t_{ST_VCSELS}=0 ms) this is supported with the drawback that the connected LEDs might light up for a short period of time during the very first startup of the device until all supplies are settled. If this behavior is acceptable, all supplies can start up in parallel.

Figure 61: AS7058 startup timing diagram



7.11.1 Parameter

Table 14: Startup timing parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ST_VCSELS}	Startup delay VLED supply voltage		0	1		ms

7.12 Standby mode

AS7058 supports standby operation mode to reduce overall power consumption during the pause times while no PPG or ECG measurement is ongoing. Especially at very low sample rates standby mode helps to reduce system power consumption to extend the battery lifetime of a device. The standby mode function is controlled with up to 14 different standby mode enable control signals. Each of the fourteen standby enable signals controls a dedicated hardware block of AS7058. An overview of the 14 different control signals is shown in Table 15 below. Furthermore, it contains information about the related blocks which are necessary for a certain application. If the device operates in PPG operation mode, only standby enable signals whose functionality is required for PPG operation need to be enabled via register **STANDBY_ON1** and **STANDBY_ON2**. In addition to the enable registers each Standby Enable signal is also connected to a dedicated timing register to define the standby startup timing of the functional block. A simplified timing diagram of all Standby Enable signals is shown in Figure 62.

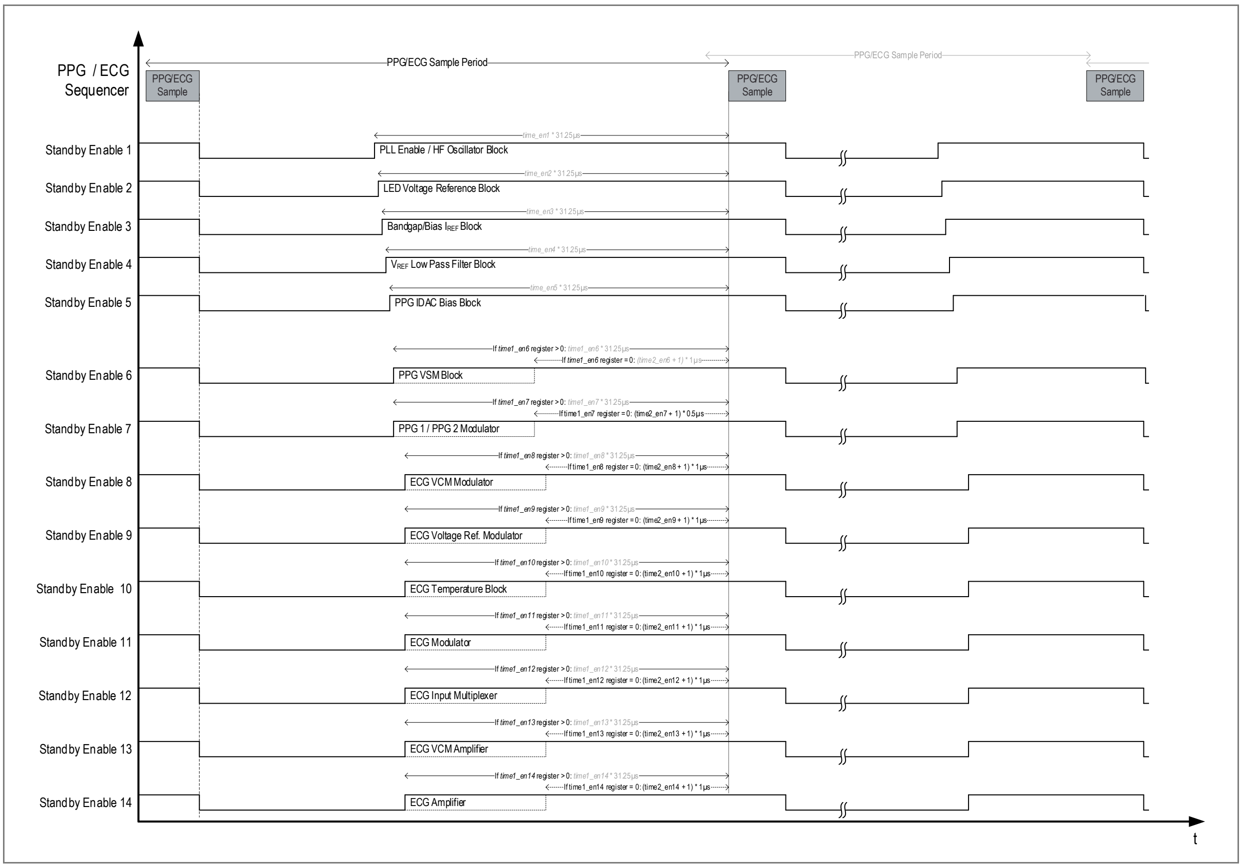
Table 15: Standby mode control signal overview

Standby control signal	Function	Timing control registers	Functionality
Standby Enable 1	Controls and enables the internal PLL and high frequency oscillator.	*time_en1*	Required for PPG and ECG operation
Standby Enable 2	Controls and enables the voltage reference for the LED drivers	*time_en2*	Required for PPG operation only
Standby Enable 3	Controls and enables on chip bandgap and bias reference current	*time_en3*	Required for PPG and ECG operation
Standby Enable 4	Controls and enables the bypass functions of the low pass filter	*time_en4*	Required for PPG and ECG operation
Standby Enable 5	Controls and enables the bias voltage block of the current DAC	*time_en5*	Required for PPG operation only
Standby Enable 6	Controls and enables the PPG common mode voltage buffer	*time1_en6* *time2_en6*	Required for PPG operation only
Standby Enable 7	Controls and enables the PPG modulators	*time1_en7* *time2_en7*	Required for PPG operation only
Standby Enable 8	Controls and enables the ECG common mode voltage buffer	*time1_en8* *time2_en8*	Required for ECG operation only
Standby Enable 9	Controls and enables the voltage reference for the ECG modulator	*time1_en9* *time2_en9*	Required for ECG operation only
Standby Enable 10	Controls and enables ECG temperature monitoring	*time1_en10* *time2_en10*	Required for ECG operation only
Standby Enable 11	Controls and enables the ECG modulator	*time1_en11* *time2_en11*	Required for ECG operation only
Standby Enable 12	Controls and enables the ECG input multiplexer	*time1_en12* *time2_en12*	Required for ECG operation only

Standby control signal	Function	Timing control registers	Functionality
Standby Enable 13	Controls and enables common mode voltage of ECG amplifier	*time1_en13* *time2_en13*	Required for ECG operation only
Standby Enable 14	Controls and enables ECG amplifiers	*time1_en14* *time2_en14*	Required for ECG operation only

The timings which are defined in the timing registers for each control signal define the start of a block prior to the actual measurement start. The timing registers allow for exact control of the startup timing behavior of all relevant blocks and it makes sure that all system blocks are active and properly settled when a measurement is started. Right after the measurement is finished and the measurement data is written to the FIFO memory of AS7058 all Standby Enable signals are disabled again and the connected blocks are powered down. Important to mention is that Standby Enable 1 – Standby Enable 5 signals do have only one timing control register (*time_enX*). Each register is linked to the 32 kHz clock domain of the device which results into a 31.25 µs multiplication factor for these registers like it is also indicated in Figure 62. The Standby Enable 6 – Standby Enable 14 control signals have two timing control registers. The *time1_enX* timing registers are also linked to the 32 kHz clock domain of the device which results into a 31.25 µs multiplication factor for these registers. The second timing control register *time2_enX* which is also linked to each of the Standby Enable 6 – Standby Enable 14 registers is connected to the 2 MHz clock domain of AS7058 which results in a 1 µs multiplication factor for these registers. Only one of the two-timing registers for a Standby Enable signal can be active at a time and the priority is controlled with the register content. In case a value greater than zero is written to *time1_enX* register the register content of time2_enX register is ignored and the timing is calculated and executed based on the register content of time1_enX register. In case the *time1_enX* register is set to zero, the content of register *time2_enX* is used for the Standby Enable signal timing based on the 1 µs clock domain.

Figure 62: Standby enable signal timing diagram



8 Register description

8.1 Register overview

Table 16: Register overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
OTP									
0x0e	**P2RAM_OTP_14**	*bioz_ref_res[7:0]*							
0x0f	**P2RAM_OTP_15**							*bioz_ref_res[9:8]*	
0x13	**P2RAM_OTP_19**	*gsr_ref_res[7:0]*							
0x14	**P2RAM_OTP_20**							*gsr_ref_res[9:8]*	
0x15	**P2RAM_OTP_21**	*temp_adc_ref[7:0]*							
0x16	**P2RAM_OTP_22**	*temp_adc_ref[15:8]*							
POWER									
0x18	**CLK_CFG**			*sel_extclk*			*pll_on*	*hf_osc_on*	*lf_osc_on*
0x19	**REF_CFG1**			*sel_vcm*	*en_bg*	*en_vcm_ppg*	*en_vr_led*	*en_bias_iref*	*en_bias_ppg_idac*
0x1a	**REF_CFG2**				*en_vtemp*	*en_ref_ecgmod*	*en_vcm_ecgamp*	*en_vcm_ecgmod*	*byp_ref_lp*
0x1b	**REF_CFG3**	*sel_vcm_ecg*		*sel_vcm_ecgamp*		*sel_vcm_ppg*		*sel_vcm_ppg_sw*	
0x1c	**STANDBY_ON1**	*stby_en_on[7:0]*							
0x1d	**STANDBY_ON2**			*stby_en_on[13:8]*					
0x1e	**STANDBY_EN1**	*stby_en1_time*							
0x1f	**STANDBY_EN2**	*stby_en2_time*							
0x20	**STANDBY_EN3**	*stby_en3_time*							
0x21	**STANDBY_EN4**	*stby_en4_time*							
0x22	**STANDBY_EN5**	*stby_en5_time*							
0x23	**STANDBY_EN6**	*stby_en6_time1*			*stby_en6_time2*				
0x24	**STANDBY_EN7**	*stby_en7_time1*			*stby_en7_time2*				
0x25	**STANDBY_EN8**	*stby_en8_time1*			*stby_en8_time2*				
0x26	**STANDBY_EN9**	*stby_en9_time1*			*stby_en9_time2*				
0x27	**STANDBY_EN10**	*stby_en10_time*							
0x28	**STANDBY_EN11**	*stby_en11_time1*			*stby_en11_time2*				
0x29	**STANDBY_EN12**	*stby_en12_time1*			*stby_en12_time2*				
0x2a	**STANDBY_EN13**	*stby_en13_time1*			*stby_en13_time2*				
0x2b	**STANDBY_EN14**	*stby_en14_time1*			*stby_en14_time2*				
0x2d	**PWR_ON**				*pwr_on*				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x2e	**PWR_ISO**				*pwr_iso*				
0x2f	**PWR_STAT**				*pwr_stat*				
CONTROL									
0x31	**I2C_MODE**								*i2c_fm_plus*
0x32	**INT_CFG**			*int_inv*	*int_e2*	*int_e4*	*reserved*	*int_pu*	int_pd
0x33	**IF_CFG**	*sda_e2*	*sda_e4*	*reserved*	*miso_e2*	*miso_e4*	*reserved*	*csxn_pu*	csxn_pd
0x34	**GPIO_CFG1**	*gpio_inv*	*gpio_oen*	*reserved*	*gpio_e2*	*gpio_e4*	*reserved*	*gpio_pu*	gpio_pd
0x35	**GPIO_CFG2**						*gpio_pinmap_sel*		
0x36	**IO_CFG**							*extclk_pu*	*extclk_pd*
PPG MOD									
0x37	**PPGMOD_CFG1**							*ppgmod_opamp_ibias*	
0x39	**PPGMOD_CFG3**				*ppgmod_reset_delay*			*ppgmod_clk*	
0x3a	**PPGMOD1_CFG1**	*ppgmod1_en*	*ppgmod1_ios_mux*	ppgmod1_dsm_ampl	*ppgmod1_cint*				
0x3b	**PPGMOD1_CFG2**	*ppgmod1_ios_dir*	*ppgmod1_ios_fs*			*ppgmod1_iref_scale*			
0x3c	**PPGMOD1_CFG3**	*ppgmod1_iref*							
0x3d	**PPGMOD2_CFG1**	*ppgmod2_en*	*ppgmod2_ios_mux*	*ppgmod2_dsm_ampl*	*ppgmod2_cint*				
0x3e	**PPGMOD2_CFG2**	*ppgmod2_ios_dir*	*ppgmod2_ios_fs*			ppgmod2_iref_scale			
0x3f	**PPGMOD2_CFG3**	*ppgmod2_iref*							
LED DRIVER									
0x40	**VCSEL_PASSWORD**								*vcsel_password*
0x41	**VCSEL_CFG**	*vcsel_wd_disable*	*vcsel_safety_disable*	*vcsel_vrsel*		*vcsel_short_vdd_wait*		*vcsel_short_vss_wait*	
0x42	**VCSEL_MODE**	*vcsel_mode*							
0x43	**LED_CFG**								*led_wd_disable*
0x44	**LED_DRV1**				*drv1_fast_tr*	*drv1_bias*			
0x45	**LED_DRV2**				*drv2_fast_tr*	*drv2_bias*			
0x46	**LED1_ICTRL**	*led1_ictrl*							
0x47	**LED2_ICTRL**	*led2_ictrl*							
0x48	**LED3_ICTRL**	*led3_ictrl*							
0x49	**LED4_ICTRL**	*led4_ictrl*							
0x4a	**LED5_ICTRL**	*led5_ictrl*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x4b	**LED6_ICTRL**	*led6_ictrl*							
0x4c	**LED7_ICTRL**	*led7_ictrl*							
0x4d	**LED8_ICTRL**	*led8_ictrl*							
0x4e	**LED_IRNG1**	*led4_irng*		*led3_irng*		*led2_irng*		*led1_irng*	
0x4f	**LED_IRNG2**	*led8_irng*		*led7_irng*		*led6_irng*		*led5_irng*	
0x50	**LED_SUB1**		*sub1_drv2_sel*				*sub1_drv1_sel*		
0x51	**LED_SUB2**		*sub2_drv2_sel*				*sub2_drv1_sel*		
0x52	**LED_SUB3**		*sub3_drv2_sel*				*sub3_drv1_sel*		
0x53	**LED_SUB4**		*sub4_drv2_sel*				*sub4_drv1_sel*		
0x54	**LED_SUB5**		*sub5_drv2_sel*				*sub5_drv1_sel*		
0x55	**LED_SUB6**		*sub6_drv2_sel*				*sub6_drv1_sel*		
0x56	**LED_SUB7**		*sub7_drv2_sel*				*sub7_drv1_sel*		
0x57	**LED_SUB8**		*sub8_drv2_sel*				*sub8_drv1_sel*		
0x58	**LOWVDS_WAIT**	*lowvds_wait*							
PHOTODIODES									
0x59	**PDSEL_CFG**								*pdref_sel*
0x5a	**PPG1_PDSEL1**	*ppg1_pdsel_sub1*							
0x5b	**PPG1_PDSEL2**	*ppg1_pdsel_sub2*							
0x5c	**PPG1_PDSEL3**	*ppg1_pdsel_sub3*							
0x5d	**PPG1_PDSEL4**	*ppg1_pdsel_sub4*							
0x5e	**PPG1_PDSEL5**	*ppg1_pdsel_sub5*							
0x5f	**PPG1_PDSEL6**	*ppg1_pdsel_sub6*							
0x60	**PPG1_PDSEL7**	*ppg1_pdsel_sub7*							
0x61	**PPG1_PDSEL8**	*ppg1_pdsel_sub8*							
0x62	**PPG2_PDSEL1**	*ppg2_pdsel_sub1*							
0x63	**PPG2_PDSEL2**	*ppg2_pdsel_sub2*							
0x64	**PPG2_PDSEL3**	*ppg2_pdsel_sub3*							
0x65	**PPG2_PDSEL4**	*ppg2_pdsel_sub4*							
0x66	**PPG2_PDSEL5**	*ppg2_pdsel_sub5*							
0x67	**PPG2_PDSEL6**	*ppg2_pdsel_sub6*							
0x68	**PPG2_PDSEL7**	*ppg2_pdsel_sub7*							
0x69	**PPG2_PDSEL8**	*ppg2_pdsel_sub8*							
0x6a	**PPG2_AFESEL1**	*ppg2_afesel_sub2*				*ppg2_afesel_sub1*			
0x6b	**PPG2_AFESEL2**	*ppg2_afesel_sub4*				*ppg2_afesel_sub3*			
0x6c	**PPG2_AFESEL3**	*ppg2_afesel_sub6*				*ppg2_afesel_sub5*			
0x6d	**PPG2_AFESEL4**	*ppg2_afesel_sub8*				*ppg2_afesel_sub7*			
0x6e	**PPG2_AFEEN**	*ppg2_afe_en*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
SINC FILTER									
0x6f	**PPG_SINC_CFGA**			*ppg_sinc_ovs*			*ppg_sinc_dec*		
0x70	**PPG_SINC_CFGB**		*ppg_os_delay*				*ppg_comb_dly_en*	*ppg_sel_order*	*ppg_filter_mode*
0x71	**PPG_SINC_CFGC**	*ppg_start_delay*							
0x72	**PPG_SINC_CFGD**	*ppg1_sinc_smd*				*ppg2_sinc_smd*			
0x73	**ECG1_SINC_CFGA**			*ecg1_sinc_ovs*			*ecg1_sinc_dec*		
0x74	**ECG1_SINC_CFGB**		*ecg1_os_delay*				*ecg1_comb_dly_en*	*ecg1_se_order*	*ecg1_filter_mode*
0x75	**ECG1_SINC_CFGC**	*ecg1_start_delay*							
0x76	**ECG2_SINC_CFGA**			*ecg2_sinc_ovs*			*ecg2_sinc_dec*		
0x77	**ECG2_SINC_CFGB**		*ecg2_os_delay*				*ecg2_comb_dly_en*	*ecg2_se_order*	*ecg2_filter_mode*
0x78	**ECG2_SINC_CFGC**	*ecg2_start_delay*							
0x79	**ECG_SINC_CFG**					*ecg_sinc_smd*			
PHOTODIODE OFFSET									
0x7a	**IOS_PPG1_SUB1**	*ios_ppg1_sub1*							
0x7b	**IOS_PPG1_SUB2**	*ios_ppg1_sub2*							
0x7c	**IOS_PPG1_SUB3**	*ios_ppg1_sub3*							
0x7d	**IOS_PPG1_SUB4**	*ios_ppg1_sub4*							
0x7e	**IOS_PPG1_SUB5**	*ios_ppg1_sub5*							
0x7f	**IOS_PPG1_SUB6**	*ios_ppg1_sub6*							
0x80	**IOS_PPG1_SUB7**	*ios_ppg1_sub7*							
0x81	**IOS_PPG1_SUB8**	*ios_ppg1_sub8*							
0x82	**IOS_PPG2_SUB1**	*ios_ppg2_sub1*							
0x83	**IOS_PPG2_SUB2**	*ios_ppg2_sub2*							
0x84	**IOS_PPG2_SUB3**	*ios_ppg2_sub3*							
0x85	**IOS_PPG2_SUB4**	*ios_ppg2_sub4*							
0x86	**IOS_PPG2_SUB5**	*ios_ppg2_sub5*							
0x87	**IOS_PPG2_SUB6**	*ios_ppg2_sub6*							
0x88	**IOS_PPG2_SUB7**	*ios_ppg2_sub7*							
0x89	**IOS_PPG2_SUB8**	*ios_ppg2_sub8*							
0x8a	**IOS_LEDOFF**	*ios_ledoff*							
0x8b	**IOS_CFG**								*dis_ledoff*
AAOC									
0x8c	**AOC_SAR_THRES**	*sar_thres*							
0x8d	**AOC_SAR_RANGE**				*sar_range_en*	*sar_range*			
0x8e	**AOC_SAR_PPG1**	*sar_ppg1_en*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0x8f	**AOC_SAR_PPG2**	*sar_ppg2_en*							
POST PROCESSING									
0x90	**PP_CFG**				*asat_on*	*asat_fil*			
0x91	**PPG1_PP1**	*ppg1_pp_sub4*		*ppg1_pp_sub3*		*ppg1_pp_sub2*		*ppg1_pp_sub1*	
0x92	**PPG1_PP2**	*ppg1_pp_sub8*		*ppg1_pp_sub7*		*ppg1_pp_sub6*		*ppg1_pp_sub5*	
0x93	**PPG2_PP1**	*ppg2_pp_sub4*		*ppg2_pp_sub3*		*ppg2_pp_sub2*		*ppg2_pp_sub1*	
0x94	**PPG2_PP2**	*ppg2_pp_sub8*		*ppg2_pp_sub7*		*ppg2_pp_sub6*		*ppg2_pp_sub5*	
0x95	**IRQ_ENABLE**	*irq_en_iir_overflow*	*irq_en_leadoff*	*irq_en_vcsel*	*irq_en_asat*	*irq_en_led_lowvds*	*irq_en_fifooverflow*	*irq_en_fifothreshold*	*irq_en_sequencer*
SEQUENCER									
0x96	**PPG_SUB_WAIT**	*sub_wait*							
0x97	**PPG_SAR_WAIT**	*sar_wait*							
0x98	**PPG_LED_INIT**	*led_init*							
0x99	**PPG_FREQL**	*ppg_freq[7:0]*							
0x9a	**PPG_FREQH**	*ppg_freq[15:8]*							
0x9b	**PPG1_SUB_EN**	*ppg1_sub_en*							
0x9c	**PPG2_SUB_EN**	*ppg2_sub_en*							
0x9d	**PPG_MODE1**				*ppg_mode_sub1*				
0x9e	**PPG_MODE2**				*ppg_mode_sub2*				
0x9f	**PPG_MODE3**				*ppg_mode_sub3*				
0xa0	**PPG_MODE4**				*ppg_mode_sub4*				
0xa1	**PPG_MODE5**				*ppg_mode_sub5*				
0xa2	**PPG_MODE6**				*ppg_mode_sub6*				
0xa3	**PPG_MODE7**				*ppg_mode_sub7*				
0xa4	**PPG_MODE8**				*ppg_mode_sub8*				
0xa5	**PPG_CFG**					ext_freq	moving_average_on	moving_average_val	
0xa6	**ECG_FREQL**	*ecg_freq[7:0]*							
0xa7	**ECG_FREQH**	*ecg_freq[15:8]*							
0xa8	**ECG1_FREQDIVL**	*ecg1_freqdiv[7:0]*							
0xa9	**ECG1_FREQDIVH**	*ecg1_freqdiv[15:8]*							
0xaa	**ECG2_FREQDIVL**	*ecg2_freqdiv[7:0]*							
0xab	**ECG2_FREQDIVH**	*ecg2_freqdiv[15:8]*							
0xac	**ECG_SUBS**						*ecg2_en*	ecg1_en	ecg1_subs
0xad	**LEADOFF_INITL**	*leadoff_init[7:0]*							
0xae	**LEADOFF_INITH**						*leadoff_init[10:8]*		
0xaf	**ECG_INITL**	*ecg_init[7:0]*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xb0	**ECG_INITH**						*ecg_init[10:8]*		
0xb1	**SAMPLE_NUM**	*sample_num*							
ECG/BIOZ									
0xb2	**BIOZ_CFG**							gsr_en	bioz_en
0xb3	**BIOZ_EXCIT**		*bioz_excit_curr*			*bioz_excit_freq_sel*			
0xb4	**BIOZ_MIXER**				*bioz_mix_phase*				
0xb5	**BIOZ_SELECT**		*bioz_meas_sel*			*bioz_inmux_sel*			
0xb6	**BIOZ_GAIN**								bioz_gain
0xb7	**ECGMOD_CFG1**					*ecgmod_en*	*ecgmod_gainh*	ecgmod_ibias_sel	
0xb8	**ECGMOD_CFG2**				*ecgmod_reset_delay*			ecgmod_clk	
0xb9	**ECGIMUX_CFG1**		*ecgmod_imux_en*	*ecgmod_imus_lpf_fc*					
0xba	**ECGIMUX_CFG2**	sub2_imux_gain	*sub2_imux_sel2*			*sub1_imux_gain*	*sub1_imux_sel2*		
0xbb	**ECGIMUX_CFG3**					*sub3_imux_gain*	*sub3_imux_sel2*		
0xbc	**ECGAMP_CFG1**		*ecgamp_en*	*ecgamp_ref_en*	*ecgamp_fast_startup*	*ecgamp_gm_high*	*ecgamp_leadoff_en*	ecgamp_leadoff_pol	
0xbd	**ECGAMP_CFG2**		*ecgamp_leadoff_curr*						
0xbe	**ECGAMP_CFG3**	reserved	*ecgamp_hp_en*	*ecgamp_hp_byp*	*ecgamp_hp_csel*		*ecgamp_hp_clk_freq*		
0xbf	**ECGAMP_CFG4**	*ecgamp_hp_clk_pw*							
0xc0	**ECGAMP_CFG5**	ecgamp_lp_en	*ecgamp_lp_byp*	*ecgamp_lp_clk_freq*		*ecgamp_ina1_en*	*ecgamp_rld_ccomp*	ecgamp_ina1_gain	
0xc1	**ECGAMP_CFG6**				*ecgamp_ina2_en*	*ecgamp_ina2_byp*	*ecgamp_ina2_gain*		
0xc2	**ECGAMP_CFG7**	ecgamp_chop1_en	*ecgamp_chop1_clk_freq*			*ecgamp_chop2_en*	*ecgamp_chop2_clk_freq*		
0xc3	**ECG_BIOZ**						*ecg_bioz_ovs*		
Lead-Off									
0xc4	**LEADOFF_CFG**			*leadoff_en*	*leadoff_edge*		*leadoff_ovs*		
0xc5	**LEADOFF_THRESL**	*leadoff_thres[7:0]*							
0xc6	**LEADOFF_THRESH**	*leadoff_thres[15:8]*							
IIR FILTER									
0xc7	**IIR_CFG**				*iir_enable*	*iir_num_sos*			
0xc8	**IIR_COEFF_ADDR**		*iir_coeff_addr*						
0xc9	**IIR_COEFF_DATA**	*iir_coeff_data*							
FIFO									
0xca	**FIFO_THRESHOLD**	*fifo_threshold[7:0]*							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0xcb	**FIFO_CTRL**	*fifo_clear*				*seq_sync_en*	*sinc_randext_en*	*sar_data_en*	*fifo_threshold[8]*
MISCELLANEOUS									
0xeb	**PRODUCT_ID**			*otp_part_id*					
0xec	**SILICON_ID**	*silicon_id*							
0xee	**GPIO_CTRL**							*gpio_in*	*gpio_out*
0xef	**CHIP_CTRL**							*wd_reset*	*chip_reset*
0xf0	**SEQ_START**								*start_seq*
0xf1	**STATUS_CGB**							*pll_lock*	*clk_pll_ok*
0xf2	**STATUS_SEQ**							*seq_end*	*seq_error*
0xf3	**STATUS_LED**	*led_lowvds*							
0xf4	**STATUS_ASATA**	*mod1_asat*				*mod2_asat*			
0xf5	**STATUS_ASATB**					*mod3_asat*			
0xf6	**STATUS_VCSEL**				*led_wd*	*vcsel_vss*	*vcsel_vdd*	*vcsel_wd*	
0xf7	**STATUS_VCSEL_VSS**	*vcsel_short_vss*							
0xf8	**STATUS_VCSEL_VDD**	*vcsel_short_vdd*							
0xf9	**STATUS_LEADOFF**						*leadoff*	*leadoff_on*	*leadoff_off*
0xfa	**STATUS**	*irq_iir_overflow*	*irq_leadoff*	*irq_vcsel*	*irq_asat*	*irq_led_lowvds*	*irq_fifooverflow*	*irq_fifothreshold*	*irq_sequencer*
0xfb	**FIFO_LEVEL0**	*fifo_level[7:0]*							
0xfc	**FIFO_LEVEL1**						*fifo_overflow*	*fifo_level[9:8]*	
0xfd	**FIFOL**	*fifol*							
0xfe	**FIFOM**	*fifom*							
0xff	**FIFOH**	*fifoh*							

8.2 OTP

The register tables store the percentage error of the internal resistors with the following structure:

- 1-bit for the sign.
- 5 bits for the integer number with 1% per code such that the range is ± 31%.
- 4 bits for the decimal number with 0.06% per code.

8.2.1 P2RAM_OTP_14 register (Address 0x0e)

Table 17: P2RAM_OTP_14 register

Addr: 0x0e		**P2RAM_OTP_14**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*bioz_ref_res[7:0]*	0	R	Bio-Z reference resistor error LSBs

8.2.2 P2RAM_OTP_15 register (Address 0x0f)

Table 18: P2RAM_OTP_15 register

Addr: 0x0f		**P2RAM_OTP_15**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1:0	*bioz_ref_res[9:8]*	0	R	Bio-Z reference resistor error MSBs

8.2.3 P2RAM_OTP_19 register (Address 0x13)

Table 19: P2RAM_OTP_19 register

Addr: 0x13		**P2RAM_OTP_19**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*gsr_ref_res[7:0]*	0	R	GSR reference resistor LSBs

8.2.4 P2RAM_OTP_20 register (Address 0x14)

Table 20: P2RAM_OTP_20 register

Addr: 0x14		**P2RAM_OTP_20**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1:0	*gsr_ref_res[9:8]*	0	R	GSR reference resistor MSBs

8.2.5 P2RAM_OTP_21 register (Address 0x15)

Table 21: P2RAM_OTP_21 register

Addr: 0x15		**P2RAM_OTP_21**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*temp_adc_ref[7:0]*	0	R	Temperature reference ADC LSBs

8.2.6 P2RAM_OTP_22 register (Address 0x16)

Table 22: P2RAM_OTP_22 register

Addr: 0x16		**P2RAM_OTP_22**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*temp_adc_ref[15:8]*	0	R	Temperature reference ADC MSBs

8.3 Power

8.3.1 CLK_CFG register (Address 0x18)

Table 23: CLK_CFG register

Addr: 0x18		**CLK_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:4	*sel_extclk*	0	RW	Selection of external clock 2 MHz or 4 MHz. 00: Internal HF_OSC (2 MHz) selected 10: External 2 MHz clock selected 11: External 4 MHz clock selected
2	*pll_on*	0	RW	Switching on the 20 MHz PLL. 0: Disable 1: Enable
1	*hf_osc_on*	0	RW	Switching on the 2 MHz Oscillator. The oscillator is the source for the 20 MHz PLL. 0: Disable 1: Enable
0	*lf_osc_on*	0	RW	Switching on the 32 kHz Oscillator. 0: Disable 1: Enable

8.3.2 REF_CFG1 register (Address 0x19)

Table 24: REF_CFG1 register

Addr: 0x19		**REF_CFG1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*sel_vcm*	0	RW	Selection of the common mode voltage. 0: VCM = 0.75 V 1: VCM =0.8 V
4	*en_bg*	0	RW	Enable the bandgap. 0: Power down 1: Enabled
3	*en_vcm_ppg*	0	RW	Enable the PPG common-mode voltage reference. 0: Power down 1: Enabled
2	*en_vr_led*	0	RW	Enable the LED driver voltage reference. 0: Power down 1: Enabled
1	*en_bias_iref*	0	RW	Enable the current reference source. 0: Power down 1: Enabled
0	*en_bias_ppg_idac*	0	RW	Enable IOS DAC and IREF DAC. 0: Disabled 1: Enabled

8.3.3 REF_CFG2 register (Address 0x1a)

Table 25: REF_CFG2 register

Addr: 0x1a		**REF_CFG2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*en_vtemp*	0	RW	Enable internal temperature sensor. 0: Power down 1: Enabled
3	*en_ref_ecgmod*	0	RW	Enable positive reference voltage for the ECG voltage modulator. 0: Power down 1: Enabled
2	*en_vcm_ecgamp*	0	RW	Enable VCM of the ECG common-mode voltage reference. 0: Disabled, 1: Enabled
1	*en_vcm_ecgmod*	0	RW	Enable the ECG common-mode voltage reference. 0: Power down 1: Enabled
0	*byp_ref_lp*	1	RW	The bypass of the low-pass filter for the Reference and VCM. 0: Not bypassed 1: Bypassed

8.3.4 REF_CFG3 register (Address 0x1b)

Table 26: REF_CFG3 register

Addr: 0x1b	**REF_CFG3**			
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*sel_vcm_ecg*	0	RW	Configuration bits for common mode voltage of ECG measurement signal path. Do not change register default register configuration.
5:4	*sel_vcm_ecgamp*	0	RW	Configuration bits for common mode voltage of ECG measurement signal path. Do not change register default register configuration.
3:2	*sel_vcm_ppg*	0	RW	Configuration bits for common mode voltage of PPG measurement signal path. Do not change register default register configuration.
1:0	*sel_vcm_ppg_sw*	0	RW	Configuration bits for common mode voltage of PPG measurement signal path. Do not change register default register configuration.

8.3.5 STANDBY_ON1 register (Address 0x1c)

Table 27: STANDBY_ON1 register

Addr: 0x1c	**STANDBY_ON1**			
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en_on[7:0]*	0	RW	Set specific Standby registers Enable. 0...7 – Enable 1...8

8.3.6 STANDBY_ON2 register (Address 0x1d)

Table 28: STANDBY_ON2 register

Addr: 0x1d	**STANDBY_ON2**			
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:0	*stby_en_on[13:8]*	0	RW	Set specific Standby register Enable 9...14 0...5 - Enable 9...14

8.3.7 STANDBY_EN1 register (Address 0x1e)

Table 29: STANDBY_EN1 register

Addr: 0x1e		**STANDBY_EN1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en1_time*	4	RW	Time for Enable 1: N * TCLK_32KHZ, N = 0...255

8.3.8 STANDBY_EN2 register (Address 0x1f)

Table 30: STANDBY_EN2 register

Addr: 0x1f		**STANDBY_EN2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en2_time*	1	RW	Time for Enable2: N * TCLK_32KHZ, N = 0...255

8.3.9 STANDBY_EN3 register (Address 0x20)

Table 31: STANDBY_EN3 register

Addr: 0x20		**STANDBY_EN3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en3_time*	3	RW	Time for Enable3: N * TCLK_32KHZ, N = 0...255

8.3.10 STANDBY_EN4 register (Address 0x21)

Table 32: STANDBY_EN4 register

Addr: 0x21		**STANDBY_EN4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en4_time*	0	RW	Time for Enable4: N * TCLK_32KHZ, N = 0...255

8.3.11 STANDBY_EN5 register (Address 0x22)

Table 33: STANDBY_EN5 register

Addr: 0x22		**STANDBY_EN5**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en5_time*	1	RW	Time for Enable5: N * TCLK_32KHZ, N = 0...255

8.3.12 STANDBY_EN6 register (Address 0x23)

Table 34: STANDBY_EN6 register

Addr: 0x23		**STANDBY_EN6**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en6_time1*	0	RW	Time1 for Enable6 0: time2_en6 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en6_time2*	16	RW	Time2 for Enable6: N * TCLK_2MHZ, N = 0...31

8.3.13 STANDBY_EN7 register (Address 0x24)

Table 35: STANDBY_EN7 register

Addr: 0x24		**STANDBY_EN7**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en7_time1*	0	RW	Time1 for Enable7 0: time2_en7 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en7_time2*	16	RW	Time2 for Enable7: N * TCLK_2MHZ, N = 0...31

8.3.14 STANDBY_EN8 register (Address 0x25)

Table 36: STANDBY_EN8 register

Addr: 0x25		**STANDBY_EN8**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en8_time1*	0	RW	Time1 for Enable8 0: time2_en8 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en8_time2*	16	RW	Time2 for Enable8: N * TCLK_2MHZ, N = 0...31

8.3.15 STANDBY_EN9 register (Address 0x26)

Table 37: STANDBY_EN9 register

Addr: 0x26		**STANDBY_EN9**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en9_time1*	0	RW	Time1 for Enable9 0: time2_en9 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en9_time2*	16	RW	Time2 for Enable9 N * TCLK_2MHZ, N = 0...31

8.3.16 STANDBY_EN10 register (Address 0x27)

Table 38: STANDBY_EN10 register

Addr: 0x27		**STANDBY_EN10**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*stby_en10_time*	1	RW	Time for Enable10: N * TCLK_32KHZ, N = 0...255

8.3.17 STANDBY_EN11 register (Address 0x28)

Table 39: STANDBY_EN11 register

Addr: 0x28		**STANDBY_EN11**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en11_time1*	0	RW	Time1 for Enable11 0: time2_en11 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en11_time2*	16	RW	Time2 for Enable11: N * TCLK_2MHZ, N = 0...31

8.3.18 STANDBY_EN12 register (Address 0x29)

Table 40: STANDBY_EN12 register

Addr: 0x29		**STANDBY_EN12**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en12_time1*	0	RW	Time1 for Enable12 0: time2_en12 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en12_time2*	16	RW	Time2 for Enable12: N * TCLK_2MHZ, N = 0...31

8.3.19 STANDBY_EN13 register (Address 0x2a)

Table 41: STANDBY_EN13 register

Addr: 0x2a		**STANDBY_EN13**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en13_time1*	0	RW	Time1 for Enable13 0: time2_en13 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en13_time2*	31	RW	Time2 for Enable13: N * TCLK_2MHZ, N = 0...31

8.3.20 STANDBY_EN14 register (Address 0x2b)

Table 42: STANDBY_EN14 register

Addr: 0x2b		**STANDBY_EN14**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:5	*stby_en14_time1*	0	RW	Time1 for Enable14 0: time2_en14 is active, Others: (N+1) * TCLK_32KHZ, N = 0...7
4:0	*stby_en14_time2*	31	RW	Time2 for Enable14: N * TCLK_2MHZ, N = 0...31

8.3.21 PWR_ON register (Address 0x2d)

Table 43: PWR_ON register

Addr: 0x2d		PWR_ON		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*pwr_on*	0	RW	Switching of ECG/BIOZ power domain 0: Disable 1: Enable
3		0	RW	Switching of MOD2 power domain 0: Disable 1: Enable
2		0	RW	Switching of MOD1 power domain 0: Disable 1: Enable
1		0	RW	Switching of CTRL power domain 0: Disable 1: Enable
0		1	RW	Switching of CONF (Configuration) power domain 0: Disable 1: Enable

8.3.22 PWR_ISO register (Address 0x2e)

Table 44: PWR_ISO register

Addr: 0x2e		PWR_ISO		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*pwr_iso*	0	RW	ECG/BIOZ power isolation register bit. It is important that this bit is inverted to the *pwr_on* register. 0: Disable 1: Enable
3		0	RW	PPG2 power isolation register bit. It is important that this bit is inverted to the *pwr_on* register. 0: Disable 1: Enable
2		0	RW	PPG1 power isolation register bit. It is important that this bit is inverted to the *pwr_on* register. 0: Disable 1: Enable
1		0	RW	CTRL power isolation register bit. It is important that this bit is inverted to the *pwr_on* register. 0: Disable 1: Enable
0		1	RW	CONF power isolation register bit. It is important that this bit is inverted to the *pwr_on* register. 0: Disable 1: Enable

8.3.23 PWR_STAT register (Address 0x2f)

Table 45: PWR_STAT register

Addr: 0x2f		PWR_STAT		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*pwr_stat*	0	RW	ECG/BIOZ
3		0	RW	PPG2
2		0	RW	PPG1
1		0	RW	CTRL
0		1	RW	CONF

8.4 Control

8.4.1 I2C_MODE register (Address 0x31)

Table 46: I2C_MODE register

Addr: 0x31		**I2C_MODE**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*i2c_fm_plus*	0	RW	This register bit enables I²C fast mode plus with 1 MHz I²C clock speed. This register must not be written during burst mode. Only single write is possible. 0: I²C Fast Mode Plus Disabled 1: I²C Fast Mode Plus Enabled

8.4.2 INT_CFG register (Address 0x32)

Table 47: INT_CFG register

Addr: 0x32		**INT_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*int_inv*	0	RW	Inverting interrupt.
4	*int_e2*	0	RW	Set the output driver strength high with 1.
3	*int_e4*	0	RW	Set the output driver strength high again with 1.
2	*reserved*	0	RW	Reserved system register. Do not change default register value.
1	*int_pu*	0	RW	PU = 1 -> pull-up at INT pin
0	*int_pd*	0	RW	PD = 1 -> pull-down at INT pin

8.4.3 IF_CFG register (Address 0x33)

Table 48: IF_CFG register

Addr: 0x33		**IF_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*sda_e2*	0	RW	Set the output driver strength high with 1.
6	*sda_e4*	1	RW	Set the output driver strength high again with 1.
5	*reserved*	0	RW	Reserved system register. Do not change default register value.
4	*miso_e2*	0	RW	Set the output driver strength high with 1.
3	*miso_e4*	1	RW	Set the output driver strength high again with 1.
2	*reserved*	0	RW	Reserved system register. Do not change default register value.
1	*csxn_pu*	0	RW	PU = 1 -> pull-up at CSXN pin
0	*csxn_pd*	0	RW	PD = 1 -> pull-down at CSXN pin

8.4.4 GPIO_CFG1 (Address 0x34)

Table 49: GPIO_CFG1 register

Addr: 0x34		**GPIO_CFG1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*gpio_inv*	0	RW	Inverting the Output of the GPIO.
6	*gpio_oen*	0	RW	Output Enable of the GPIO.
5	*reserved*	0	RW	Reserved system register. Do not change default register value.
4	*gpio_e2*	0	RW	Set the output driver strength high with 1.
3	*gpio_e4*	0	RW	Set the output driver strength high again with 1.
2	*reserved*	0	RW	Reserved system register. Do not change default register value.
1	*gpio_pu*	0	RW	PU = 1 -> pull-up at GPIO pin
0	*gpio_pd*	0	RW	PD = 1 -> pull-down at GPIO pin

8.4.5 GPIO_CFG2 (Address 0x35)

Table 50: GPIO_CFG2 register

Addr: 0x35		GPIO_CFG2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*gpio_pinmap_sel*	0	RW	Pinmap multiplexer for GPIO. If *gpio_oen* = 1, select the signal which is driven to the GPIO. 0: gpio_out 1: led_on 2: standby_en5 3: 0 Others: Reserved

8.4.6 IO_CFG (Address 0x36)

Table 51: IO_CFG register

Addr: 0x36		IO_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*extclk_pu*	0	RW	PU = 1 -> pull-up at EXTCLK_SYNC pin
0	*extclk_pd*	0	RW	PD = 1 -> pull-down at EXTCLK_SYNC pin

8.5 PPG MOD

8.5.1 PPGMOD_CFG1 (Address 0x37)

Table 52: PPGMOD_CFG1 register

Addr: 0x37		PPGMOD_CFG1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1:0	*ppgmod_opamp_ibias*	0	RW	This register changes the PPG OPAMP bias current scaling. **Please do not change this register.** 0: x1 current scaling factor 1: x1.25 current scaling factor 2: x0.5 current scaling factor 3: x0.75 current scaling factor

8.5.2 PPGMOD_CFG3 (Address 0x39)

Table 53: PPGMOD_CFG3 register

Addr: 0x39		PPGMOD_CFG3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppgmod_reset_delay*	0	RW	Reset Time for all PPG Modulators N * MOD_CLK 0: N = 4 1: N = 8 2: N = 16 3: N = 32 4: N = 64 5: N = 128 >5: N = 256
1:0	*ppgmod_clk*	0	RW	PPG Modulator clock frequency MOD_CLK Sequence1 and Sequence2 use the same Modulator frequency. 0: 10 MHz 1: 5 MHz 2: 2.5 MHz 3: 1.25 MHz

8.5.3 PPGMOD1_CFG1 (Address 0x3a)

Table 54: PPGMOD1_CFG1 register

Addr: 0x3a		PPGMOD1_CFG1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppgmod1_en*	0	RW	Enable Modulator1 0: Off 1: On
6	*ppgmod1_ios_mux*	0	RW	Multiplex IOS DAC2 to modulator 1 for the calibration. 0: IOS DAC to MOD1 1: IOS DAC to PPGMOD2 if mod1_ios_dir = 1
5	*ppgmod1_dsm_ampl*	0	RW	This bit enables the DSM integrator scaling function. Please do not write this register and keep it at its default value.
4:0	*ppgmod1_cint*	0	RW	This register controls the integrator capacitor value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of the PPG modulator. 0: 1 pF 1: 2 pF … … 30: 31 pF 31: 32 pF

8.5.4 PPGMOD1_CFG2 (Address 0x3b)

Table 55: PPGMOD1_CFG2 register

Addr: 0x3b		PPGMOD1_CFG2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppgmod1_ios_dir*	0	RW	Offset DAC current direction 0: PMOS (Ambient Light Cancellation) PD Current - PD Offset Current 1: NMOS (Special Mode) PD Current + PD Offset Current
6:4	*ppgmod1_ios_fs*	0	RW	Offset DAC Full-Scale Current 0: 1 µA 1: 2 µA 2: 4 µA 3: 8 µA 4: 16 µA 5: 32 µA 6: 64 µA 7: 128 µA
3:0	*ppgmod1_iref_scale*	0	RW	This is the current reference scale factor for modulator 1 photodiode offset DAC. Default reset value of the register is 0, however it is recommended to use 0.625 scale factor for measurements. 0: 0.125 1: 0.250 2: 0.375 3: 0.500 **4: 0.625** 5: 0.750 6: 0.875 7: 1.000 8-15: Do not use.

8.5.5 PPGMOD1_CFG3 (Address 0x3c)

Table 56: PPGMOD1_CFG3 register

Addr: 0x3c		**PPGMOD1_CFG3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppgmod1_iref*	0	RW	This register defines an internal current reference value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of PPG modulator. 0: 1 µA 1: 2 µA ... ... 63: 64 µA 64-255: Do not use

8.5.6 PPGMOD2_CFG1 (Address 0x3d)

Table 57: PPGMOD2_CFG1 register

Addr: 0x3d		**PPGMOD2_CFG1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppgmod2_en*	0	RW	Enable Modulator1 0: Off 1: On
6	*ppgmod2_ios_mux*	0	RW	Multiplex IOS DAC2 to modulator 1 for calibration. 0: IOS DAC to MOD1 1: IOS DAC to PPGMOD2 if mod1_ios_dir = 1
5	*ppgmod2_dsm_ampl*	0	RW	This bit enables the DSM integrator scaling function. Please do not write this register and keep it at its default value.
4:0	*ppgmod2_cint*	0	RW	This register controls the integrator capacitor value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of PPG modulator. 0: 1 pF 1: 2 pF … … 30: 31 pF 31: 32 pF

8.5.7 PPGMOD2_CFG2 (Address 0x3e)

Table 58: PPGMOD2_CFG2 register

Addr: 0x3e		PPGMOD2_CFG2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppgmod2_ios_dir*	0	RW	Offset DAC current direction 0: PMOS (Ambient Light Cancellation) PD Current - PD Offset Current 1: NMOS (Special Mode) PD Current + PD Offset Current
6:4	*ppgmod2_ios_fs*	0	RW	Offset DAC Full-Scale Current 0: 1 µA 1: 2 µA 2: 4 µA 3: 8 µA 4: 16 µA 5: 32 µA 6: 64 µA 7: 128 µA
3:0	*ppgmod2_iref_scale*	0	RW	This is the current reference scale factor for modulator 2 photodiode offset DAC. Default reset value of the register is 0, however it is recommended to use 0.625 scale factor for measurements. 0: 0.125 1: 0.250 2: 0.375 3: 0.500 **4: 0.625** 5: 0.750 6: 0.875 7: 1.000 8-15: Do not use.

8.5.8 PPGMOD2_CFG3 (Address 0x3f)

Table 59: PPGMOD2_CFG3 register

Addr: 0x3f		PPGMOD2_CFG3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppgmod2_iref*	0	RW	This register defines an internal current reference value. Please do not change register unless instructed by ams OSRAM support team. The ams OSRAM support team provides different configuration values depending on the selected full scale range of PPG modulator. 0: 1 µA 1: 2 µA ... ... 63: 64 µA 64-255: Do not use

8.6 LED driver

8.6.1 VCSEL_PASSWORD (Address 0x40)

Table 60: VCSEL_PASSWORD register

Addr: 0x40		VCSEL_PASSWORD		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*vcsel_password*	0	RO	Writing Value = 0x57 to this Register address sets the vcsel_password = 1'b1. Writing other Values to this Register address sets the vcsel_password = 1'b0. Only vcsel_password can be read.

8.6.2 VCSEL_CFG (Address 0x41)

Table 61: VCSEL_CFG register

Addr: 0x41		VCSEL_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*vcsel_wd_disable*	0	RW	Disable VCSEL Watchdog 0: Watchdog active 1: Watchdog inactive
6	*vcsel_safety_disable*	0	RW	Disable the safety control logic evaluation of the short to the VSS/VDD signals. 0: Safety logic active 1: Safety logic inactive
5:4	*vcsel_vrsel*	0	RW	Selection of the reference voltage for short to VDD comparators. 0: 50 mV 1: 100 mV 2: 150 mV 3: 200 mV
3:2	*vcsel_short_vdd_wait*	0	RW	The vcsel_t_short_vdd_wait defines the time between switching on Short detection and a valid result. All the VCSEL LEDs use the same time. 0: 2 µs 1: 4 µs 2: 8 µs 3: 12 µs
1:0	*vcsel_short_vss_wait*	0	RW	The vcsel_t_short_vss_wait defines the time between switching on Short detection and a valid result. All the VCSEL LEDs use the same time. 0: 2 µs 1: 4 µs 2: 7 µs 3: 10 µs

8.6.3 VCSEL_MODE (Address 0x42)

Table 62: VCSEL_MODE register

Addr: 0x42		**VCSEL_MODE**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*vcsel_mode*	255	RW	Setting mode for LED pin 8. 0: LED mode 1: VCSEL mode
6			RW	Setting mode for LED pin 7, explanation at bit 7.
5			RW	Setting mode for LED pin 6, explanation at bit 7.
4			RW	Setting mode for LED pin 5, explanation at bit 7.
3			RW	Setting mode for LED pin 4, explanation at bit 7.
2			RW	Setting mode for LED pin 3, explanation at bit 7.
1			RW	Setting mode for LED pin 2, explanation at bit 7.
0			RW	Setting mode for LED pin 1, explanation at bit 7.

8.6.4 LED_CFG (Address 0x43)

Table 63: LED_CFG register

Addr: 0x43		**LED_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*led_wd_disable*	0	RW	Disable the LED Watchdog 0: Watchdog active 1: Watchdog inactive

8.6.5 LED_DRV1 (Address 0x44)

Table 64: LED_DRV1 register

Addr: 0x44		**LED_DRV1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*drv1_fast_tr*	0	RW	Switching time of LED Driver 1 0: Normal switching 1: Fast switching
3:0	*drv1_bias*	0	RW	Bias current register for LED driver 1. Do not change default register setting.

8.6.6 LED_DRV2 (Address 0x45)

Table 65: LED_DRV2 register

Addr: 0x45		**LED_DRV2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*drv2_fast_tr*	0	RW	Switching time of LED Driver 2 0: Normal switching 1: Fast switching
3:0	*drv2_bias*	0	RW	Bias current register for LED driver 2. Do not change default register setting.

8.6.7 LED1_ICTRL (Address 0x46)

Table 66: LED1_ICTRL register

Addr: 0x46		**LED1_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led1_ictrl*	0	RW	LED output current control of driver 1 for pin LED1.

8.6.8 LED2_ICTRL (Address 0x47)

Table 67: LED2_ICTRL register

Addr: 0x47		**LED2_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led2_ictrl*	0	RW	LED output current control of driver 1 for pin LED2.

8.6.9 LED3_ICTRL (Address 0x48)

Table 68: LED3_ICTRL register

Addr: 0x48		**LED3_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led3_ictrl*	0	RW	LED output current control of driver 1 for pin LED3.

8.6.10 LED4_ICTRL (Address 0x49)

Table 69: LED4_ICTRL register

Addr: 0x49		**LED4_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led4_ictrl*	0	RW	LED output current control of driver 1 for pin LED4.

8.6.11 LED5_ICTRL (Address 0x4a)

Table 70: LED5_ICTRL register

Addr: 0x4a		**LED5_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led5_ictrl*	0	RW	LED output current control of driver 2 for pin LED5.

8.6.12 LED6_ICTRL (Address 0x4b)

Table 71: LED6_ICTRL register

Addr: 0x4b		**LED6_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led6_ictrl*	0	RW	LED output current control of driver 2 for pin LED6.

8.6.13 LED7_ICTRL (Address 0x4c)

Table 72: LED7_ICTRL register

Addr: 0x4c		**LED7_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led7_ictrl*	0	RW	LED output current control of driver 2 for pin LED7.

8.6.14 LED8_ICTRL (Address 0x4d)

Table 73: LED8_ICTRL register

Addr: 0x4d		**LED8_ICTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led8_ictrl*	0	RW	LED output current control of driver 2 for pin LED8.

8.6.15 LED_IRNG1 (Address 0x4e)

Table 74: LED_IRNG1 register

Addr: 0x4e		**LED_IRNG1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*led4_irng*	0	RW	LED output current range for pin LED4. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
5:4	*led3_irng*	0	RW	LED output current range for pin LED3. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
3:2	*led2_irng*	0	RW	LED output current range for pin LED2. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
1:0	*led1_irng*	0	RW	LED output current range for pin LED1. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA

8.6.16 LED_IRNG2 (Address 0x4f)

Table 75: LED_IRNG2 register

Addr: 0x4f		**LED_IRNG2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*led8_irng*	0	RW	LED output current range for pin LED8. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
5:4	*led7_irng*	0	RW	LED output current range for pin LED7. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
3:2	*led6_irng*	0	RW	LED output current range for pin LED6. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA
1:0	*led5_irng*	0	RW	LED output current range for pin LED5. 0: 25 mA 1: 150 mA 2: 225 mA 3: 300 mA

8.6.17 LED_SUB1 (Address 0x50)

Table 76: LED_SUB1 register

Addr: 0x50		**LED_SUB1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub1_drv2_sel*	0	RW	Select the LED used in subsample 1. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub1_drv1_sel*	0	RW	Select the LED used in subsample 1. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.18 LED_SUB2 (Address 0x51)

Table 77: LED_SUB2 register

Addr: 0x51		**LED_SUB2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub2_drv2_sel*	0	RW	Select the LED used in subsample 2. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub2_drv1_sel*	0	RW	Select the LED used in subsample 2. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.19 LED_SUB3 (Address 0x52)

Table 78: LED_SUB3 register

Addr: 0x52		LED_SUB3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub3_drv2_sel*	0	RW	Select the LED used in subsample 3. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub3_drv1_sel*	0	RW	Select the LED used in subsample 3. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.20 LED_SUB4 (Address 0x53)

Table 79: LED_SUB4 register

Addr: 0x53		**LED_SUB4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub4_drv2_sel*	0	RW	Select the LED used in subsample 4. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub4_drv1_sel*	0	RW	Select the LED used in subsample 4. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.21 LED_SUB5 (Address 0x54)

Table 80: LED_SUB5 register

Addr: 0x54		**LED_SUB5**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub5_drv2_sel*	0	RW	Select the LED used in subsample 5. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub5_drv1_sel*	0	RW	Select the LED used in subsample 5. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.22 LED_SUB6 (Address 0x55)

Table 81: LED_SUB6 register

Addr: 0x55		LED_SUB6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub6_drv2_sel*	0	RW	Select the LED used in subsample 6. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub6_drv1_sel*	0	RW	Select the LED used in subsample 6. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.23 LED_SUB7 (Address 0x56)

Table 82: LED_SUB7 register

Addr: 0x56		**LED_SUB7**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub7_drv2_sel*	0	RW	Select the LED used in subsample 7. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub7_drv1_sel*	0	RW	Select the LED used in subsample 7. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.24 LED_SUB8 (Address 0x57)

Table 83: LED_SUB8 register

Addr: 0x57		**LED_SUB8**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*sub8_drv2_sel*	0	RW	Select the LED used in subsample 8. Only one LED from LED5 to LED8 must be active. 0: No LED used 1: LED5 2: LED6 3: LED7 4-7: LED8
2:0	*sub8_drv1_sel*	0	RW	Select the LED used in subsample 8. Only one LED from LED1 to LED4 must be active. 0: No LED used 1: LED1 2: LED2 3: LED3 4-7: LED4

8.6.25 LOWVDS_WAIT (Address 0x58)

Table 84: LOWVDS_WAIT register

Addr: 0x58		**LOWVDS_WAIT**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*lowvds_wait*	0	RW	LOWVDS_WAIT defines the time between switching on an LED and the start of voltage monitoring. All the LEDs use the same time. Time = lowvds_wait * 1 µs

8.7 Photodiodes

8.7.1 PDSEL_CFG register (Address 0x59)

Table 85: PDSEL_CFG register

Addr: 0x59		**PDSEL_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*pdref_sel*	0	RW	Select the PDREF voltage. 0: PDREF connected to PPG common-mode voltage during measurement 1: Always connected to AGND

8.7.2 PPG1_PDSEL1 register (Address 0x5a)

Table 86: PPG1_PDSEL1 register

Addr: 0x5a		**PPG1_PDSEL1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub1*	0	RW	Selects PD8 for MOD1 in subsample 1. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 1, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 1, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 1, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 1, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 1, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 1, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 1, explanation at bit 7.

8.7.3 PPG1_PDSEL2 register (Address 0x5b)

Table 87: PPG1_PDSEL2 register

Addr: 0x5b		PPG1_PDSEL2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub2*	0	RW	Selects PD8 for MOD1 in subsample 2. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 2, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 2, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 2, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 2, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 2, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 2, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 2, explanation at bit 7.

8.7.4 PPG1_PDSEL3 register (Address 0x5c)

Table 88: PPG1_PDSEL3 register

Addr: 0x5c		PPG1_PDSEL3		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub3*	0	RW	Selects PD8 for MOD1 in subsample 3. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 3, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 3, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 3, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 3, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 3, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 3, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 3, explanation at bit 7.

8.7.5 PPG1_PDSEL4 register (Address 0x5d)

Table 89: PPG1_PDSEL4 register

Addr: 0x5d		**PPG1_PDSEL4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub4*	0	RW	Selects PD8 for MOD1 in subsample 4. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 4, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 4, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 4, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 4, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 4, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 4, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 4, explanation at bit 7.

8.7.6 PPG1_PDSEL5 register (Address 0x5e)

Table 90: PPG1_PDSEL5 register

Addr: 0x5e		**PPG1_PDSEL5**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub5*	0	RW	Selects PD8 for MOD1 in subsample 5. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 5, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 5, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 5, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 5, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 5, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 5, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 5, explanation at bit 7.

8.7.7 PPG1_PDSEL6 register (Address 0x5f)

Table 91: PPG1_PDSEL6 register

Addr: 0x5f		PPG1_PDSEL6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub6*	0	RW	Selects PD8 for MOD1 in subsample 6. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 6, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 6, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 6, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 6, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 6, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 6, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 6, explanation at bit 7.

8.7.8 PPG1_PDSEL7 register (Address 0x60)

Table 92: PPG1_PDSEL7 register

Addr: 0x60		PPG1_PDSEL7		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub7*	0	RW	Selects PD8 for MOD1 in subsample 7. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 7, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 7, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 7, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 7, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 7, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 7, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 7, explanation at bit 7.

8.7.9 PPG1_PDSEL8 register (Address 0x61)

Table 93: PPG1_PDSEL8 register

Addr: 0x61		PPG1_PDSEL8		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg1_pdsel_sub8*	0	RW	Selects PD8 for MOD1 in subsample 8. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD1 in subsample 8, explanation at bit 7.
5		0	RW	Selects PD6 for MOD1 in subsample 8, explanation at bit 7.
4		0	RW	Selects PD5 for MOD1 in subsample 8, explanation at bit 7.
3		0	RW	Selects PD4 for MOD1 in subsample 8, explanation at bit 7.
2		0	RW	Selects PD3 for MOD1 in subsample 8, explanation at bit 7.
1		0	RW	Selects PD2 for MOD1 in subsample 8, explanation at bit 7.
0		0	RW	Selects PD1 for MOD1 in subsample 8, explanation at bit 7.

8.7.10 PPG2_PDSEL1 register (Address 0x62)

Table 94: PPG2_PDSEL1 register

Addr: 0x62		PPG2_PDSEL1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub1*	0	RW	Selects PD8 For MOD2 In subsample 1. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 1, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 1, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 1, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 1, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 1, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 1, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 1, explanation at bit 7.

8.7.11 PPG2_PDSEL2 register (Address 0x63)

Table 95: PPG2_PDSEL2 register

Addr: 0x63		**PPG2_PDSEL2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub2*	0	RW	Selects PD8 for MOD2 in subsample 2. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 2, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 2, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 2, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 2, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 2, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 2, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 2, explanation at bit 7.

8.7.12 PPG2_PDSEL3 register (Address 0x64)

Table 96: PPG2_PDSEL3 register

Addr: 0x64		**PPG2_PDSEL3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub3*	0	RW	Selects PD8 for MOD2 in subsample 3. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 3, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 3, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 3, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 3, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 3, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 3, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 3, explanation at bit 7.

8.7.13 PPG2_PDSEL4 register (Address 0x65)

Table 97: PPG2_PDSEL4 register

Addr: 0x65		**PPG2_PDSEL4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub4*	0	RW	Selects PD8 for MOD2 in subsample 4. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 4, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 4, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 4, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 4, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 4, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 4, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 4, explanation at bit 7.

8.7.14 PPG2_PDSEL5 register (Address 0x66)

Table 98: PPG2_PDSEL5 register

Addr: 0x66		**PPG2_PDSEL5**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub5*	0	RW	Selects PD8 for MOD2 in subsample 5. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 5, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 5, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 5, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 5, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 5, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 5, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 5, explanation at bit 7.

8.7.15 PPG2_PDSEL6 register (Address 0x67)

Table 99: PPG2_PDSEL6 register

Addr: 0x67		PPG2_PDSEL6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub6*	0	RW	Selects PD8 for MOD2 in subsample 6. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 6, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 6, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 6, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 6, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 6, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 6, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 6, explanation at bit 7.

8.7.16 PPG2_PDSEL7 register (Address 0x68)

Table 100: PPG2_PDSEL7 register

Addr: 0x68		PPG2_PDSEL7		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub7*	0	RW	Selects PD8 for MOD2 in subsample 7. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 7, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 7, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 7, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 7, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 7, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 7, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 7, explanation at bit 7.

8.7.17 PPG2_PDSEL8 register (Address 0x69)

Table 101: PPG2_PDSEL8 register

Addr: 0x69		**PPG2_PDSEL8**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_pdsel_sub8*	0	RW	Selects PD8 for MOD2 in subsample 8. 0: Disabled 1: Enabled
6		0	RW	Selects PD7 for MOD2 in subsample 8, explanation at bit 7.
5		0	RW	Selects PD6 for MOD2 in subsample 8, explanation at bit 7.
4		0	RW	Selects PD5 for MOD2 in subsample 8, explanation at bit 7.
3		0	RW	Selects PD4 for MOD2 in subsample 8, explanation at bit 7.
2		0	RW	Selects PD3 for MOD2 in subsample 8, explanation at bit 7.
1		0	RW	Selects PD2 for MOD2 in subsample 8, explanation at bit 7.
0		0	RW	Selects PD1 for MOD2 in subsample 8, explanation at bit 7.

8.7.18 PPG2_AFESEL1 register (Address 0x6a)

Table 102: PPG2_AFESEL1 register

Addr: 0x6a		**PPG2_AFESEL1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*ppg2_afesel_sub2*	0	RW	Source for the AFE Input for MOD2 in subsample 2. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: VDDA 15: VSSA
3:0	*ppg2_afesel_sub1*	0	RW	Source for the AFE Input for MOD2 in subsample 1. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: VDDA 15: VSSA

8.7.19 PPG2_AFESEL2 register (Address 0x6b)

Table 103: PPG2_AFESEL2 register

Addr: 0x6b		**PPG2_AFESEL2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*ppg2_afesel_sub4*	0	RW	Source for the AFE Input for MOD2 in subsample 4. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: AGND 15: AGND
3:0	*ppg2_afesel_sub3*	0	RW	Source for the AFE Input for MOD2 in subsample 3. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: AGND 15: AGND

8.7.20 PPG2_AFESEL3 register (Address 0x6c)

Table 104: PPG2_AFESEL3 register

Addr: 0x6c		**PPG2_AFESEL3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*ppg2_afesel_sub6*	0	RW	Source for the AFE Input for MOD2 in subsample 6. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: AGND 15: AGND
3:0	*ppg2_afesel_sub5*	0	RW	Source for the AFE Input for MOD2 in subsample 5. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: AGND 15: AGND

8.7.21 PPG2_AFESEL4 register (Address 0x6d)

Table 105: PPG2_AFESEL4 register

Addr: 0x6d		PPG2_AFESEL4		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*ppg2_afesel_sub8*	0	RW	Source for the AFE Input for MOD2 in subsample 8. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: AGND 15: AGND
3:0	*ppg2_afesel_sub7*	0	RW	Source for the AFE Input for MOD2 in subsample 7. 0: PGND0 1: PGND1 2: LED1 3: LED2 4: LED3 5: LED4 6: LED5 7: LED6 8: LED7 9: LED8 10: PGND0 11: PGND1 12: VCSELA 13: VCSELS 14: AGND 15: AGND

8.7.22 PPG2_AFEEN register (Address 0x6e)

Table 106: PPG2_AFEEN register

Addr: 0x6e		**PPG2_AFEEN**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ppg2_afe_en*	0	RW	Select the AFE Input for MOD2 in subsample 8.
6		0	RW	Select the AFE Input for MOD2 in subsample 7.
5		0	RW	Select the AFE Input for MOD2 in subsample 6.
4		0	RW	Select the AFE Input for MOD2 in subsample 5.
3		0	RW	Select the AFE Input for MOD2 in subsample 4.
2		0	RW	Select the AFE Input for MOD2 in subsample 3.
1		0	RW	Select the AFE Input for MOD2 in subsample 2.
0		0	RW	Select the AFE Input for MOD2 in subsample 1.

8.8 SINC filter

8.8.1 PPG_SINC_CFGA register (Address 0x6f)

Table 107: PPG_SINC_CFGA register

Addr: 0x6f		**PPG_SINC_CFGA**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:3	*ppg_sinc_ovs*	0	RW	In this configuration, register an oversampling function of the data provided by the SINC filter can be enabled for signal enhancement of the PPG data channel. 0: SINC filter oversampling disabled 1: x2 oversampling enabled 2: x4 oversampling enabled 3: x8 oversampling enabled 4: x16 oversampling enabled 5: x32 oversampling enabled 6: x64 oversampling enabled 7: x128 oversampling enabled
2:0	*ppg_sinc_dec*	0	RW	Value for decimation. 0: 16 1: 32 2: 64 3: 128 4: 256

8.8.2 PPG_SINC_CFGB register (Address 0x70)

Table 108: PPG_SINC_CFGB register

Addr: 0x70		PPG_SINC_CFGB		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:3	*ppg_os_delay*	0	RW	The delay after which data is valid for the average calculation.
2	*ppg_comb_dly_en*	0	RW	Enables additional delay in COMB path. 0: Disable 1: Enable
1	*ppg_sel_order*	0	RW	Select the filter order. 0: 4 1: 5
0	*ppg_filter_mode*	0	RW	Select the mode of the filter. 0: Integrator mode (COI) 1: CIC filter mode

8.8.3 PPG_SINC_CFGC register (Address 0x71)

Table 109: PPG_SINC_CFGC register

Addr: 0x71		PPG_SINC_CFGC		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppg_start_delay*	0	RW	Delay to the Start of decimation N * MOD_CLK

8.8.4 PPG_SINC_CFGD register (Address 0x72)

Table 110: PPG_SINC_CFGD register

Addr: 0x72		**PPG_SINC_CFGD**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*ppg1_sinc_smd*	0	RW	Enlargement of the measured value of the PPG1 SINC filter. 0: + 50.00% 1: + 25.00% 2: + 12.50% 3: + 6.25%
3:0	*ppg2_sinc_smd*	0	RW	Enlargement of the measured value of the PPG2 SINC filter. 0: + 50.00% 1: + 25.00% 2: + 12.50% 3: + 6.25%

8.8.5 ECG1_SINC_CFGA register (Address 0x73)

Table 111: ECG1_SINC_CFGA register

Addr: 0x73		**ECG1_SINC_CFGA**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:3	*ecg1_sinc_ovs*	0	RW	In this configuration, register an oversampling function of the data provided by the SINC filter can be enabled for ECG signal enhancement. 0: SINC filter oversampling disabled 1: x2 oversampling enabled 2: x4 oversampling enabled 3: x8 oversampling enabled 4: x16 oversampling enabled 5: x32 oversampling enabled 6: x64 oversampling enabled 7: x128 oversampling enabled
2:0	*ecg1_sinc_dec*	0	RW	Value for decimation. 0: 16 1: 32 2: 64 3: 128 4: 256

8.8.6 ECG1_SINC_CFGB register (Address 0x74)

Table 112: ECG1_SINC_CFGB register

Addr: 0x74 **ECG1_SINC_CFGB**

Bit	Bit name	Default	Access	Bit description
6:3	*ecg1_os_delay*	0	RW	The delay after which data is valid for the average calculation.
2	*ecg1_comb_dly_en*	0	RW	Enables additional delay in COMB path stage 4. 0: Disable 1: Enable
1	*ecg1_sel_order*	0	RW	Select the filter order. 0: 4 1: 5
0	*ecg1_filter_mode*	1	RW	Select the mode of the filter. 0: Integrator mode (COI) 1: CIC filter mode

8.8.7 ECG1_SINC_CFGC register (Address 0x75)

Table 113: ECG1_SINC_CFGC register

Addr: 0x75 **ECG1_SINC_CFGC**

Bit	Bit name	Default	Access	Bit description
7:0	*ecg1_start_delay*	0	RW	Delay to the Start of decimation N * MOD_CLK

8.8.8 ECG2_SINC_CFGA register (Address 0x76)

Table 114: ECG2_SINC_CFGA register

Addr: 0x76		**ECG2_SINC_CFGA**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:3	*ecg2_sinc_ovs*	0	RW	In this configuration, register an oversampling function of the data provided by the SINC filter can be enabled for ECG signal enhancement. 0: SINC filter oversampling disabled 1: x2 oversampling enabled 2: x4 oversampling enabled 3: x8 oversampling enabled 4: x16 oversampling enabled 5: x32 oversampling enabled 6: x64 oversampling enabled 7: x128 oversampling enabled
2:0	*ecg2_sinc_dec*	0	RW	Value for decimation. 0: 16 1: 32 2: 64 3: 128 4: 256

8.8.9 ECG2_SINC_CFGB register (Address 0x77)

Table 115: ECG2_SINC_CFGB register

Addr: 0x77		**ECG2_SINC_CFGB**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:3	*ecg2_os_delay*	0	RW	The delay after which data is valid for the average calculation.
2	*ecg2_comb_dly_en*	0	RW	Enables additional delay in COMB path stage 4. 0: Disable 1: Enable
1	*ecg2_sel_order*	0	RW	Select the filter order. 0: 4 1: 5
0	*ecg2_filter_mode*	1	RW	Select the mode of the filter. 0: Integrator mode 1: CIC filter mode

8.8.10 ECG2_SINC_CFGC register (Address 0x78)

Table 116: ECG2_SINC_CFGC register

Addr: 0x78		**ECG2_SINC_CFGC**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg2_start_delay*	0	RW	Delay to the Start of decimation N * MOD_CLK

8.8.11 ECG_SINC_CFG register (Address 0x79)

Table 117: ECG_SINC_CFG register

Addr: 0x79		**ECG_SINC_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3:0	*ecg_sinc_smd*	0	RW	Enlargement of the measured value of the ECG SINC filter. 0: + 50.00% 1: + 25.00% 2: + 12.50% 3: + 6.25%

8.9 Photodiode offset

8.9.1 IOS_PPG1_SUB1 register (Address 0x7a)

Table 118: IOS_PPG1_SUB1 register

Addr: 0x7a		**IOS_PPG1_SUB1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg1_sub1*	0	RW	PD Offset Current for Modulator 1 in subsample 1.

8.9.2 IOS_PPG1_SUB2 register (Address 0x7b)

Table 119: IOS_PPG1_SUB2 register

Addr: 0x7b		**IOS_PPG1_SUB2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg1_sub2*	0	RW	PD Offset Current for Modulator 1 in subsample 2.

8.9.3 IOS_PPG1_SUB3 register (Address 0x7c)

Table 120: IOS_PPG1_SUB3 register

Addr: 0x7c **IOS_PPG1_SUB3**

Bit	Bit name	Default	Access	Bit description
7:0	*ios_ppg1_sub3*	0	RW	PD Offset Current for Modulator 1 in subsample 3.

8.9.4 IOS_PPG1_SUB4 register (Address 0x7d)

Table 121: IOS_PPG1_SUB4 register

Addr: 0x7d **IOS_PPG1_SUB4**

Bit	Bit name	Default	Access	Bit description
7:0	*ios_ppg1_sub4*	0	RW	PD Offset Current for Modulator 1 in subsample 4.

8.9.5 IOS_PPG1_SUB5 register (Address 0x7e)

Table 122: IOS_PPG1_SUB5 register

Addr: 0x7e **IOS_PPG1_SUB5**

Bit	Bit name	Default	Access	Bit description
7:0	*ios_ppg1_sub5*	0	RW	PD Offset Current for Modulator 1 in subsample 5.

8.9.6 IOS_PPG1_SUB6 register (Address 0x7f)

Table 123: IOS_PPG1_SUB6 register

Addr: 0x7f **IOS_PPG1_SUB6**

Bit	Bit name	Default	Access	Bit description
7:0	*ios_ppg1_sub6*	0	RW	PD Offset Current for Modulator 1 in subsample 6.

8.9.7 IOS_PPG1_SUB7 register (Address 0x80)

Table 124: IOS_PPG1_SUB7 register

Addr: 0x80		**IOS_PPG1_SUB7**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg1_sub7*	0	RW	PD Offset Current for Modulator 1 in subsample 7.

8.9.8 IOS_PPG1_SUB8 register (Address 0x81)

Table 125: IOS_PPG1_SUB8 register

Addr: 0x81		**IOS_PPG1_SUB8**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg1_sub8*	0	RW	PD Offset Current for Modulator 1 in subsample 8.

8.9.9 IOS_PPG2_SUB1 register (Address 0x82)

Table 126: IOS_PPG2_SUB1 register

Addr: 0x82		**IOS_PPG2_SUB1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub1*	0	RW	PD Offset Current for Modulator 2 in subsample 1.

8.9.10 IOS_PPG2_SUB2 register (Address 0x83)

Table 127: IOS_PPG2_SUB2 register

Addr: 0x83		**IOS_PPG2_SUB2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub2*	0	RW	PD Offset Current for Modulator 2 in subsample 2.

8.9.11 IOS_PPG2_SUB3 register (Address 0x84)

Table 128: IOS_PPG2_SUB3 register

Addr: 0x84		**IOS_PPG2_SUB3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub3*	0	RW	PD Offset Current for Modulator 2 in subsample 3.

8.9.12 IOS_PPG2_SUB4 register (Address 0x85)

Table 129: IOS_PPG2_SUB4 register

Addr: 0x85		**IOS_PPG2_SUB4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub4*	0	RW	PD Offset Current for Modulator 2 in subsample 4.

8.9.13 IOS_PPG2_SUB5 register (Address 0x86)

Table 130: IOS_PPG2_SUB5 register

Addr: 0x86		**IOS_PPG2_SUB5**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub5*	0	RW	PD Offset Current for Modulator 2 in subsample 5.

8.9.14 IOS_PPG2_SUB6 register (Address 0x87)

Table 131: IOS_PPG2_SUB6 register

Addr: 0x87		**IOS_PPG2_SUB6**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub6*	0	RW	PD Offset Current for Modulator 2 in subsample 6.

8.9.15 IOS_PPG2_SUB7 register (Address 0x88)

Table 132: IOS_PPG2_SUB7 register

Addr: 0x88		**IOS_PPG2_SUB7**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub7*	0	RW	PD Offset Current for Modulator 2 in subsample 7.

8.9.16 IOS_PPG2_SUB8 register (Address 0x89)

Table 133: IOS_PPG2_SUB8 register

Addr: 0x89		**IOS_PPG2_SUB8**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ppg2_sub8*	0	RW	PD Offset Current for Modulator 2 in subsample 8.

8.9.17 IOS_LEDOFF register (Address 0x8a)

Table 134: IOS_LEDOFF register

Addr: 0x8a		**IOS_LEDOFF**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ios_ledoff*	0	RW	PD Offset Current for all subsamples during LED off sampling phase (Double and Triple Sampling).

8.9.18 IOS_CFG register (Address 0x8b)

Table 135: IOS_CFG register

Addr: 0x8b		**IOS_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*dis_ledoff*	0	RW	0 = Using of the SUBX LEDON PD Offset current for SUBX LEDOFF sampling phase (Double, Triple) 1 = Using the PDOffset current from IOS_LEDOFF for all subsamples **Note:** If IOS_LEDOFF = 0, no current is used.

8.10 Advanced automatic offset control

8.10.1 AOC_SAR_THRES (Address 0x8c)

Table 136: AOC_SAR_THRES register

Addr: 0x8c		**AOC_SAR_THRES**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sar_thres*	0	RW	Threshold for SAR single measurement.

8.10.2 AOC_SAR_RANGE (Address 0x8d)

Table 137: AOC_SAR_RANGE register

Addr: 0x8d		**AOC_SAR_RANGE**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*sar_range_en*	0	RW	Enable the Range for SAR single measurement.
3:0	*sar_range*	0	RW	The Range for SAR single measurement.

8.10.3 AOC_SAR_PPG1 (Address 0x8e)

Table 138: AOC_SAR_PPG1 register

Addr: 0x8e		AOC_SAR_PPG1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sar_ppg1_en*	0	RW	Enabled when using the last SAR value in PPG1. 7:0 …. subsample 8…. subsample 1

8.10.4 AOC_SAR_PPG2 (Address 0x8f)

Table 139: AOC_SAR_PPG2 register

Addr: 0x8f		AOC_SAR_PPG2		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sar_ppg2_en*	0	RW	Enabled when using the last SAR value in PPG2. 7:0 …. subsample 8…. subsample 1

8.11 Post processing

8.11.1 PP_CFG (Address 0x90)

Table 140: PP_CFG register

Addr: 0x90		PP_CFG		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*asat_on*	0	RW	Enable Analog Saturation post processing.
3:0	*asat_fil*	0	RW	Digital Filter for Analog Saturation

8.11.2 PPG1_PP1 (Address 0x91)

Table 141: PPG1_PP1 register

Addr: 0x91		**PPG1_PP1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*ppg1_pp_sub4*	0	RW	Post-processing for Modulator1 in subsample 4. 0: Normal value 1: Invert value 2: Value - *pp_offset* 3: Write value to *pp_offset*
5:4	*ppg1_pp_sub3*	0	RW	Post-processing for Modulator1 in subsample 3. 0: Normal value 1: Invert value 2: Value - *pp_offset* 3: Write value to *pp_offset*
3:2	*ppg1_pp_sub2*	0	RW	Post-processing for Modulator1 in subsample 2. 0: Normal value 1: Invert value 2: Value - *pp_offset* 3: Write value to *pp_offset*
1:0	*ppg1_pp_sub1*	0	RW	Post-processing for Modulator1 in subsample 1. 0: Normal value 1: Invert value 2: Value - *pp_offset* 3: Write value to *pp_offset*

8.11.3 PPG1_PP2 (Address 0x92)

Table 142: PPG1_PP2 register

Addr: 0x92		**PPG1_PP2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*ppg1_pp_sub8*	0	RW	Post-processing for Modulator1 in subsample 8. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
5:4	*ppg1_pp_sub7*	0	RW	Post-processing for Modulator1 in subsample 7. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
3:2	*ppg1_pp_sub6*	0	RW	Post-processing for Modulator1 in subsample 6. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
1:0	*ppg1_pp_sub5*	0	RW	Post-processing for Modulator1 in subsample 5. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset

8.11.4 PPG2_PP1 (Address 0x93)

Table 143: PPG2_PP1 register

Addr: 0x93		**PPG2_PP1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*ppg2_pp_sub4*	0	RW	Post-processing for Modulator2 in subsample 4. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
5:4	*ppg2_pp_sub3*	0	RW	Post-processing for Modulator2 in subsample 3. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
3:2	*ppg2_pp_sub2*	0	RW	Post-processing for Modulator2 in subsample 2. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
1:0	*ppg2_pp_sub1*	0	RW	Post-processing for Modulator2 in subsample 1. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset

8.11.5 PPG2_PP2 (Address 0x94)

Table 144: PPG2_PP2 register

Addr: 0x94		**PPG2_PP2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:6	*ppg2_pp_sub8*	0	RW	Post-processing for Modulator2 in subsample 8. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
5:4	*ppg2_pp_sub7*	0	RW	Post-processing for Modulator2 in subsample 7. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
3:2	*ppg2_pp_sub6*	0	RW	Post-processing for Modulator2 in subsample 6. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset
1:0	*ppg2_pp_sub5*	0	RW	Post-processing for Modulator2 in subsample 5. 0: Normal value 1: Invert value 2: Value - pp_offset 3: Write value to pp_offset

8.12 Sequencer

8.12.1 IRQ_ENABLE (Address 0x95)

Table 145: IRQ_ENABLE register

Addr: 0x95		**IRQ_ENABLE**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*irq_en_iir_overflow*	0	RW	Enable the interrupt for IIR Filter overflow.
6	*irq_en_leadoff*	0	RW	Edge Lead-Off Interrupt.
5	*irq_en_vcsel*	0	RW	VCSEL short to the VDD/VSS or VCSEL watchdog detection.
4	*irq_en_asat*	0	RW	Analog Saturation Interrupt.
3	*irq_en_led_lowvds*	0	RW	LED lowvds Interrupt.
2	*irq_en_fifooverflow*	0	RW	FIFO overflow occurred. Next sample is lost.
1	*irq_en_fifothreshold*	0	RW	FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD
0	*irq_en_sequencer*	0	RW	Sequencer Measurements ended in accordance with SEQ_COUNT>0. No display with continuous measurement SEQ_COUNT=0. Reset by reading the STATUS.

8.12.2 PPG_SUBWAIT (Address 0x96)

Table 146: PPG_SUBWAIT register

Addr: 0x96		**PPG_SUBWAIT**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sub_wait*	0	RW	Distance between the subsamples; N * 1 μs

8.12.3 PPG_SAR_WAIT (Address 0x97)

Table 147: PPG_SAR_WAIT register

Addr: 0x97		**PPG_SAR_WAIT**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sar_wait*	0	RW	Distance between the SAR measurements; N * 1 µs

8.12.4 PPG_LED_INIT (Address 0x98)

Table 148: PPG_LED_INIT register

Addr: 0x98		**PPG_LED_INIT**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_init*	0	RW	t_LED_INIT = N * 1µs with N = 0 ... 255

8.12.5 PPG_FREQL (Address 0x99)

Table 149: PPG_FREQL register

Addr: 0x99		**PPG_FREQL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppg_freq[7:0]*	79	RW	PPG Sample period sequence: T(SEQ) = (n+1) * 31.25 µs f(SEQ) = 1/((n+1) * 31.25 µs)

8.12.6 PPG_FREQH (Address 0x9a)

Table 150: PPG_FREQH register

Addr: 0x9a		PPG_FREQH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppg_freq[15:8]*	79	RW	See PPG_FREQL (Address 0x99).

8.12.7 PPG1_SUB_EN (Address 0x9b)

Table 151: PPG1_SUB_EN register

Addr: 0x9b		PPG1_SUB_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppg1_sub_en*	0	RW	Enable subsamples for Modulator1. Bit 0 to 7 enable or disable subsample 1 to 8.

8.12.8 PPG2_SUB_EN (Address 0x9c)

Table 152: PPG2_SUB_EN register

Addr: 0x9c		PPG2_SUB_EN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ppg2_sub_en*	0	RW	Enable subsamples for Modulator2. Bit 0 to 7 enable or disable subsample 1 to 8.

8.12.9 PPG_MODE1 (Address 0x9d)

Table 153: PPG_MODE1 register

Addr: 0x9d		PPG_MODE1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub1*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.10 PPG_MODE2 (Address 0x9e)

Table 154: PPG_MODE2 register

Addr: 0x9e		**PPG_MODE2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub2*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.11 PPG_MODE3 (Address 0x9f)

Table 155: PPG_MODE3 register

Addr: 0x9f		**PPG_MODE3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub3*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.12 PPG_MODE4 (Address 0xa0)

Table 156: PPG_MODE4 register

Addr: 0xa0		**PPG_MODE4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub4*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.13 PPG_MODE5 (Address 0xa1)

Table 157: PPG_MODE5 register

Addr: 0xa1		**PPG_MODE5**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub5*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.14 PPG_MODE6 (Address 0xa2)

Table 158: PPG_MODE6 register

Addr: 0xa2		PPG_MODE6		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub6*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.15 PPG_MODE7 (Address 0xa3)

Table 159: PPG_MODE7 register

Addr: 0xa3		**PPG_MODE7**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub7*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.16 PPG_MODE8 (Address 0xa4)

Table 160: PPG_MODE8 register

Addr: 0xa4		**PPG_MODE8**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ppg_mode_sub8*	0	RW	This register defines the number of measurement repetitions for the selected measurement mode. 0: No repetition of selected measurement mode 1: 2 measurement repetitions 2: 4 measurement repetitions 3: 8 measurement repetitions 4: 16 measurement repetitions 5: 32 measurement repetitions 6: 64 measurement repetitions 7: 128 measurement repetitions
1:0			RW	Measure Mode 0: Single Sampling 1: Double Sampling 2: Triple Sampling 3: SAR Single Sampling

8.12.17 PPG_CFG (Address 0xa5)

Table 161: PPG_CFG register

Addr: 0xa5		**PPG_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3	*ext_freq*	0	RW	This bit disables the FREQ registers of PPG and ECG. A rising edge on the EXTCLK_SYNC pin starts the measurement of one sample in case *ext_freq* bit is set.
2	*moving_average_on*	0	RW	Turn ON Moving Average for PPG.
1:0	*moving_average_val*	0	RW	Number of samples used for the moving average filter of the PPG. 0: 2 1: 4 2: 8 3: 16

8.12.18 ECG_FREQL (Address 0xa6)

Table 162: ECG_FREQL register

Addr: 0xa6		**ECG_FREQL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg_freq[7:0]*	79	RW	ECG Sample period Sequence: T(SEQ) = (n+1) * 31.25 µs f(SEQ) = 1/((n+1) * 31.25 µs)

8.12.19 ECG_FREQH (Address 0xa7)

Table 163: ECG_FREQH register

Addr: 0xa7		**ECG_FREQH**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg_freq[15:8]*	79	RW	See ECG_FREQL (Address 0xa6).

8.12.20 ECG1_FREQDIVL (Address 0xa8)

Table 164: ECG1_FREQDIVL register

Addr: 0xa8		**ECG1_FREQDIVL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg1_freqdiv[7:0]*	0	RW	ECG Sample period, Sequence 1: T(SEQ1) = (n+1) * T(SEQ) f(SEQ1) = f(SEQ)/(n+1)

8.12.21 ECG1_FREQDIVH (Address 0xa9)

Table 165: ECG1_FREQDIVH register

Addr: 0xa9		ECG1_FREQDIVH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg1_freqdiv[15:8]*	0	RW	See ECG1_FREQDIVL (Address 0xa8).

8.12.22 ECG2_FREQDIVL (Address 0xaa)

Table 166: ECG2_FREQDIVL register

Addr: 0xaa		ECG2_FREQDIVL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg2_freqdiv[7:0]*	0	RW	ECG Sample period, Sequence 2: T(SEQ1) = (n+1) * T(SEQ) f(SEQ1) = f(SEQ)/(n+1)

8.12.23 ECG2_FREQDIVH (Address 0xab)

Table 167: ECG2_FREQDIVH register

Addr: 0xab		ECG2_FREQDIVH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg2_freqdiv[15:8]*	0	RW	See ECG2_FREQDIVL (Address 0xaa).

8.12.24 ECG_SUBS (Address 0xac)

Table 168: ECG_SUBS register

Addr: 0xac		**ECG_SUBS**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2	*ecg2_en*	0	RW	Enable ECG Sequence2
1	*ecg1_en*	0	RW	Enable ECG Sequence1
0	*ecg1_subs*	0	RW	Number of subsamples for ECG Sequence1 (n+1). 0: n = 1 1: n = 2

8.12.25 LEADOFF_INITL (Address 0xad)

Table 169: LEADOFF_INITL register

Addr: 0xad		**LEADOFF_INITL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*leadoff_init[7:0]*	1	RW	Programs the delay from the beginning of each LEAD sequence to the beginning of the LEAD sample measurement.

8.12.26 LEADOFF_INITH (Address 0xae)

Table 170: LEADOFF_INITH register

Addr: 0xae		**LEADOFF_INITH**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*leadoff_init[10:8]*	0	RW	If the decimal value of this register is N, then the delay is N * 4 µs.

8.12.27 ECG_INITL (Address 0xaf)

Table 171: ECG_INITL register

Addr: 0xaf		ECG_INITL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecg_init[7:0]*	1	RW	Programs the time delay from the beginning of each ECGAMP sequence to the beginning of the ECGAMP sample measurement.

8.12.28 ECG_INITH (Address 0xb0)

Table 172: ECG_INITH register

Addr: 0xb0		ECG_INITH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*ecg_init[10:8]*	1	RW	If the decimal value of this register is N, then the delay is N * 4µs.

8.12.29 SAMPLE_NUM (Address 0xb1)

Table 173: SAMPLE_NUM register

Addr: 0xb1		SAMPLE_NUM		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*sample_num*	1	RW	Number of samples for the active channel. If *seq_sample* = 0, the sequencer runs continuously.

8.13 ECG/BioZ

8.13.1 BIOZ_CFG (Address 0xb2)

Table 174: BIOZ_CFG register

Addr: 0xb2		**BIOZ_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*gsr_en*	0	RW	Enable GSR measurement. 0: Power down 1: Enable
0	*bioz_en*	0	RW	Enable BIOZ measurement. 0: Power down 1: Enable

8.13.2 BIOZ_EXCIT (Address 0xb3)

Table 175: BIOZ_EXCIT register

Addr: 0xb3		**BIOZ_EXCIT**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:4	*bioz_excit_curr*	0	RW	Control BioZ excitation current amplitude from 10 µA to 100 µA, if bioz_en = 1. 0: 10 µA 1: 25 µA 2: 40 µA 3: 55 µA 4: 70 µA 5: 85 µA 6: 100 µA 7: do not use
3:0	*bioz_excit_freq_sel*	0	RW	Control BioZ excitation signal frequency from 1 kHz to 1 MHz. 0: 1 MHz 1: 500 kHz 2: 250 kHz 3: 125 kHz 4: 100 kHz 5: 50 kHz 6: 45.45 kHz 7: 35.71 kHz 8: 25 kHz 9: 20 kHz 10: 15.15 kHz 11: 10 kHz 12: 8.06 kHz 13: 5 kHz 14: 2.5 kHz 15: 1 kHz

8.13.3 BIOZ_MIXER (Address 0xb4)

Table 176: BIOZ_MIXER register

Addr: 0xb4		**BIOZ_MIXER**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:0	*bioz_mix_phase*	0	RW	Mixer control signal phase shift. 1 MHz excit freq: mix_ph_con * 18° Max value (19) : 342° Non-1 MHz excit freq: mix_ph_con * 9° Max value (31) : 279°4: 70 µA 5: 85 µA 6: 100 µA 7: 115 µA

8.13.4 BIOZ_SELECT (Address 0xb5)

Table 177: BIOZ_SELECT register

<table>
<tr><th>Addr: 0xb5</th><th></th><th colspan="3">BIOZ_SELECT</th></tr>
<tr><th>Bit</th><th>Bit name</th><th>Default</th><th>Access</th><th>Bit description</th></tr>
<tr><td>6:4</td><td><i>bioz_meas_sel</i></td><td>0</td><td>RW</td><td>BIOZ measurement selection:
0: Bioimpedance or gsr measurement
1: Offset (0 Ω) measurement
2: Internal 2 kΩ resistor measurement
3: Internal 1 MΩ resistor measurement
4: Internal 1 kΩ resistor measurement
5: Internal 500 Ω resistor measurement</td></tr>
<tr><td>3:0</td><td><i>bioz_inmux_sel</i></td><td>0</td><td>RW</td><td>BIOZ input mux selection:
<table>
<tr><th></th><th>V_INP</th><th>V_INN</th><th>I_INP</th><th>I_INN</th></tr>
<tr><td>0:</td><td>BIOZ1</td><td>BIOZ2</td><td>BIOZ3</td><td>BIOZ4</td></tr>
<tr><td>1:</td><td>BIOZ1</td><td>BIOZ3</td><td>BIOZ2</td><td>BIOZ4</td></tr>
<tr><td>2:</td><td>BIOZ1</td><td>BIOZ4</td><td>BIOZ2</td><td>BIOZ3</td></tr>
<tr><td>3</td><td>BIOZ2</td><td>BIOZ3</td><td>BIOZ1</td><td>BIOZ4</td></tr>
<tr><td>4:</td><td>BIOZ2</td><td>BIOZ4</td><td>BIOZ1</td><td>BIOZ3</td></tr>
<tr><td>5:</td><td>BIOZ3</td><td>BIOZ4</td><td>BIOZ1</td><td>BIOZ2</td></tr>
<tr><td>6:</td><td>BIOZ1</td><td>BIOZ2</td><td>BIOZ1</td><td>BIOZ2</td></tr>
<tr><td>7:</td><td>BIOZ1</td><td>BIOZ3</td><td>BIOZ1</td><td>BIOZ3</td></tr>
<tr><td>8:</td><td>BIOZ1</td><td>BIOZ4</td><td>BIOZ1</td><td>BIOZ4</td></tr>
<tr><td>9:</td><td>BIOZ2</td><td>BIOZ3</td><td>BIOZ2</td><td>BIOZ3</td></tr>
<tr><td>10:</td><td>BIOZ2</td><td>BIOZ4</td><td>BIOZ2</td><td>BIOZ4</td></tr>
<tr><td>11:</td><td>BIOZ3</td><td>BIOZ4</td><td>BIOZ3</td><td>BIOZ4</td></tr>
</table></td></tr>
</table>

8.13.5 BIOZ_GAIN (Address 0xb6)

Table 178: BIOZ_GAIN register

Addr: 0xb6		BIOZ_GAIN		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
0	*bioz_gain*	0	RW	Select AFE gain: 0: x1 gain 1: x2 gain

8.13.6 ECGMOD_CFG1 (Address 0xb7)

Table 179: ECGMOD_CFG1 register

Addr: 0xb7		ECGMOD_CFG1		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3	*ecgmod_en*	0	RW	Enable ADC. 0: ADC power down 1: ADC enable
2	*ecgmod_gainh*	0	RW	This bit control the ECG modulator gain range. Do not change this parameter and leave it with its default configuration. 0: Normal gain range 1: High gain range
1:0	*ecgmod_ibias_sel*	0	RW	The register controls the bias current setting for the ECG modulator. Do not change this parameter and leave it with its default configuration. 0: 10 µA bias current 1: 5 µA bias current 2: 12.5 µA bias current 3: 6.25 µA bias current

8.13.7 ECGMOD_CFG2 (Address 0xb8)

Table 180: ECGMOD_CFG2 register

Addr: 0xb8		**ECGMOD_CFG2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4:2	*ecgmod_reset_delay*	0	RW	Reset Time for ECG Modulator N * MOD_CLK. 0: N = 4 1: N = 8 2: N = 16 3: N = 32 4: N = 64 5: N = 128 >5: N = 256
1:0	*ecgmod_clk*	0	RW	ECG Modulator clock frequency MOD_CLK. Sequence1 and Sequence2 use the same Modulator frequency. 0: 10 MHz 1: 5 MHz 2: 2.5 MHz 3: 1.25 MHz

8.13.8 ECGIMUX_CFG1 (Address 0xb9)

Table 181: ECGIMUX_CFG1 register

Addr: 0xb9		**ECGIMUX_CFG1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*ecgmod_imux_en*	0	RW	Enables the input multiplexer of the ECG modulator. 0: ECGMOD_IMUX disabled 1: ECGMOD_IMUX enabled
5:4	*ecgmod_imux_lpf_fc*	0	RW	Selects the nominal cut-off frequency of the antialiasing low-pass filer. 0: 200 Hz 1: 270 Hz 2: 400 Hz 3: 800 Hz
3:0	*reserved*	0	RW	Reserved system register. Do not change default register value.

8.13.9 ECGIMUX_CFG2 (Address 0xba)

Table 182: ECGIMUX_CFG2 register

Addr: 0xba		**ECGIMUX_CFG2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*sub2_imux_gain*	0	RW	Selects the gain of the output buffer of ECGMOD_IMUX for the referred sub-sequence, sub2. 0: Gain = 1 1: Gain = 2
6:4	*sub2_imux_sel2*	0	RW	Selects the input of the second stage multiplexer for the referred sub-sequence, sub2. 0: Filtered signal coming from first stage multiplexer 1: Unfiltered signal coming from first stage multiplexer 2: ECG lead detection 3: GSR signal 4: IDEMOD 5: QDEMOD 6: Temperature
3	*sub1_imux_gain*	0	RW	Selects the gain of the output buffer of ECGMOD_IMUX for the referred sub-sequence, sub1. 0: Gain = 1 1: Gain = 2
2:0	*sub1_imux_sel2*	0	RW	Selects the input of the second stage multiplexer for the referred sub-sequence, sub1. 0: Filtered signal coming from first stage multiplexer 1: Unfiltered signal coming from first stage multiplexer 2: ECG lead detection 3: GSR signal 4: IDEMOD 5: QDEMOD 6: Temperature

8.13.10 ECGIMUX_CFG3 (Address 0xbb)

Table 183: ECGIMUX_CFG3 register

Addr: 0xbb		**ECGIMUX_CFG3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3	*sub3_imux_gain*	0	RW	Selects the gain of the output buffer of ECGMOD_IMUX for the referred sub-sequence, sub3. 0: Gain = 1 1: Gain = 2
2:0	*sub3_imux_sel2*	0	RW	Selects the input of the second stage multiplexer for the referred sub-sequence, sub3. 0: Filtered signal coming from first stage multiplexer 1: Unfiltered signal coming from first stage multiplexer 2: ECG lead detection 3: GSR signal 4: BIOZ 5: QDEMOD 6: Temperature

8.13.11 ECGAMP_CFG1 (Address 0xbc)

Table 184: ECGAMP_CFG1 register

Addr: 0xbc		**ECGAMP_CFG1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*ecgamp_en*	0	RW	Enable ECG Amplifier. 0: Disabled 1: Enabled
5	*ecgamp_ref_en*	0	RW	Enable ECG reference amplifier. 0: Disabled 1: Enabled
4	*ecgamp_fast_startup*	0	RW	ECG reference amplifier fast startup. 0: Normal startup 1: Fast startup
3	*ecgamp_gm_high*	0	RW	ECG reference amplifier high gm. 0: Normal gain 1: High gain
2	*ecgamp_leadoff_en*	0	RW	This bit programs the value of the signal during the ECGAMP signal measurement phase. 0: Leadoff current disabled during the ECGAMP signal measurement 1: Leadoff current enabled during the ECGAMP signal measurement
1:0	*ecgamp_leadoff_pol*	2	RW	These bits define how the signal behaves during leadoff detection sequence: 00: The ecgamp_leadoff_pol signal is low all the time during leadoff detection sequence. 01: The ecgamp_leadoff_pol signal is high all the time during leadoff detection sequence. 10: The ecgamp_leadoff_pol signal toggles after each lead measurement during leadoff detection sequence, but the first value is 0. 11: The ecgamp_leadoff_pol signal toggles after each lead measurement during leadoff detection sequence, but the first value is 1.

8.13.12 ECGAMP_CFG2 (Address 0xbd)

Table 185: ECGAMP_CFG2 register

Addr: 0xbd		**ECGAMP_CFG2**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6	*ecgamp_leadoff_curr*	0	RW	Most significant bit select between normal ranges and special low current range: 0: Normal Ranges. 1: Special low current range
5:4			RW	If ecgamp_leadoff_curr[6] = 0: Select the LSB current 0: 6.25 nA 1: 12.5 nA 2: 18.75 nA 3: 25 nA If ecgamp_leadoff_curr[6] = 1: Ignored. The LSB is set to 1.6 nA.
3:0			RW	The last four bits select the lead-off current (from 1 LSB to 16 LSB).

8.13.13 ECGAMP_CFG3 (Address 0xbe)

Table 186: ECGAMP_CFG3 register

Addr: 0xbe		**ECGAMP_CFG3**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*reserved*	0	RW	Reserved system register. Do not change default register value.
6	*ecgamp_hp_en*	0	RW	Enable ECG SC high-pass filter. 0: ECG SC HP Filter off 1: ECG SC HP Filter on
5	*ecgamp_hp_byp*	0	RW	Bypass ECG SC high-pass filter. 0: ECG SC HP Filter bypass off 1: ECG SC HP Filter bypass on
4:3	*ecgamp_hp_csel*	3	RW	Select the capacitor value in ECG SC high-pass filter. 0: 750 fF 1: 750 fF/2 2: 750 fF/4 3: 750 fF/8
2:0	*ecgamp_hp_clk_freq*	1	RW	Select the clock frequency in ECG SC high-pass filter. 0: 977 Hz (1 MHz/1024) 1: 1953 Hz (1 MHz/512) 2: 3906 Hz (1 MHz/256) 3: 7813 Hz (1 MHz/128) 4: 15.6 kHz (1 MHz/64) 5: 250 kHz 6: 500 kHz 7: 1 MHz

8.13.14 ECGAMP_CFG4 (Address 0xbf)

Table 187: ECGAMP_CFG4 register

Addr: 0xbf		**ECGAMP_CFG4**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*ecgamp_hp_clk_pw*	0	RW	This registers controls the clock pulse width of the ECG SC high-pass filter. Please do not change register unless instructed by ams OSRAM support team. 0: 0.5 µs 1: 1 µs 2: 2 µs … 254: 254 µs 255: 50% duty cycle

8.13.15 ECGAMP_CFG5 (Address 0xc0)

Table 188: ECGAMP_CFG5 register

Addr: 0xc0		ECGAMP_CFG5		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ecgamp_lp_en*	0	RW	Enable ECG SC low-pass filter. 0: ECG SC LP Filter off 1: ECG SC LP Filter on
6	*ecgamp_lp_byp*	0	RW	Bypass ECG SC low-pass filter. 0: ECG SC LP Filter bypass off 1: ECG SC LP Filter bypass on
5:4	*ecgamp_lp_clk_freq*	2	RW	Select the clock frequency in ECG SC low-pass filter. 0: 1 MHz/8 (fc_lpf = 80 Hz) 1: 1 MHz/4 (fc_lpf = 160 Hz) 2: 1 MHz/2 (fc_lpf = 320 Hz) 3: 1 MHz/1 (fc_lpf = 640 Hz)
3	*ecgamp_ina1_en*	0	RW	Enable ECG INA 1. 0: Power down 1: Enabled
2	*ecgamp_rld_ccomp*	0	RW	Extra compensation capacitor for RLD loop. 0: No capacitor 1: 5 pF capacitor
1:0	*ecgamp_ina1_gain*	3	RW	Select the gain of INA 1. 0: Gain = 1 1: Gain = 2 2: Gain = 3 3: Gain = 4

8.13.16 ECGAMP_CFG6 (Address 0xc1)

Table 189: ECGAMP_CFG6 register

Addr: 0xc1		**ECGAMP_CFG6**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*ecgamp_ina2_en*	0	RW	Enable ECG INA 2. 0: ECG INA 2 off 1: ECG INA 2 on
3	*ecgamp_ina2_byp*	0	RW	Bypass ECG INA 2. 0: ECG INA 2 bypass off 1: ECG INA 2 bypass on
2:0	*ecgamp_ina2_gain*	5	RW	Select the gain of INA 2. 0: Gain = 1 1: Gain = 2 2: Gain = 4 3: Gain = 8 4: Gain = 16 5: Gain = 32 6: Gain = 64 7: Gain = 128

8.13.17 ECGAMP_CFG7 (Address 0xc2)

Table 190: ECGAMP_CFG7 register

Addr: 0xc2		**ECGAMP_CFG7**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*ecgamp_chop1_en*	0	RW	Enable chopper for INA1: 0: Disabled 1: Enabled
6:4	*ecgamp_chop1_clk_freq*	0	RW	Frequency of the INA1 chopper modulators clock. When ecgamp_chop1_en is 1, then: 0: 1 kHz 1: 2 kHz 2: 4 kHz 3: 8 kHz 4: 16 kHz 5-7: 32 kHz If ecgamp_chop1_en is 0, then the signal ecgamp_chop1_clk must be 0.
3	*ecgamp_chop2_en*	0	RW	Enable chopper for INA2: 0: Disabled 1: Enabled
2:0	*ecgamp_chop2_clk_freq*	0	RW	Frequency of the INA2 chopper modulators clock. When ecgamp_chop2_en is 1, then: 0: 4 kHz 1: 8 kHz 2: 16 kHz 3: 32 kHz 4: 64kHz 5: 100 kHz 6: 100 kHz 7: 100 kHz If ecgamp_chop2_en is 0, then the signal ecgamp_chop2_clk must be 0.

8.13.18 ECG_BIOZ (Address 0xc3)

Table 191: ECG_BIOZ register

Addr: 0xc3		**ECG_BIOZ**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2:0	*ecg_bioz_ovs*	0	RW	Oversampling after SINC/Average.

8.14 Lead-Off

8.14.1 LEADOFF_CFG (Address 0xc4)

Table 192: LEADOFF_CFG register

Addr: 0xc4		**LEADOFF_CFG**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5	*leadoff_en*	0	RW	Enable Leadoff. 0: Disable 1: Enable
4:3	*leadoff_edge*	0	RW	Enable Event for Generation Leadoff Interrupt. Bit 0: Negedge Leadoff Bit 1: Posedge Leadoff
2:0	*leadoff_ovs*	0	RW	Oversampling for Leadoff Off. 0-7: 1-8 Values for change Leadoff Status

8.14.2 LEADOFF_THRESL (Address 0xc5)

Table 193: LEADOFF_THRESL register

Addr: 0xc5		**LEADOFF_THRESL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*leadoff_thres[7:0]*	0	RW	Threshold for Leadoff (low byte).

8.14.3 LEADOFF_THRESH (Address 0xc6)

Table 194: LEADOFF_THRESH register

Addr: 0xc6	LEADOFF_THRESH			
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*leadoff_thres[15:8]*	0	RW	Threshold for Leadoff (high byte).

8.15 IIR filter

8.15.1 IIR_CFG (Address 0xc7)

Table 195: IIR_CFG register

<table>
<tr><th>Addr: 0xc7</th><th>IIR_CFG</th><th></th><th></th><th></th></tr>
<tr><th>Bit</th><th>Bit name</th><th>Default</th><th>Access</th><th>Bit description</th></tr>
<tr><td>4</td><td><i>iir_enable</i></td><td>0</td><td>RW</td><td>IIR filter enable.</td></tr>
<tr><td>3:0</td><td><i>iir_num_sos</i></td><td>5</td><td>RW</td><td>IIR filter number of cascaded SOS structures.
<table>
<tr><th>Enumeration</th><th>Number of SOS</th><th>Filter Order</th></tr>
<tr><td>0</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>2</td><td>4</td></tr>
<tr><td>2</td><td>3</td><td>6</td></tr>
<tr><td>3</td><td>4</td><td>8</td></tr>
<tr><td>4</td><td>5</td><td>10</td></tr>
<tr><td>5</td><td>6</td><td>12</td></tr>
<tr><td>6</td><td>7</td><td>14</td></tr>
<tr><td>7</td><td>8</td><td>16</td></tr>
<tr><td>8</td><td>9</td><td>18</td></tr>
<tr><td>9</td><td>10</td><td>20</td></tr>
<tr><td>10</td><td>11</td><td>22</td></tr>
<tr><td>11</td><td>12</td><td>24</td></tr>
<tr><td>Others</td><td>12</td><td>24</td></tr>
</table>
</td></tr>
</table>

8.15.2 IIR_COEFF_ADDR (Address 0xc8)

Table 196: IIR_COEFF_ADDR register

Addr: 0xc8		**IIR_COEFF_ADDR**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
6:0	*iir_coeff_addr*	0	R_PUSH	RAM for coefficient address.

8.15.3 IIR_COEFF_DATA (Address 0xc9)

Table 197: IIR_COEFF_DATA register

Addr: 0xc9		**IIR_COEFF_DATA**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*iir_coeff_data*	0	R_PUSH	RAM for coefficient data.

8.16 FIFO

8.16.1 FIFO_THRESHOLD (Address 0xca)

Table 198: FIFO_THRESHOLD register

Addr: 0xca		**FIFO_THRESHOLD**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifo_threshold[7:0]*	64	RW	FIFO threshold Bit 7:0 0 = Interrupt on one sample

8.16.2 FIFO_CTRL (Address 0xcb)

Table 199: FIFO_CTRL register

Addr: 0xcb		**FIFO_CTRL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*fifo_clear*	0	RW	Write 1 here to clear the FIFO.
3	*seq_sync_en*	0	RW	Write Synchronization Information.
2	*sinc_randext_en*	1	RW	Enables SINC data extension with randomized bits, otherwise zeros are inserted.
1	*sar_data_en*	0	RW	Write 4-bit SAR into SINC data Bit (3:0).
0	*fifo_threshold[8]*	0	RW	FIFO threshold Bit 8.

8.17 Miscellaneous

8.17.1 PRODUCT_ID (Address 0xeb)

Table 200: PRODUCT_ID register

Addr: 0xeb		**PRODUCT_ID**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
5:1	*otp_part_id*	-	RO	Image of the OTP bit for part ID.

8.17.2 SILICON_ID (Address 0xec)

Table 201: SILICON_ID register

Addr: 0xec		**SILICON_ID**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*silicon_id*	0x92	RO	Silicon identification number.

8.17.3 GPIO_CTRL (Address 0xee)

Table 202: GPIO_CTRL register

Addr: 0xee		GPIO_CTRL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*gpio_in*	0	RW	Readable value from the GPIO.
0	*gpio_out*	0	RW	Programmable GPIO output.

8.17.4 CHIP_CTRL (Address 0xef)

Table 203: CHIP_CTRL register

Addr: 0xef		CHIP_CTRL		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*wd_reset*	0	W	Writing this register resets the watchdog output inside VCSEL safety block to remove an error condition.
0	*chip_reset*	0	W	Writing this registers triggers a power on reset condition.

8.17.5 SEQ_START (Address 0xf0)

Table 204: SEQ_START register

Addr: 0xf0		SEQ_START		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*start_seq*	0	R_PUSH	Write a pulse for the start or stop of the measurements. 0: Stop 1: Start Read the status of the measurement. 0: Inactive 1: Active The number of measurements is specified in the SEQ_SAMPLE register.

8.17.6 STATUS_CGB (Address 0xf1)

Table 205: STATUS_CGB register

Addr: 0xf1		**STATUS_CGB**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*pll_lock*	0	RO	PLL locked state indicator.
0	*clk_pll_ok*	0	RO	Status indicator of CLK20M.

8.17.7 STATUS_SEQ (Address 0xf2)

Table 206: STATUS_SEQ register

Addr: 0xf2		**STATUS_SEQ**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
1	*seq_end*	0	RO	Measurement was stopped.
0	*seq_error*	0	RO	Measurement of a sample was not started. Sample frequency is too high.

8.17.8 STATUS_LED (Address 0xf3)

Table 207: STATUS_LED register

Addr: 0xf3		**STATUS_LED**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*led_lowvds*	0	RO	If active, the LED current does not reach the expected value.

8.17.9 STATUS_ASATA (Address 0xf4)

Table 208: STATUS_ASATA register

Addr: 0xf4		**STATUS_ASATA**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*mod1_asat*	0	RO	Analog Saturation Modulator1.
3:0	*mod2_asat*	0	RO	Analog Saturation Modulator2.

8.17.10 STATUS_ASATB (Address 0xf5)

Table 209: STATUS_ASATB register

Addr: 0xf5		**STATUS_ASATB**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
3:0	*mod3_asat*	0	RO	Analog Saturation Modulator 3.

8.17.11 STATUS_VCSEL (Address 0xf6)

Table 210: STATUS_VCSEL register

Addr: 0xf6		**STATUS_VCSEL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
4	*led_wd*	0	RO	VCSEL LED digital Watchdog occurred t > 1.0 ms.
3	*vcsel_vss*	0	RO	VCSEL short to PGND detected.
2	*vcsel_vdd*	0	RO	VCSEL short to VCSELS detected.
1:0	*vcsel_wd*	0	RO	VCSEL LED analog Watchdog occurred t > 3.2 ms Bit0 - LED Driver 1 Bit1 - LED Driver 2

8.17.12 STATUS_VCSEL_VSS (Address 0xf7)

Table 211: STATUS_VCSEL_VSS register

Addr: 0xf7		**STATUS_VCSEL_VSS**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*vcsel_short_vss*	0	RO	Pin LED8
6			RO	Pin LED7
5			RO	Pin LED6
4			RO	Pin LED5
3			RO	Pin LED4
2			RO	Pin LED3
1			RO	Pin LED2
0			RO	Pin LED1

8.17.13 STATUS_VCSEL_VDD (Address 0xf8)

Table 212: STATUS_VCSEL_VDD register

Addr: 0xf8		**STATUS_VCSEL_VDD**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*vcsel_short_vdd*	0	RO	Pin LED8
6			RO	Pin LED7
5			RO	Pin LED6
4			RO	Pin LED5
3			RO	Pin LED4
2			RO	Pin LED3
1			RO	Pin LED2
0			RO	Pin LED1

8.17.14 STATUS_LEADOFF (Address 0xf9)

Table 213: STATUS_LEADOFF register

Addr: 0xf9		**STATUS_LEADOFF**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2	*leadoff*	0	RO	Internal Lead-Off.
1	*leadoff_on*	0	RO	Lead-Off has been activated. Automatic Reset by reading.
0	*leadoff_off*	0	RO	Lead-Off has been deactivated. Automatic Reset by reading.

8.17.15 STATUS (Address 0xfa)

The STATUS register shows the current status of the interface. When released via IRQ_ENABLE, all the bits can trigger an interrupt.
Reading the STATUS registers only deletes *irq_iir_overflow*, *irq_fifooverflow*, and *irq_sequencer*.
To delete *irq_leadoff*, the **STATUS_LEADOFF** register must be read.
To delete *irq_vcsel*, the **STATUS_VCSEL** register must be read.
To delete *irq_asat*, the **STATUS_ASAT** register must be read.
To delete *irq_lowvds*, the **STATUS_LED** register must be read.
To delete *irq_sequencer*, the **STATUS_SEQ** register must be read.
The interrupt for the fill level of the FIFO *irq_fifothreshold* cannot be deleted directly, but only by lowering the FIFO level.

Table 214: STATUS register

Addr: 0xfa		**STATUS**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7	*irq_iir_overflow*	0	RO	Interrupt status bit if the IIR filter block has an overflow condition.
6	*irq_leadoff*	0	RO	Lead-Off Interrupt. Check Register STATUS_LEADOFF.
5	*irq_vcsel*	0	RO	VCSEL short to VCSELS/PGND or VCSEL watchdog detection. Check Register STATUS_VCSEL, STATUS_VCSEL_VSS and STATUS_VCSEL_VDD.
4	*irq_asat*	0	RO	Analog Saturation Interrupt. Check Register STATUS_ASATA and STATUS_ASATB.
3	*irq_led_lowvds*	0	RO	LED lowvds Interrupt. Check Register STATUS_LED.
2	*irq_fifooverflow*	0	RO	FIFO overflow occurred. The next sample is lost.
1	*irq_fifothreshold*	0	RO	FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD
0	*irq_sequencer*	0	RO	Sequencer Interrupt. Check Register STATUS_SEQ.

8.17.16 FIFO_LEVEL0 (Address 0xfb)

Table 215: FIFO_LEVEL0 register

Addr: 0xfb		**FIFO_LEVEL0**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifo_level[7:0]*	0	RO	FIFO level Bit 7:0.

8.17.17 FIFO_LEVEL1 (Address 0xfc)

Table 216: FIFO_LEVEL1 register

Addr: 0xfc		**FIFO_LEVEL1**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
2	*fifo_overflow*	0	RO	FIFO overflow.
1:0	*fifo_level[9:8]*	0	RO	FIFO level Bit 9:8.

8.17.18 FIFOL (Address 0xfd)

Table 217: FIFOL register

Addr: 0xfd		**FIFOL**		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:4	*fifol*	0	PUSHPOP	Bits 3..0 of ADC
3			PUSHPOP	Block frame
2:0			PUSHPOP	Data marker

8.17.19 FIFOM (Address 0xfe)

Table 218: FIFOM register

Addr: 0xfe		FIFOM		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifom*	0	PUSHPOP	Bits 11..4 of ADC

8.17.20 FIFOH (Address 0xff)

Table 219: FIFOH register

Addr: 0xff		FIFOH		
Bit	**Bit name**	**Default**	**Access**	**Bit description**
7:0	*fifoh*	0	PUSHPOP	Bits 19..12 of ADC

9 Application information

This chapter contains application related information.

9.1 Schematic

Figure 63: AS7058 PPG and ECG application schematic

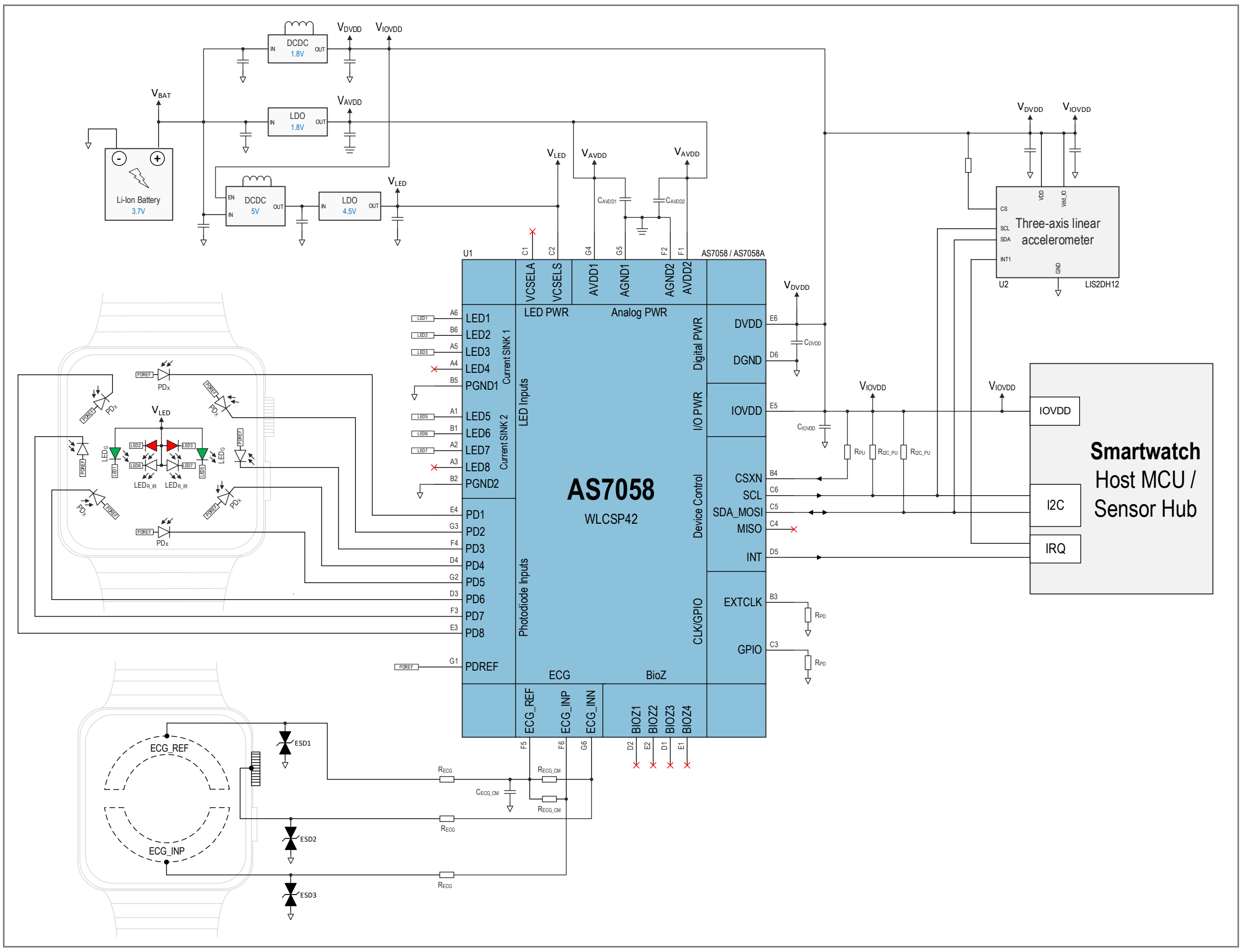


Figure 64: AS7058 PPG, ECG and BioZ application schematic

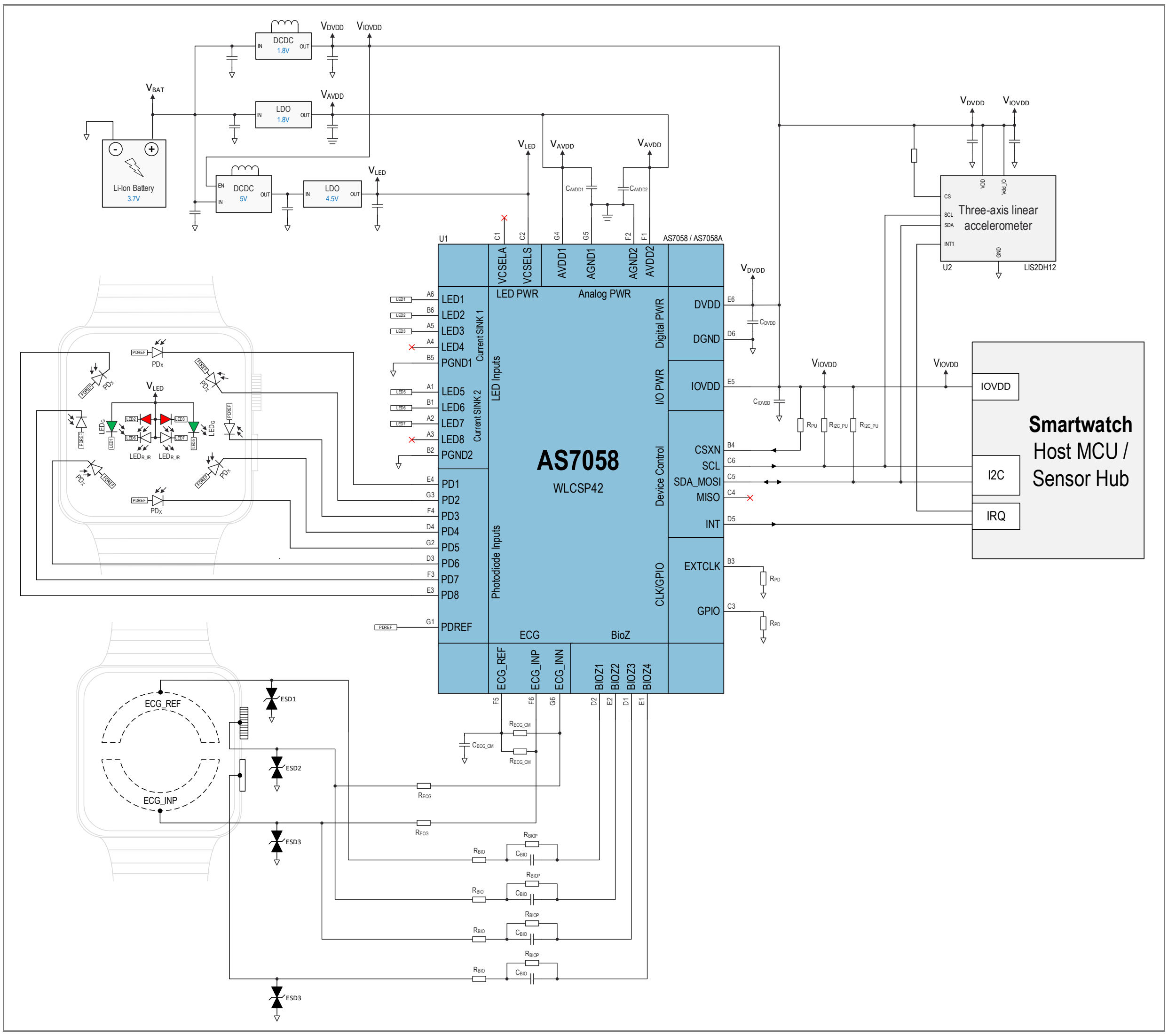
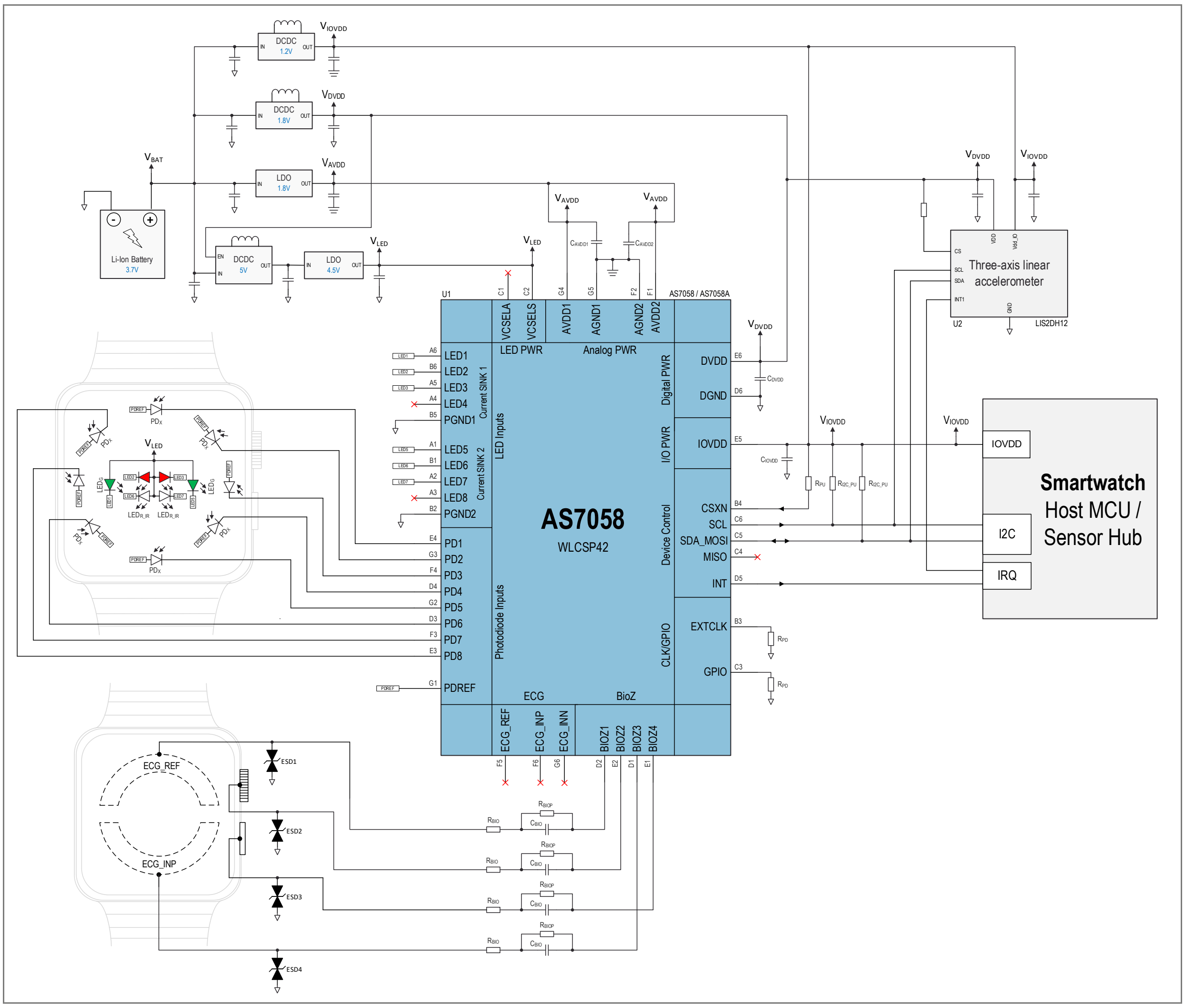


Figure 65: AS7058 PPG and BioZ application schematic with 1.2 V I²C interface voltage



9.2 External components

This chapter provides recommended external components for the example schematics shown in chapter 9.1.

Table 220: External components - capacitors

Symbol	Parameter	Temp. characteristic	Min. rated voltage	Max. tolerance	Recommended typ. value
C_{DVDD}	Input capacitor for DVDD pin	Y5R; X5R	4 V	±10%	1 µF
C_{IOVDD}	Input capacitor for IOVDD pin	Y5R; X5R	4 V	±10%	100 nF
C_{ECG_CM}	Input capacitor for ECG_REF pin	Y5R; X5R	4 V	±1%	100 pF
C_{AVDDx}	Input capacitor for AVVDx pin	Y5R; X5R	4 V	±10%	1 µF
C_{BIO}	Safety protection capacitor	Y5R; X5R	4 V	±10%	47 nF

Table 221: External components - resistors

Symbol	Parameter	Min. power dissipation	Max. tolerance	Min. / Max. nominal resistance	Recommended typ. value
R_{PU}	Pull up resistor	0.03 W	±10%	1 kΩ / 100 kΩ	47 kΩ
R_{I2C_PU}	I²C bus pull up resistors	0.03 W	±10%	1 kΩ / 47 kΩ	10 kΩ
R_{PD}	Pull down resistor	0.03 W	±10%	1 kΩ / 100 kΩ	47 kΩ
R_{ECG}	ECG resistor	0.03 W	±0.1%	50 kΩ / 100 kΩ	50 kΩ
R_{ECG_CM}	ECG common mode rejection resistor	0.03 W	±0.1%	100 kΩ / 1 MΩ	1 MΩ
R_{BIO}	Safety protection resistor	0.03 W	±1%	-	5100 Ω
R_{BIOP}	Safety protection resistor	0.03 W	±1%	-	100 kΩ

Table 222: External components – photodiodes

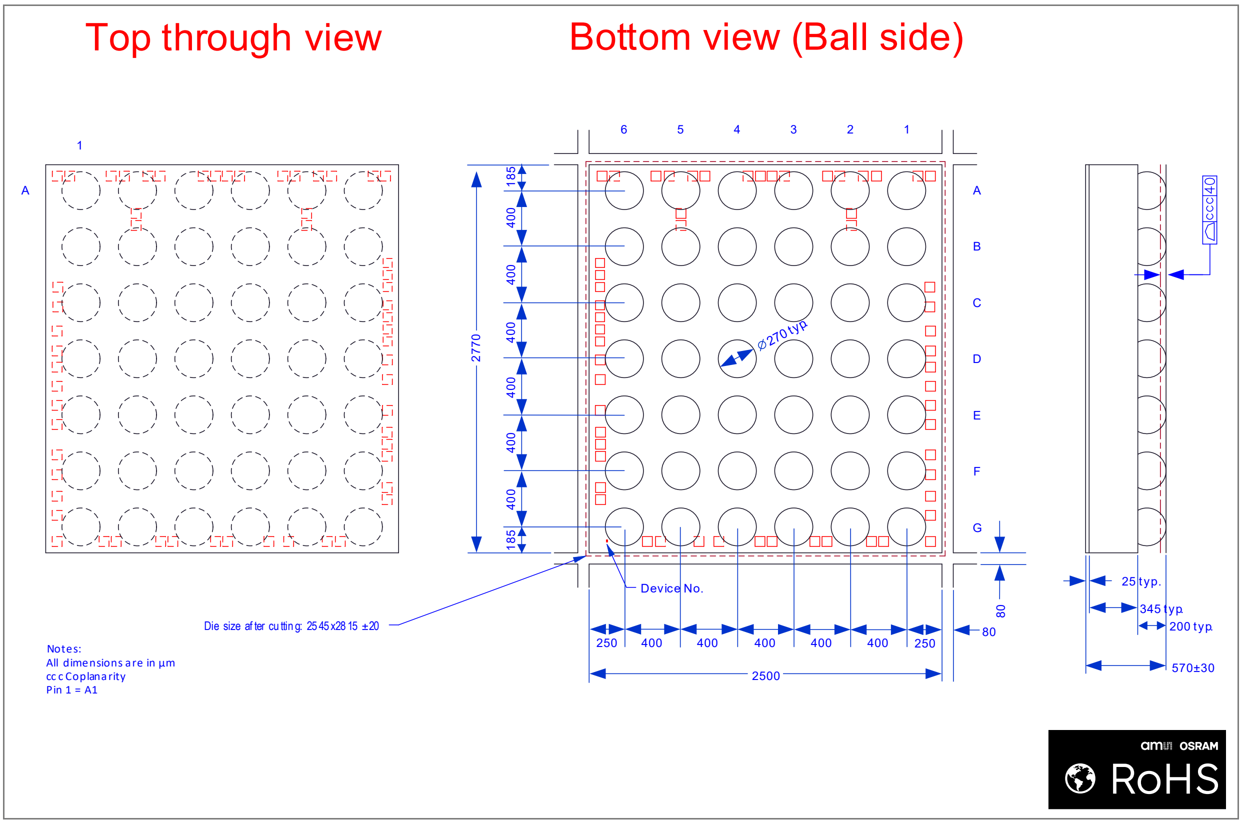
Symbol	Parameter	Vendor	Part number	Max. sensitivity wavelength	Radiant sensitive area
PD_x	Photodiode	ams OSRAM	SFH 2705	930 nm	3.5 mm^2
PD_x	Photodiode	ams OSRAM	SFH 2202	830 nm	8.12 mm^2

Table 223: External components – LEDs

Symbol	Parameter	Vendor	Part number	Typ. forward voltage Green	Typ. forward voltage Red	Typ. forward voltage IR
LED_x	LED module (RED, IR)	ams OSRAM	SFH 7015	-	1.9 V @ 20 mA	1.3 V @ 20 mA
LED_x	LED module (Green, Red, IR)	ams OSRAM	SFH 7018A	2.35V @ 20 mA	1.9 V @ 20 mA	1.3 V @ 20 mA

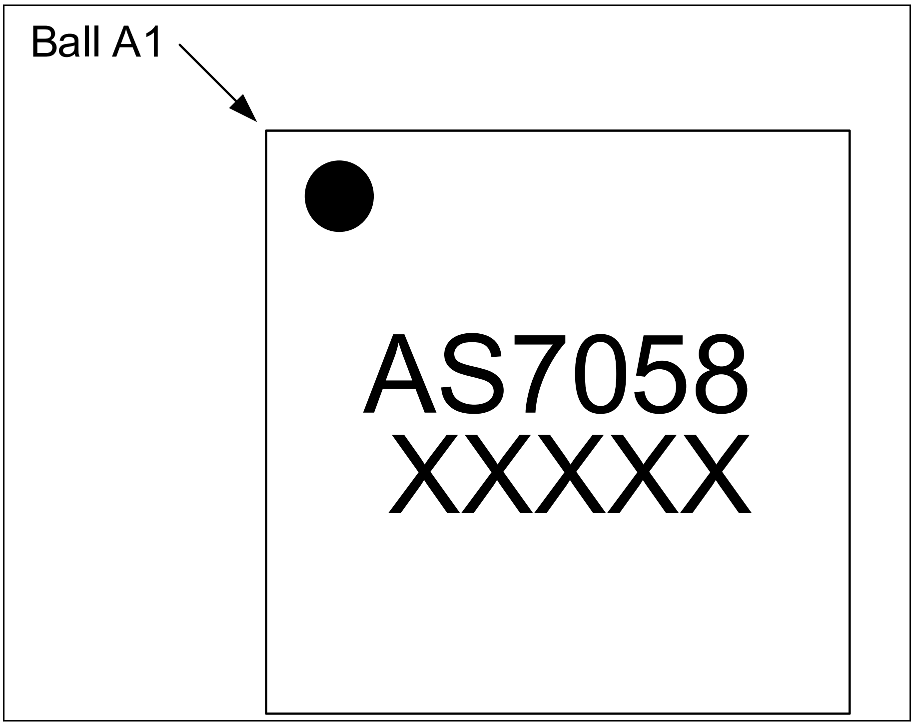
10 Package drawings & markings

Figure 66: WLCSP42 package outline drawing



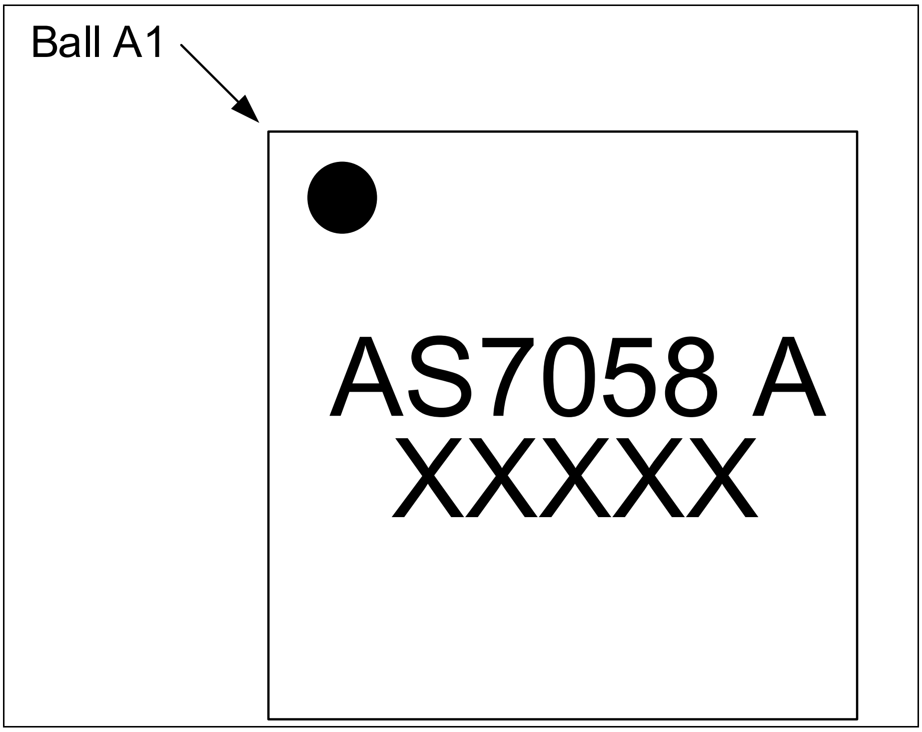
(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

Figure 67: AS7058 WLCSP42 package marking/code



xxxxx	Tracecode

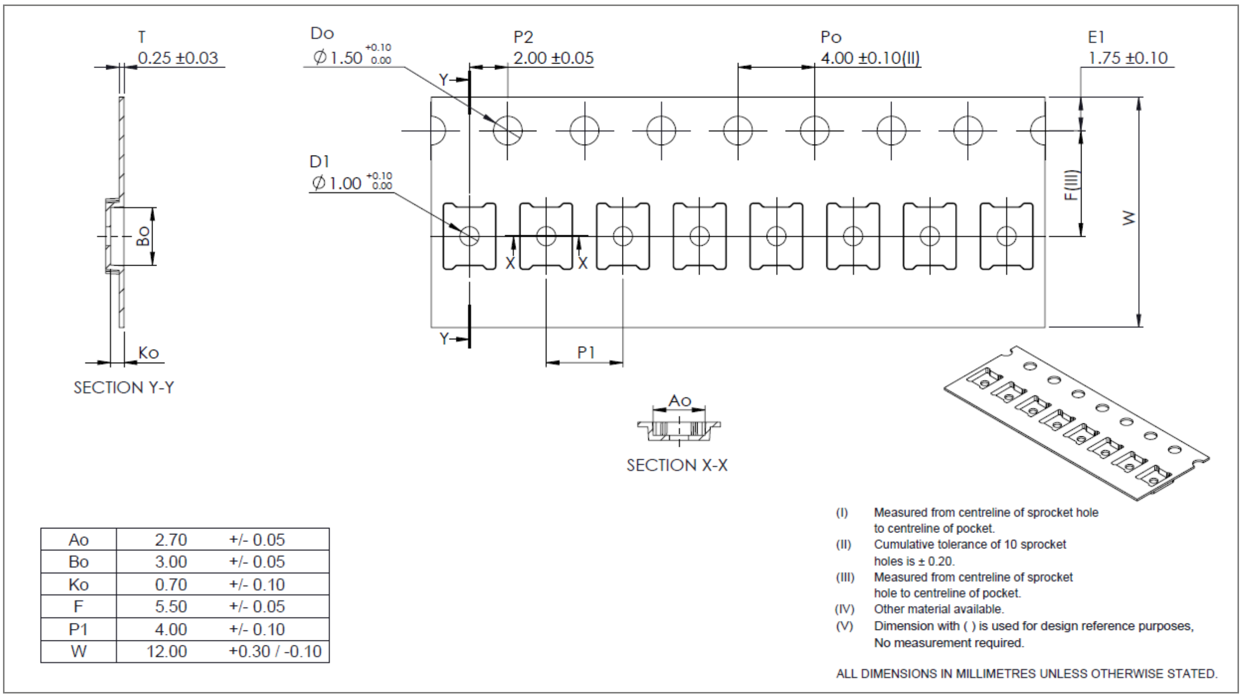
Figure 68: AS7058A WLCSP42 package marking/code



xxxxx	Tracecode

11 Tape & reel information

Figure 69: WLCSP42 tape dimensions



Ao	2.70	+/- 0.05
Bo	3.00	+/- 0.05
Ko	0.70	+/- 0.10
F	5.50	+/- 0.05
P1	4.00	+/- 0.10
W	12.00	+0.30 / -0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension with ( ) is used for design reference purposes, No measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

12 Revision information

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Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous released version to current revision v2-00	Page
Document security class is updated as “PUBLIC” in the footer	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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