AS1163

Datasheet

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AS1163 SAID - Standalone intelligent driver

1 General description

AS1163 is a mixed signal silicon device optimized for dynamic lighting applications.

The basic purpose of AS1163 is to drive 9 LEDs organized in 3 channel triplets (RGB) with an independent PWM dimming dynamic range up to 16 bits.

AS1163 is often addressed with a different name: “SAID”, an acronym, which stands for Stand-Alone Intelligent Driver.

Daisy chain configurations of multiple AS1163 devices will enable cost effective implementation of complex dynamic lighting effects.

AS1163 will support single layer slim PCB designs.

The communication protocol supported by AS1163 is Open System Protocol (OSP), which makes the SAID fully compatible with the ams OSRAM OSIRE E3731i. AS1163 will support additional features such as I²C gateway, parallel connection, power-rail feedback, analog readout.

Each AS1163 device in the chain will be usable by a MCU to read and write an external I²C device, e.g. EEPROM, temperature sensor, Ambient Light Sensor.

AS1163 is with Functional Safety QM and supports to achieve ASIL-B on system level.

1.1 Key benefits & features

The benefits and features of AS1163, SAID - Standalone intelligent driver are listed below:

Table 1: Added value of using AS1163

Benefits	Features
Cost effective system design	Single layer PCB
Slim layout	3x RGB channels per IC
Sensing integration	I²C gateway (compatible with 5V and tolerant for 3V3 and 1V8)
Open system protocol	• Auto-addressing 2.4 Mbit/s two-wire daisy chain protocol • Up to 1000 nodes • CRC protected communication

Benefits	Features
Adjustable output current	1.5, 3, 6, 12, 24, 48 mA
Configurable output power	Output clustering options (up to 288 mA)
Brightness adjustment	16-bit equivalent dynamic range when LSB dithering function is activated. 15-bit PWM engine @ 500 Hz 14-bit PWM engine @ 1000 Hz
• Low EMI • Low power consumption • Reduced phantom effect	Enhanced driving mode (Dithering)
Star network implementation	External setting of parallel addressing (also called branching)
Sync pin	External HW sync for display application
Remote analog input for sensing	Integrated 10-bit ADC + MUX – range VDD – VDD-3.56 V
Functional Safety	QM (compliant with ASIL-B on system level)

1.2 Applications

- Interior dynamic lighting effect
- Ambient lighting
- Functional lighting
- Exterior lighting (e.g. grill application)
- Roof lighting
- Smart surface

1.3 Use case overview

In this section possible use cases of AS1163 are presented.

Figure 1: Use case 1

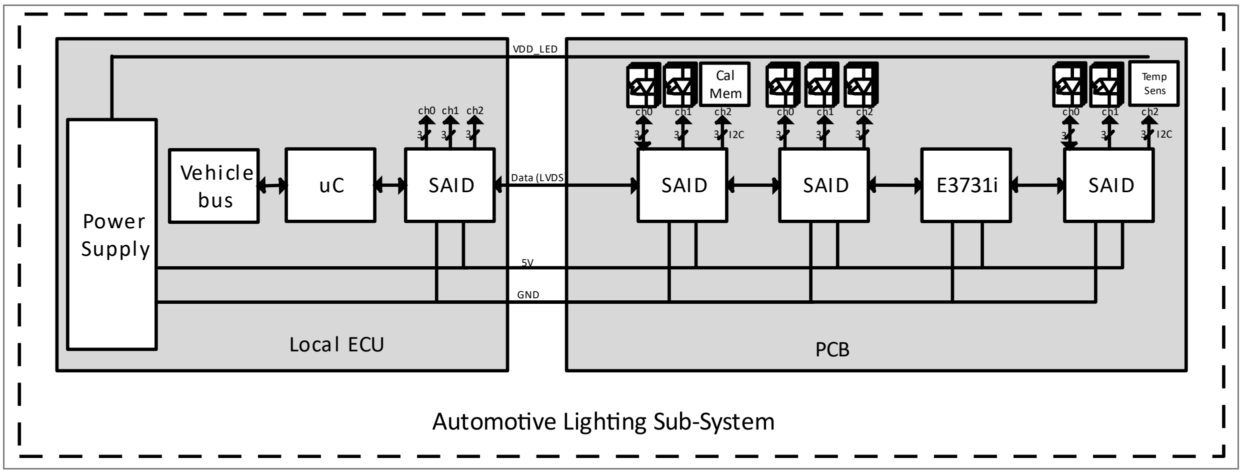


Figure 1 shows daisy chain using LVDS as local bus and supporting OSIRE E3731i and I²C device interfacing.

Figure 2: Use case 2

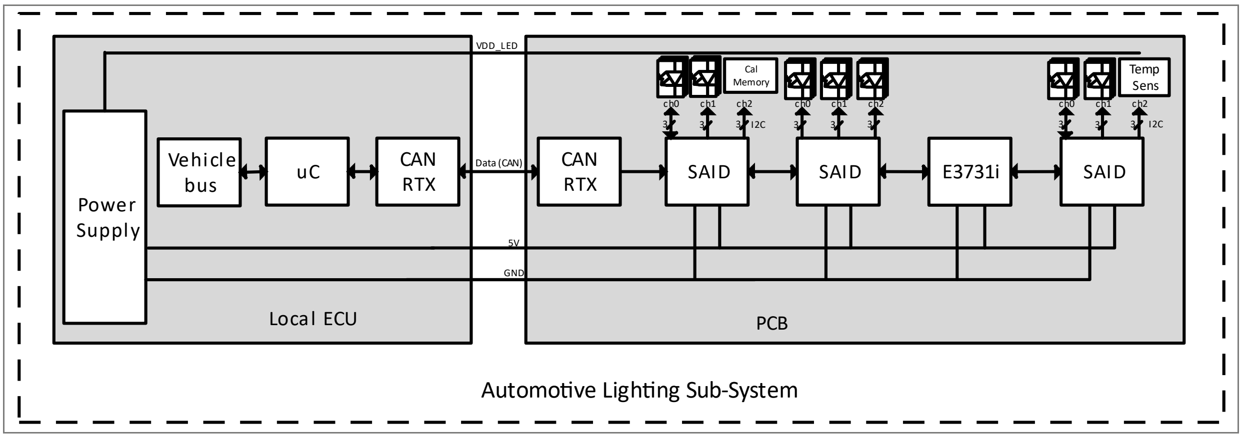


Figure 2 shows daisy chain using CAN bus and supporting OSIRE E3731i and I²C device interfacing.

MCU mode having Manchester downstream and data & clock upstream will produce communication error flags at parallel devices that are not addressed, while MCU - SPI mode supports parallel communication, given its symmetry in downstream and upstream flows.

Figure 3: Use case 3

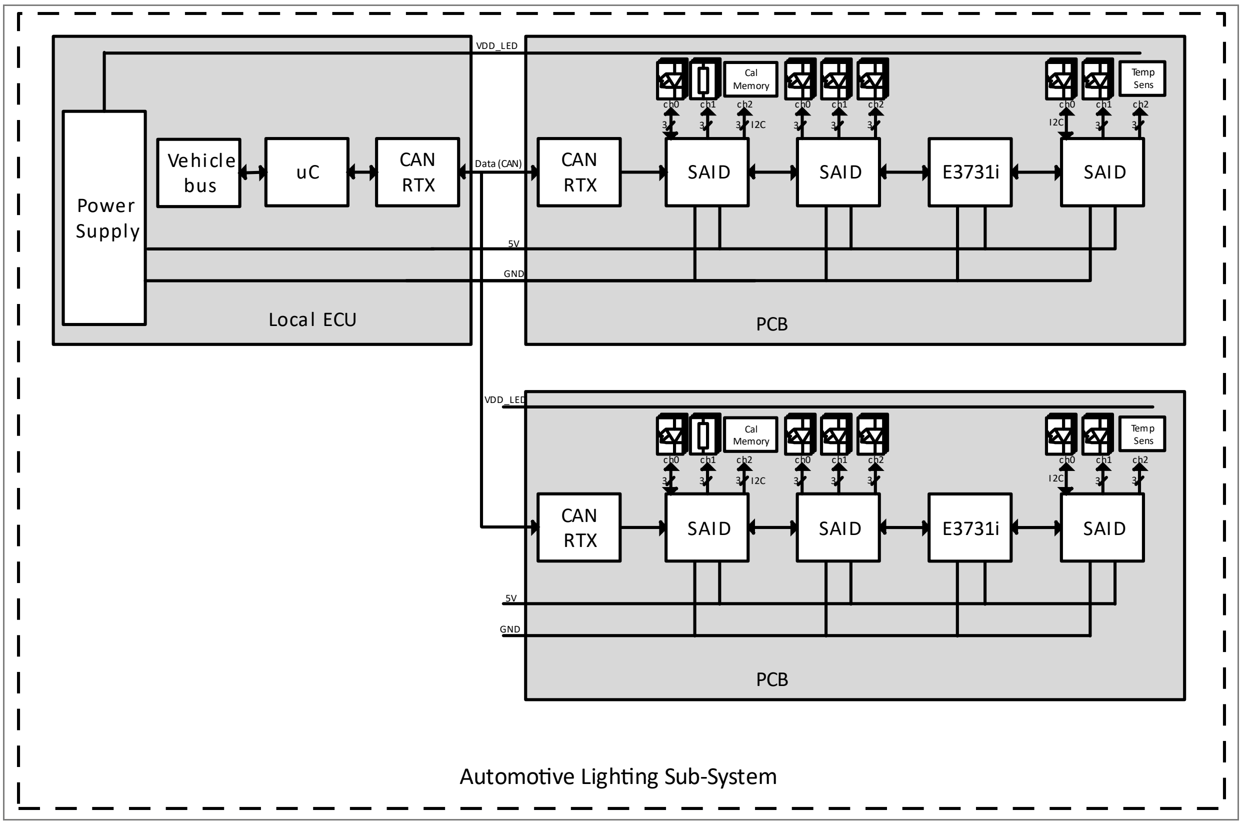


Figure 3 shows parallel connection of Daisy Chains using local CAN bus, supporting OSIRE RGBi and I²C device interfacing.

Parallel addressing (Figure 4) is fully supported with symmetrical communication modes, such as SPI-mode, LVDS mode, CAN mode.

Figure 4: Use case 4

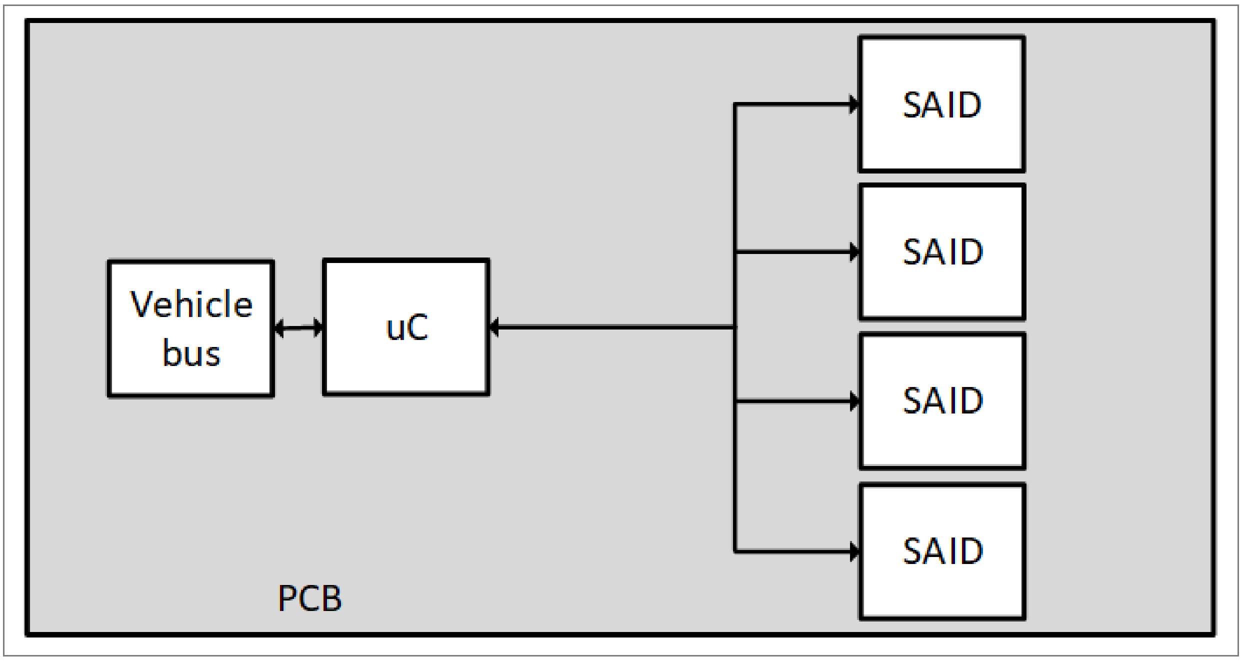
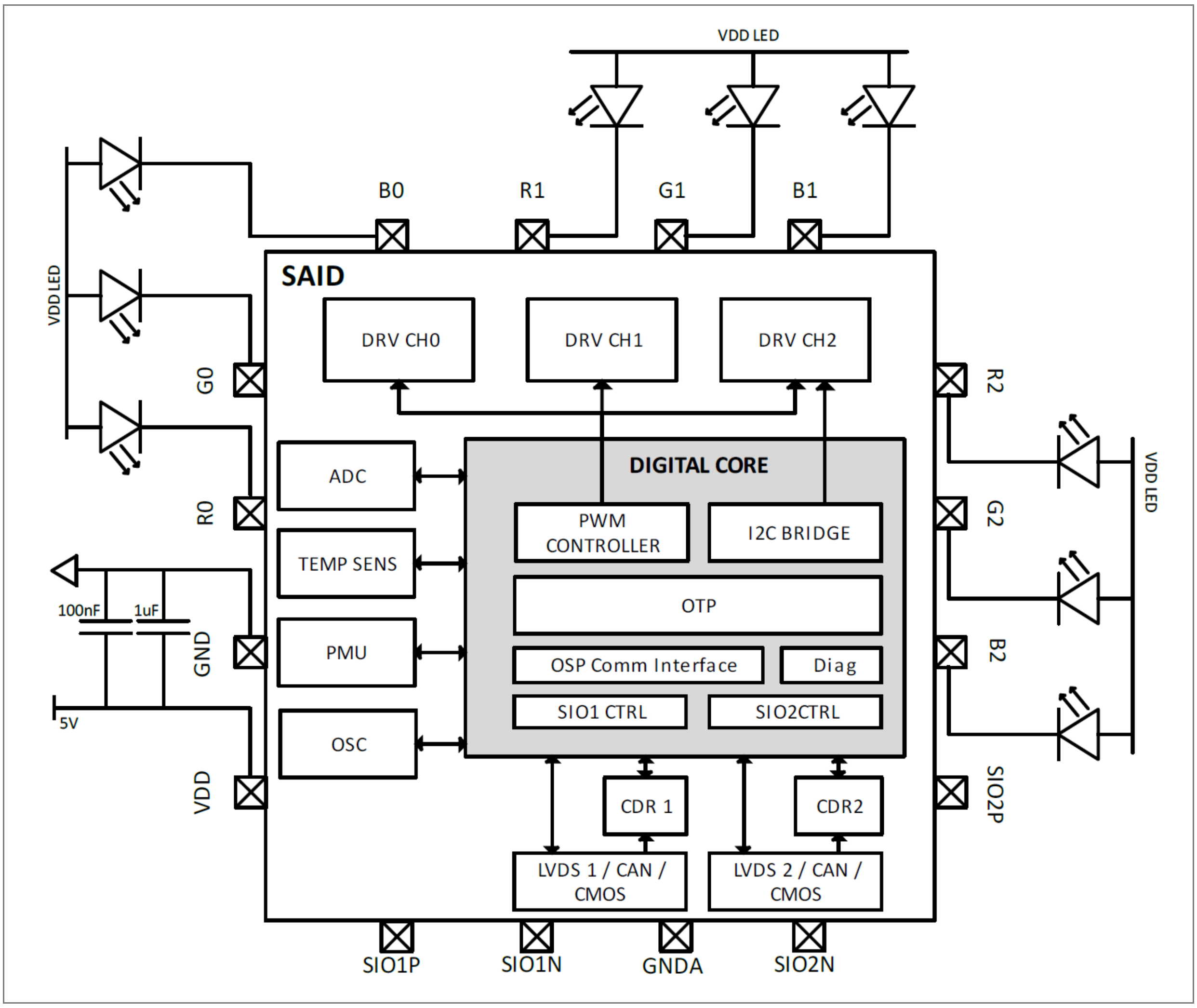


Figure 4 shows parallel connection of SAID devices with direct MCU connection.

1.4 Block diagram

The functional blocks of this device are shown below:

Figure 5: Functional blocks of AS1163



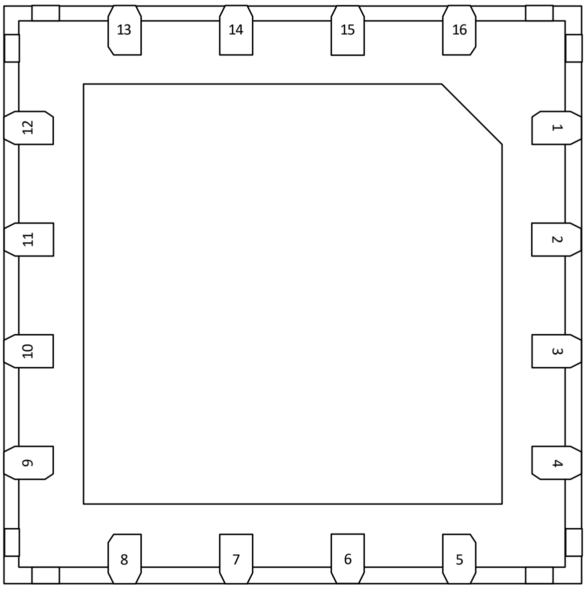
2 Ordering information

Ordering code	Package	Marking	Delivery form	Delivery quantity
Q65113A6575	QFN16	AS1163	Tape & reel	5k pcs/reel
Q65113A9863	QFN16	AS1163	Tape & reel	1k pcs/reel

3 Pin assignment

3.1 Pin diagram

Figure 6: Block diagram and pinout (package bottom view)



(1) The heat pad on bottom side is connected to the device substrate. It is recommended to connect the heat pad to GND or leave it floating, do not connect to any other signal.

3.2 Pin description

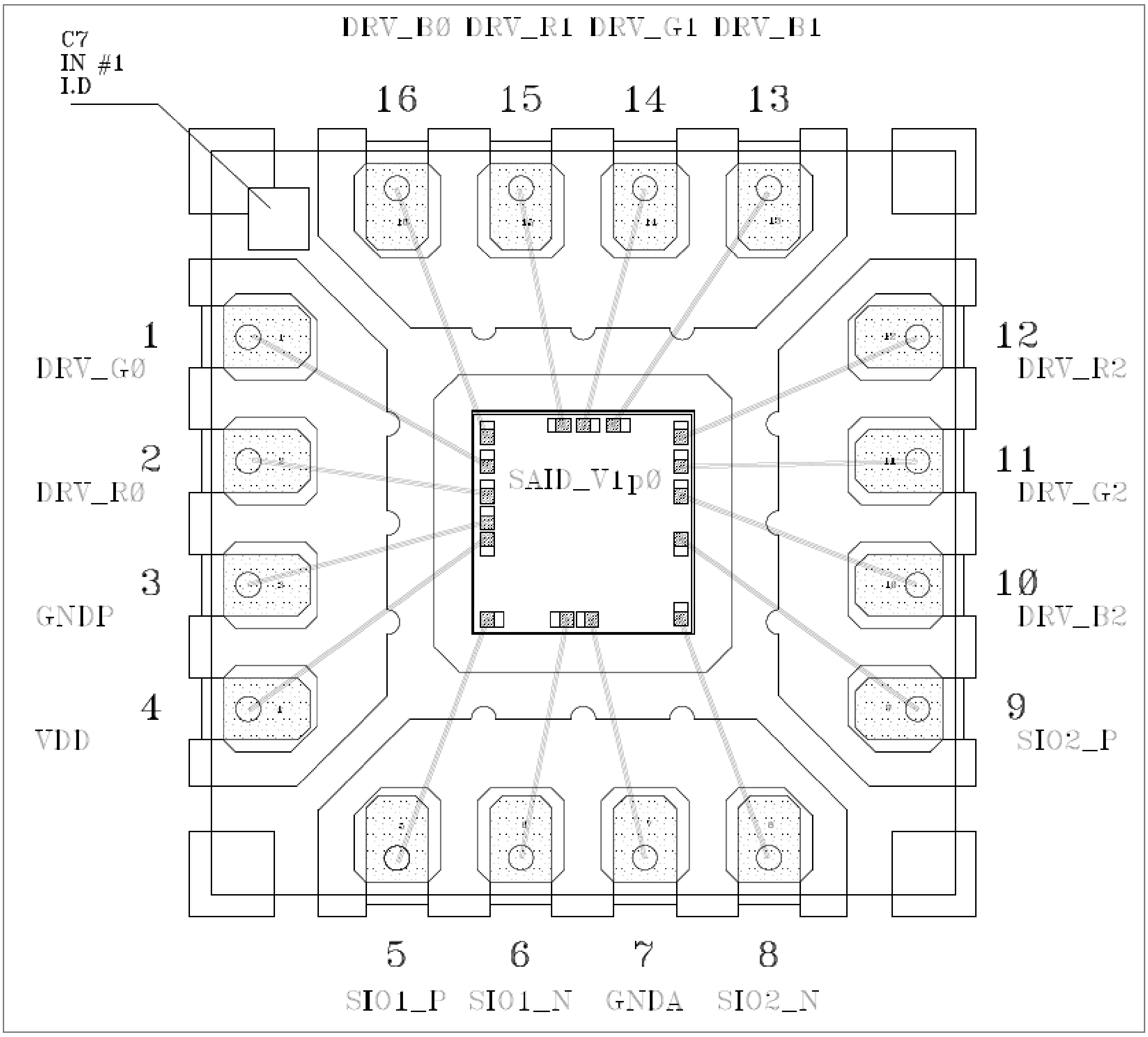
Table 2: Pin description of AS1163

Pin number	Pin name	Pin type(1)	Description(2)
QFN 3x3 16			
1	G0	ANA	Driver 1 of channel 0 (Green)
2	R0	ANA	Driver 0 of channel 0 (Red)
3	GNDP	PWR	Power ground
4	VDD	PWR	5 V power supply
5	SIO1P	ANA/DIO	Positive digital IO for SIO1 interface
6	SIO1N	ANA/DIO	Negative digital IO for SIO1 interface
7	GNDA	PWR	Analog ground
8	SIO2N	ANA/DIO	Negative digital IO for SIO2 interface, test-bus
9	SIO2P	ANA/DIO	Positive digital IO for SIO2 interface, test-bus
10	B2	ANA	Driver 2 of channel 2 (Blue), also INT
11	G2	ANA	Driver 1 of channel 2 (Green), also SCL
12	R2	ANA	Driver 0 of channel 2 (Red), also SDA
13	B1	ANA	Driver 2 of channel 1 (Blue), also SYNC
14	G1	ANA	Driver 1 of channel 1 (Green), also for parallel address configuration
15	R1	ANA	Driver 0 of channel 1 (Red), also for parallel address configuration
16	B0	ANA	Driver 2 of channel 0 (Blue)

(1) Explanation of abbreviations:
DIO Digital input and output
ANA Analog pin
PWR Power pin

(2) Pin name: R, G and B are only for naming purposes, not necessarily to be bound to red, green or blue color.

Figure 7: Pin arrangement (top view)



4 Absolute maximum ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings of AS1163

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
V_{DD} / V_{GND}	Supply voltage to ground	-0.3	7	V	Referenced to GND
V_{IN}	Input pin voltage to ground	-0.3	V_{DD}+0.3	V	
I_{SCR}	Input current (latch-up immunity)	± 100		mA	AEC-Q100-004
Continuous power dissipation (T_A = 70 °C)					
P_T	Continuous power dissipation		600	mW	
Continuous power dissipation (T_A = 125 °C, V_{OUT} = 2.5 V, R_{TH} = 71.6 °C/W)					
P_T	Continuous power dissipation		300	mW	
Electrostatic discharge					
ESD_{HBM}	Electrostatic discharge HBM	± 4		KV	AEC-Q100-002
ESD_{CDM}	Electrostatic discharge CDM	± 500		V	AEC-Q100-011, ±750V for corner pins
Temperature ranges and storage conditions					
T_A	Operating ambient temperature	-40	125	°C	
T_J	Operating junction temperature	-40	150	°C	
T_{STRG}	Storage temperature range	-55	150	°C	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020(1)
RH_{NC}	Relative humidity (non-condensing)	5	85	%	
MSL	Moisture sensitivity level	3			ICP/JEDEC J-STD-033

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100 % Sn).

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Voltages are referred to the GNDA pin unless differently specified.

Table 4: Electrical characteristics of AS1163

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Startup time					1	ms
VDD_com_stop	VDD communication stop (stop of communication when VDD drops below)			2.6		V
VDD	Positive supply voltage		4.3		5.5	V
IDD	Supply current	All drivers at full current		50		mA
IDD_sleep	Sleep current			1.6		mA
IDD_Dsleep	Deep sleep current			1.5		mA
VLED_Head	Min headroom LED driver	1% current compression relative to 2.5V		600		mV
LED_Short	LED short detection threshold		VDD-1.8	VDD-1.2	VDD-0.5	V
LED_Open	LED open detection threshold		50	250	550	mV
LED_Pers	Minimum PWM duration and fault duration for LED_open / LED_Short functionality			27		µs
ILED_abs_acc	LED current absolute accuracy	Max ILED absolute driver accuracy. Over the whole temperature range and max current setting. Tested with VDD=5V	-8.5		8.5	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ILED_C2C_Mis	LED channel to channel matching(1)	Max ILED Channel to Channel over the whole temperature range and max current setting. Tested with VDD=5V	-5		5	%
ILED_Mis	LED channel current matching(2)	Max ILED Driver to Driver (same channel). Over the whole temperature range and max current setting. Tested with VDD=5V	-2.5		2.5	%
ILED_rise/fall	LED rising / falling edge	From 10 to 90%		50		ns
LED Off	LED Off current			3		µA
PWM_freq	PWM freq. fast			1.172		kHz
PWM_freq	PWM freq. slow			0.586		kHz
PWM_res	PWM freq. fast			14		bit
PWM_res	PWM freq. slow			15		bit
PWM_freq_acc	PWM freq. accuracy		-5		5	%
PWM_INL				0.2		LSB
VDD_UV	Under voltage threshold			4.15		V
VDD_UV_HYST	Under voltage hysteresis			100		mV
VTH_Dig	Valid digital input(3)		0.5	0.75	1.2	V
ADC_VREF1				0.365		V
ADC_VREF2				0.972		V
ADC_VREF	Buffered ADC reference			1.340		V
ADC_OS	ADC offset(4)	Vf meas.	-2		2	LSB
ADC_RANGE	Typical input range, Vf mode	Vf meas.	VDD - 8/3 ADC_VREF		VDD	V
ADC_GAIN		Vf meas.		3.494		mV/LSB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ADC_GAIN_ERR	Gain variation	Vf meas, referred to full-scale. Tested with VDD=5V	-1.12		1.12	%
ADC_DNL	DNL	Vf meas. Valid for Tj<125ºC	-1		1	LSB
ADC_INL	INL	Vf meas.	-3		3	LSB
ADC_TSAMPLE		Vf meas.		1.6		µs
T_acc	Temperature sensor accuracy	Room temp.	-8		8	ºC
T_AMB	Ambient temperature		-40		125	ºC
T_J	Junction temperature		-40		150	ºC
Rth	Thermal resistance from junction to ambient temperature			64		°C/W
V_th_se_high	Threshold on SIOx_x to detect communication mode (high)		2.85		VDD+0.3	V
V_th_se_low	Threshold on SIOx_x to detect communication mode (low)		-0.3		0.7	V
V_SIOx_P/N(O,L)	Output low level for pin SIOx_P and SIOx_N for single-ended communication	10k Ohm load	0		0.7	V
V_SIOx_P/N(O,H)	Output high level for pin SIOx_P and SIOx_N for single-ended communication	10k Ohm load	VDD-0.7		VDD	V
F_com_mcu	Allowed input data rate for communication in MCU mode. Tested with VDD=5V.		2.23	2.4	2.62	Mbps
DUTY_com_mcu	Allowed input duty cycle in MCU mode. Tested with VDD=5V.		47.5		52.5	%
F_com_can	Allowed input data rate for communication in CAN RTX mode. Tested with VDD=5V.		2.31	2.4	2.55	Mbps

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DUTY_com_can	Allowed input duty cycle in CAN RTX mode. Tested with VDD=5V.		40		55	%
	Time between consecutive telegrams from MCU	Dependent on length of daisy chain	8.3			µs
VIH_SE	High level input voltage single ended communication		2.4		VDD+0.3	V
VIL_SE	Low level input voltage single ended communication		-0.3		0.7	V
LVDS_VCM	LVDS common mode voltage with active communication			1.2		V
LVDS_VDIFF	LVDS differential voltage			300		mV
LVDS_VCM_IDLE	LVDS common mode voltage with no active communication			0		V
LVDS_RTERM	LVDS termination resistance	Included in the IC		200		Ohm
LVDS_ITX	LVDS current			1.5		mA

(1) Channel to channel relative accuracy is calculated with the following formulas:
ILED_C2C_Mis(ch0_x) = ((0.5*I(ch0_x) **–** average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)) **/** average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)))*100
ILED_C2C_Mis(ch1_x) = ((I(ch1_x) **–** average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)) **/** average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)))*100,
ILED_C2C_Mis(ch2_x) = ((I(ch2_x) **–** average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)) **/** average(0.5*I(ch0_RGB),I(ch1_RGB),I(ch2_RGB)))*100,

Where:
a) ILED_C2C_Mis(ch0_x) refers to a general driver x inside channel 0, for example: ch0_R refers to the R driver in channel 0. Similarly, for ILED_C2C_Mis(ch1_x), ILED_C2C_Mis(ch2_x).
b) I(ch0_x) refers to the high current level of a particular driver in channel 0. Similarly, for I(ch1_x) and I(ch2_x),
c) I(ch0_RGB) refers to the sum of the high current levels for the drivers belonging to channel 0. Similarly, for I(ch1_RGB) and I(ch2_RGB).

(2) In-channel relative accuracy is calculated with the following formula:
ILED_Mis(chx_y) = ((I(chx_y) **–** average(I(chx_RGB))) **/** average(I(chx_RGB)))*100

Where:
a) ILED_Mis(chx_y) refers to a general driver y inside a general channel x, for example: ch0_R refers to the R driver in channel 0.
b) I(chx_y) refers to the high current level of a general driver y in a general channel x.
c) I(chx_RGB) refers to the sum of the high current levels of all drivers belonging to a general channel x.

(3) LED drivers can be used as receiving path for: I²C bridge, Sync pin, parallel address setting by external HW.
(4) Relative accuracy. For absolute accuracy, calibration in applications is necessary.

5.1 Power supply

For operating SAID a voltage supply VDD of typical 5 V is required. Each SAID can sink up to nominal 288 mA from the LEDs and the power delivery network needs to be sized accordingly.

Decoupling caps are recommended between VDD and GND, placed as close as possible to the device power pins.

Recommended values for these caps are:

- 1 µF elco capacity
- 100 nF high ESR capacitor
- VDD voltage up to 6 V

5.2 Startup sequence

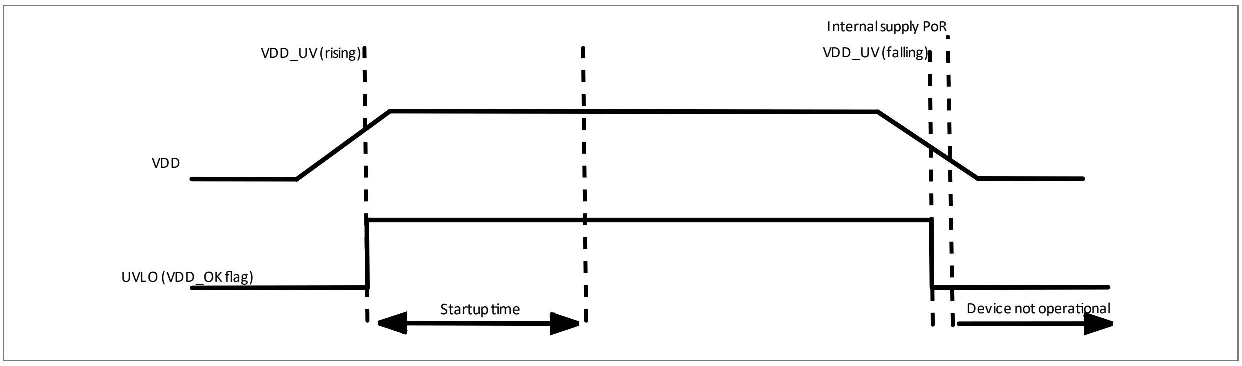
The device starts-up with VDD overcoming the UVLO (undervoltage lockout) threshold. After the bandgap reference starts-up, the voltage regulator generates an internal voltage, VREG.

The internal blocks supplied by VREG (nominally 1.5 V) are reset until the supply reaches the POR_N threshold. The RC oscillator is also enabled with POR_N. In this state, for a trimmed device, the OTP is downloaded, and the trimming/configuration bits activated (~200 µs).

All internal blocks supplied by the external VDD supply start up after the supply reaches the UVLO threshold. At this point the communication interface and the led drivers are functional. Once the communication is enabled, also in case of an under-voltage event, the device does not lose functionality until an internal falling POR_N event. The VDD_OK flag signals that the VDD is above the VDD_UV threshold.

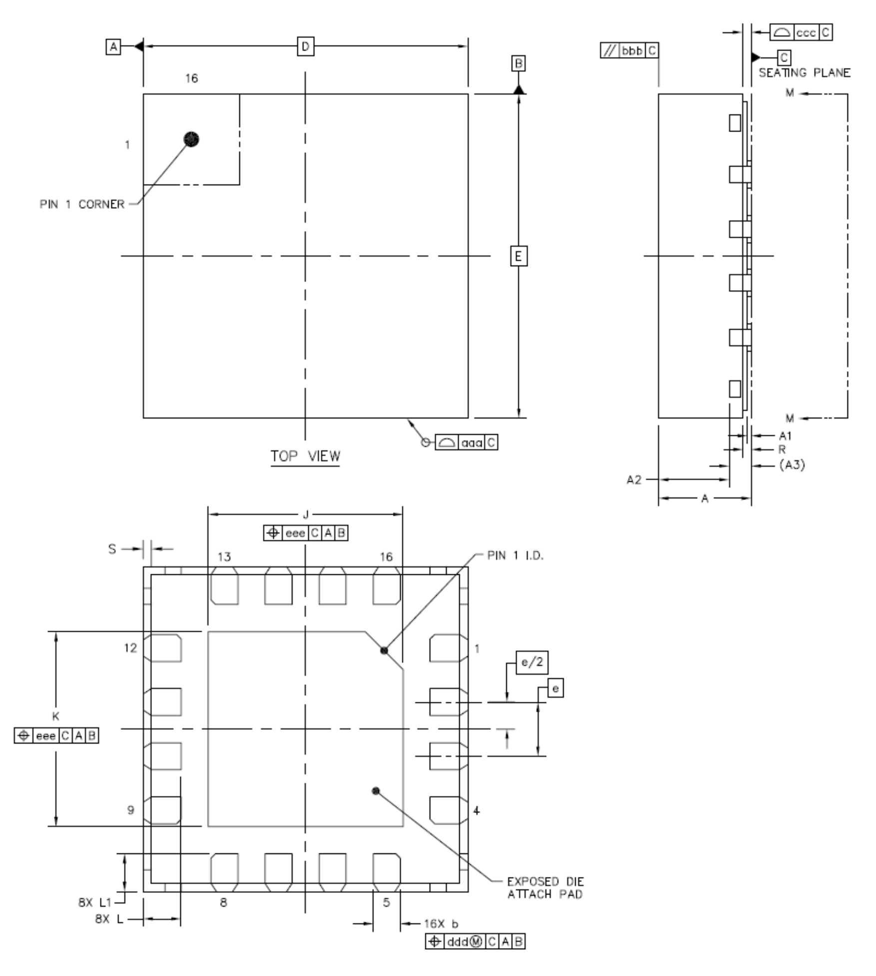
Note: VREG, POR_N are internal signals.

Figure 8: Startup sequence



6 Package drawings & markings

Figure 9: AS1163 package outline drawing



Ref.	Min	Nom	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2		0.65	
A3		0.203	
b	0.2	0.25	0.3
D, E		3	
e		0.5	
J, K	1.7	1.8	1.9
L	0.3	0.35	0.4
L1	0.25	0.35	0.4
aaa,bbb		0.1	
ccc		0.08	
ddd,eee		0.1	

(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5M-1994.
(3) N is the total number of terminals.
(4) This package contains no lead (Pb).
(5) This drawing is subject to change without notice.

7 Tape & reel information

Figure 10: AS1163 tape and reel

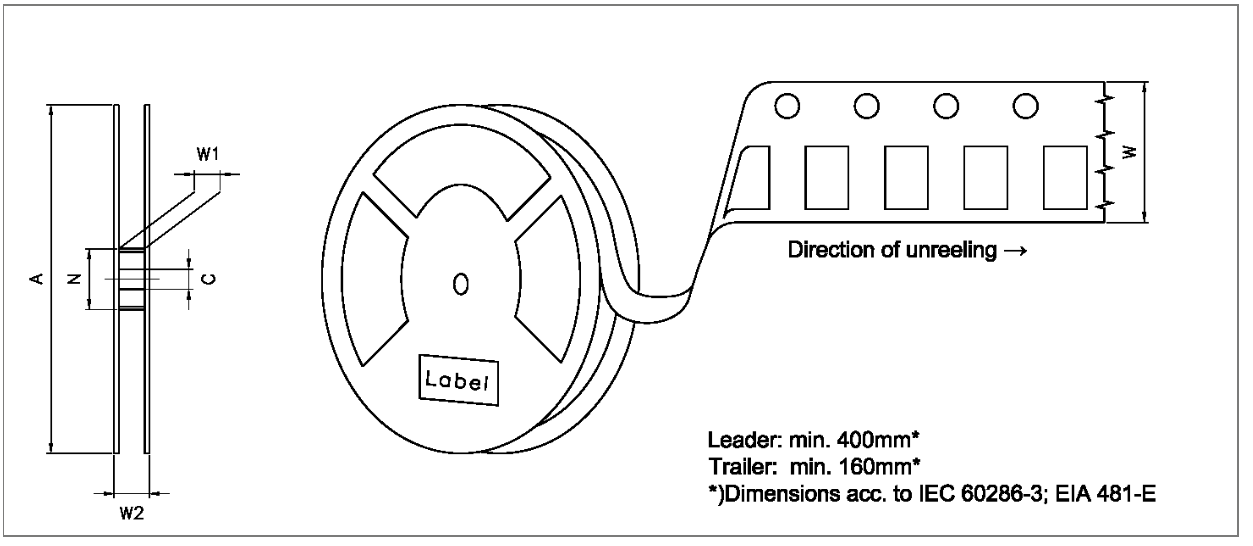


Table 5: Reel dimensions

A	W	N_{min}	W_1	W_{2max}	Pieces per PU
330 mm	12 + 0.3/-0.3 mm	102 mm	12.8 mm	18.2 mm	5000
180 mm	12 + 0.3/-0.3 mm	60 mm	12.4 +2/-0 mm	18.4 mm max	1000

8 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Changes from previous version to current revision v1-00	Page
This short datasheet is derived from v1-00 of full datasheet	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

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