Product Document

Published by
ams OSRAM Group

TSL2591

Light-to-Digital Converter

General Description

The TSL2591 is a very-high sensitivity light-to-digital converter that transforms light intensity into a digital signal output capable of direct I^2C interface. The device combines one broadband photodiode (visible plus infrared) and one infrared-responding photodiode on a single CMOS integrated circuit. Two integrating ADCs convert the photodiode currents into a digital output that represents the irradiance measured on each channel. This digital output can be input to a microprocessor where illuminance (ambient light level) in lux is derived using an empirical formula to approximate the human eye response. The TSL2591 supports a traditional level style interrupt that remains asserted until the firmware clears it.

Ordering Information and Content Guide appear at end of datasheet.

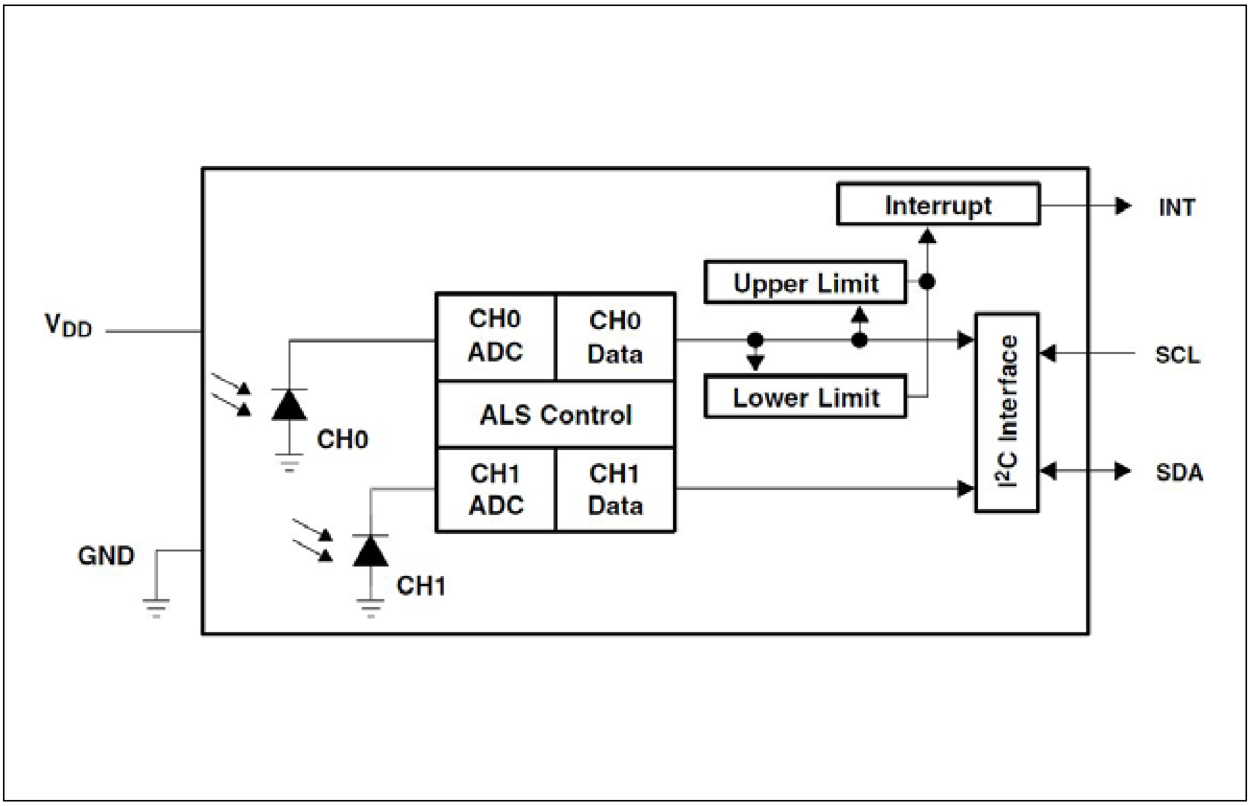
Figure 1:
Added Value of Using TSL2591

Benefits	Features
• Approximates Human Eye Response	• Dual Diode
• Flexible Operation	• Programmable Analog Gain and Integration Time
• Suited for Operation Behind Dark Glass	• 600M:1 Dynamic Range
• Low Operating Overhead	• Two Internal Interrupt Sources • Programmable Upper and Lower Thresholds • One Interrupt Includes Programmable Persistence Filter
• Low Power 3.0 µA Sleep State	• User Selectable Sleep Mode
• I^2C Fast Mode Compatible Interface	• Data Rates up to 400 kbit/s • Input Voltage Levels Compatible with 3.0V Bus

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Block Diagram



Detailed Description

The TSL2591 contains two integrating analog-to-digital converters (ADC) that integrate currents from two photodiodes. Integration of both channels occurs simultaneously. Upon completion of the conversion cycle, the conversion result is transferred to the Channel 0 and Channel 1 data registers, respectively. The transfers are double-buffered to ensure that the integrity of the data is maintained. After the transfer, the device automatically begins the next integration cycle.

Communication with the device is accomplished through a standard, two-wire I^2C serial bus. Consequently, the TSL2591 can be easily connected to a microcontroller or embedded controller. No external circuitry is required for signal conditioning. Because the output of the device is digital, the output is effectively immune to noise when compared to an analog signal.

The TSL2591 also supports an interrupt feature that simplifies and improves system efficiency by eliminating the need to poll a sensor for a light intensity value. The primary purpose of the interrupt function is to detect a meaningful change in light intensity. The concept of a meaningful change can be defined by the user both in terms of light intensity and time, or persistence, of that change in intensity. The device has the ability to define two sets of thresholds, both above and below the current light level. An interrupt is generated when the value of a conversion exceeds either of these limits. One set of thresholds can be configured to trigger an interrupt only when the ambient light exceeds them for a configurable amount of time (persistence) while the other set can be configured to trigger an immediate interrupt.

Pin Assignment

The TSL2591 pin assignments are described below.

Figure 3:
Pin Diagram

Package FN Dual Flat No-Lead (Top View): Package drawing is not to scale.

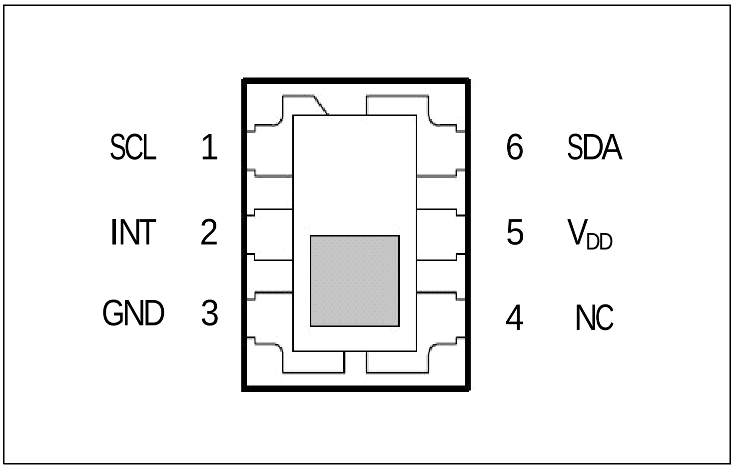


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	SCL	I²C serial clock input terminal
2	INT	Interrupt — open drain output (active low).
3	GND	Power supply ground. All voltages are referenced to GND.
4	NC	No connect — do not connect.
5	V_{DD}	Supply voltage
6	SDA	I²C serial data I/O terminal

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Supply voltage, V_{DD}		3.8	V	All voltages are with respect to GND
Input terminal voltage	-0.5	3.8	V	
Output terminal voltage	-0.5	3.8	V	
Output terminal current	-1	20	mA	
Storage temperature range, T_{stg}	-40	85	°C	
ESD tolerance, human body model	±2000		V	JESD22-A114-B
ESD tolerance, charge device model (CDM)	±500		V	JESD22-C101

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods. Device parameters are guaranteed at T_A = 25°C unless otherwise noted.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage	2.7	3	3.6	V
T_A	Operating free-air temperature	-30		70	°C

Figure 7:
Operating Characteristics, V_{DD} = 3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply Current	Active Sleep state - no I²C activity		275 2.3	325 4	µA
V_{OL}	INT, SDA output low voltage	3mA sink current 6mA sink current	0 0		0.4 0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	µA
V_{IH}	SCL, SDA input high voltage	TSL25911 ($V_{bus} = V_{DD}$)	0.7 V_{DD}			V
		TSL25913 (V_{bus} = 1.8)	1.26			
V_{IL}	SCL, SDA input low voltage	TSL25911 ($V_{bus} = V_{DD}$)			0.3 V_{DD}	V
		TSL25913 (V_{bus} = 1.8)			0.54	

Figure 8:
ALS Characteristics, V_{DD} = 3V, T_A = 25°C, AGAIN = High, AEN = 1, (unless otherwise noted)(1) (2) (3)

Parameter	Conditions	Channel	Min	Typ	Max	Units
Dark ADC count value	$E_e = 0$, AGAIN = Max, ATIME=000b (100ms)	CH0 CH1	0 0		20 20	counts
ADC integration time step size	ATIME = 000b (100ms)		95	100	105	ms
ADC number of integration steps (4)			1		6	steps
Max ADC count	ATIME = 000b (100ms)		0		36863	counts
Max ADC count	ATIME = 001b (200ms), 010b (300ms), 011b (400ms), 100b (500ms), 101b (600ms)		0		65535	counts
ADC count value	White light (2) $E_e = 4.98\ \mu W/cm^2$ ATIME = 000b (100 ms)	CH0 CH1	1120	1315 174	1510	counts
	$\lambda_P = 850$ nm (3) $E_e = 5.62\ \mu W/cm^2$, ATIME = 000b (100 ms)	CH0 CH1	1230	1447 866	1665	counts
ADC count value ratio: CH1/CH0	White light (2)		0.092	0.132	0.172	
	$\lambda_P = 850$ nm (3)		0.558	0.598	0.638	
R_e Irradiance responsivity	White light (2) ATIME = 000b (100 ms)	CH0 CH1		264.1 34.9		counts/ ($\mu W/cm^2$)
	$\lambda_P = 850$ nm (3) ATIME = 000b (100 ms)	CH0 CH1		257.5 154.1		
Noise (4)	White light (2) $E_e = 4.98\ \mu W/cm^2$ ATIME = 000b (100 ms)	CH0		1	2	1 standard deviation

Parameter	Conditions	Channel	Min	Typ	Max	Units
Gain scaling, relative to 1x gain setting (AGAIN = Low)	AGAIN = Med	CH0 CH1	22 22	24.5 24.5	27 27	x
	AGAIN = High	CH0 CH1	360 360	400 400	440 440	
	AGAIN = Max	CH0 CH1	8500 9100	9200 9900	9900 10700	

Note(s):

1. Optical measurements are made using small-angle incident radiation from light-emitting diode optical sources. Visible white LEDs and infrared 850 nm LEDs are used for final product testing for compatibility with high-volume production
2. The white LED irradiance is supplied by a white light-emitting diode with a nominal color temperature of 4000 K.
3. The 850 nm irradiance is supplied by a GaAs light-emitting diode with the following typical characteristics: peak wavelength λ_P = 850 nm and spectral halfwidth $\Delta\lambda½$ = 42 nm.
4. Parameter ensured by design and is not 100% tested.

Timing Characteristics

The timing characteristics of TSL2591 are given below.

Figure 9:
AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

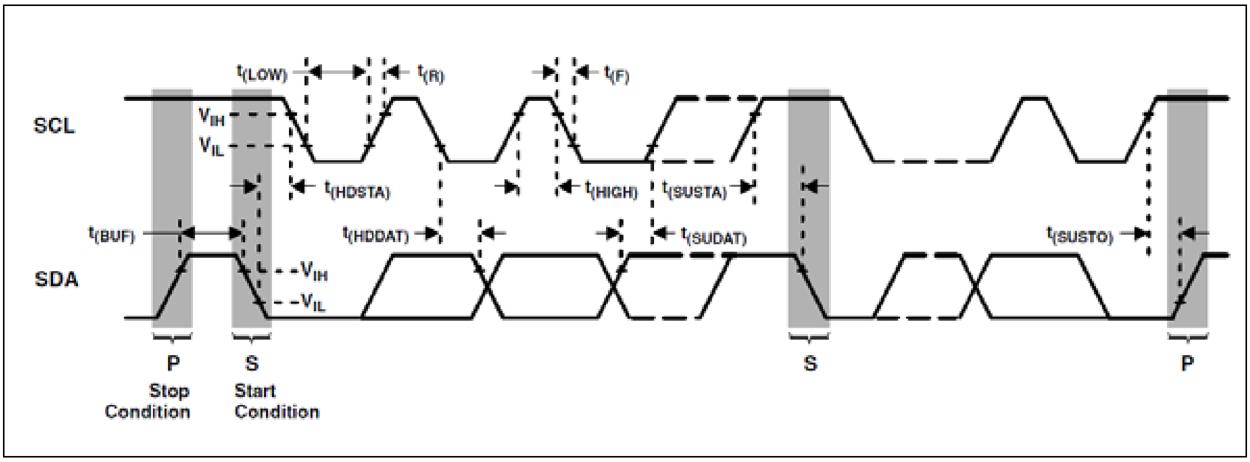
Parameter [1]	Description	Min	Typ	Max	Units
$f_{(SCL)}$	Clock frequency (I^2C only)	0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(HDDAT)}$	Data hold time	0			µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns
C_i	Input pin capacitance			10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagrams

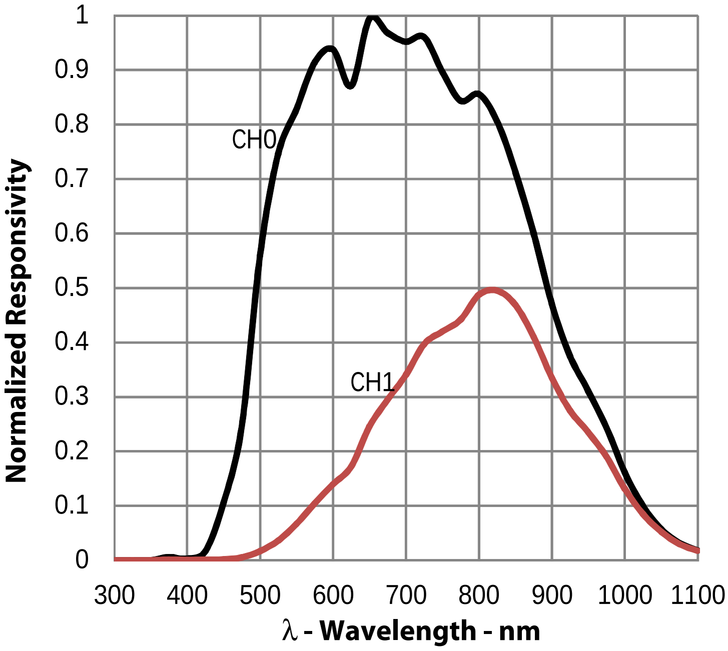
Figure 10:
Parameter Measurement Information



Typical Operating Characteristics

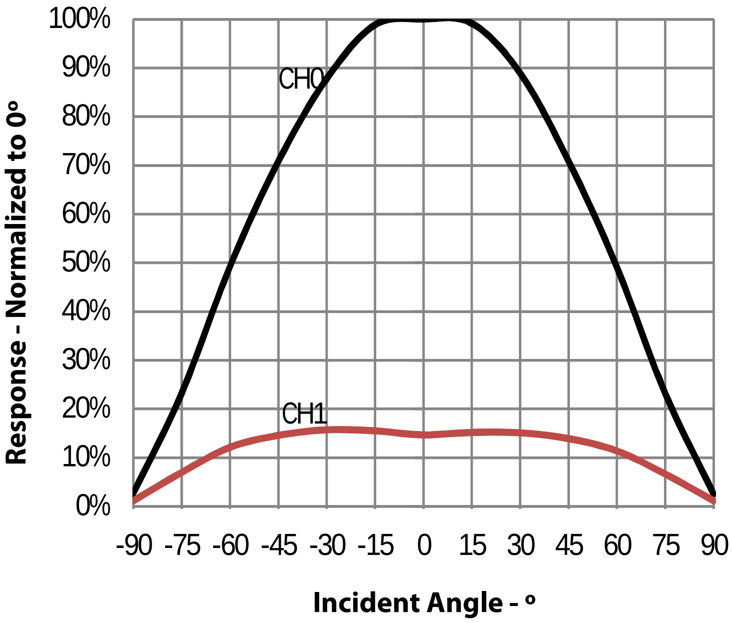
Spectral Responsivity: Two channel response allows for tunable illuminance (lux) calculation regardless of transmissivity of glass.

Figure 11:
Spectral Responsivity



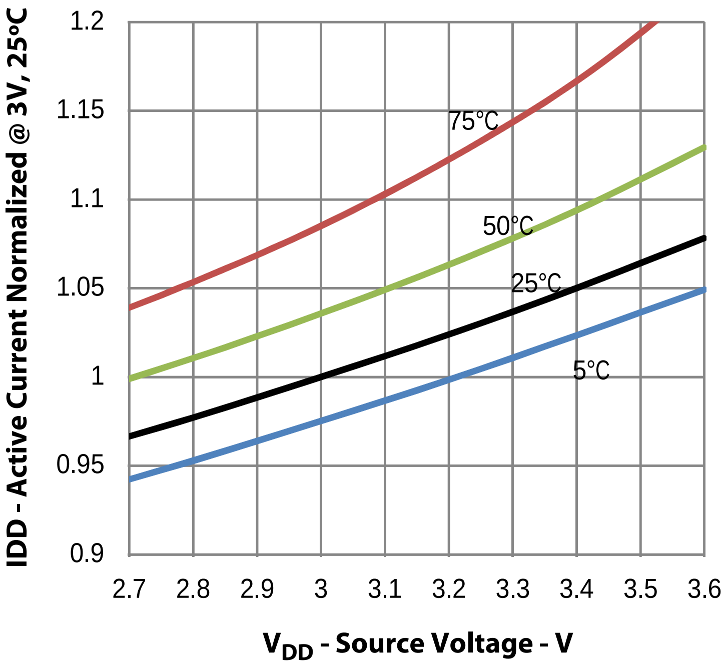
White LED Angular Response: Near cosine angular response for broadband white light sources.

Figure 12:
White Normalized Responsivity vs. Angular Displacement



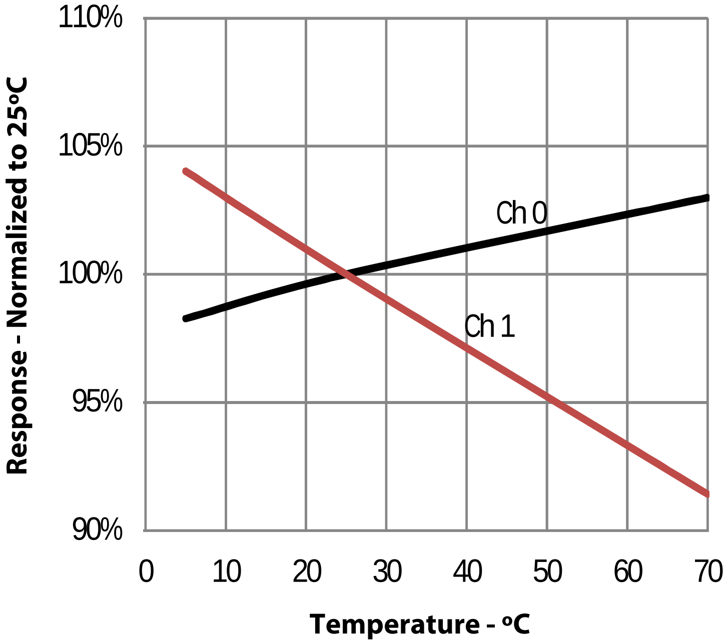
I_{DD} vs. V_{DD} and Temp: Effect of supply voltage and temperature on active current.

Figure 13:
Normalized I_{DD} vs. V_{DD} and Temperature



White LED Response vs. Temp: Effect of temperature on the device response for a broadband white light source.

Figure 14:
Response to White LED vs. Temperature



Register Description

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 15.

Figure 15:
Register Description

Address	Register Name	R/W	Register Function	Reset Value
--	COMMAND	W	Specifies Register Address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	CONFIG	R/W	ALS gain and integration time configuration	0x00
0x04	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x05	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x08	NPAILTL	R/W	No Persist ALS interrupt low threshold low byte	0x00
0x09	NPAILTH	R/W	No Persist ALS interrupt low threshold high byte	0x00
0x0A	NPAIHTL	R/W	No Persist ALS interrupt high threshold low byte	0x00
0x0B	NPAIHTH	R/W	No Persist ALS interrupt high threshold high byte	0x00
0x0C	PERSIST	R/W	Interrupt persistence filter	0x00
0x11	PID	R	Package ID	--
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	C0DATAL	R	CH0 ADC low data byte	0x00
0x15	C0DATAH	R	CH0 ADC high data byte	0x00
0x16	C1DATAL	R	CH1 ADC low data byte	0x00
0x17	C1DATAH	R	CH1 ADC high data byte	0x00

Note(s):

1. Devices with a primary I²C address of 0x29 also have a secondary I²C address of 0x28 that can be used for read only registers to quickly read in a single block I²C transaction.

Command Register

The COMMAND register specifies the address of the target register for future read and write operations, as well as issues special function commands.

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>CMD</td><td colspan="2">TRANSACTION</td><td colspan="5">ADDR/SF</td></tr>
</table>

<table>
<tr><th>Fields</th><th>Bits</th><th colspan="2">Description</th></tr>
<tr><td>CMD</td><td>7</td><td colspan="2">Select Command Register. Must write as 1 when addressing COMMAND register.</td></tr>
<tr><td rowspan="6">TRANSACTION</td><td rowspan="6">6:5</td><td colspan="2">Select type of transaction to follow in subsequent data transfers.</td></tr>
<tr><td>FIELD VALUE</td><td>DESCRIPTION</td></tr>
<tr><td>00</td><td>Reserved - Do not use</td></tr>
<tr><td>01</td><td>Normal Operation</td></tr>
<tr><td>10</td><td>Reserved – Do not use</td></tr>
<tr><td>11</td><td>Special Function – See description below</td></tr>
<tr><td rowspan="8">ADDR/SF</td><td rowspan="8">4:0</td><td colspan="2">Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-data register for subsequent read and write transactions. The field values listed below apply only to special function commands.</td></tr>
<tr><td>FIELD VALUE</td><td>DESCRIPTION</td></tr>
<tr><td>00100</td><td>Interrupt set – forces an interrupt</td></tr>
<tr><td>00110</td><td>Clears ALS interrupt</td></tr>
<tr><td>00111</td><td>Clears ALS and no persist ALS interrupt</td></tr>
<tr><td>01010</td><td>Clears no persist ALS interrupt</td></tr>
<tr><td>Other</td><td>Reserved – Do not write</td></tr>
<tr><td colspan="2">The interrupt set special function command sets the interrupt bits in the status register (0x13). For the interrupt to be visible on the INT pin, one of the interrupt enable bits in the enable register (0x00) must be asserted.
The interrupt set special function must be cleared with an interrupt clear special function. The ALS interrupt clear special functions clear any pending interrupt(s) and are self-clearing.</td></tr>
</table>

Enable Register (0x00)

The ENABLE register is used to power the device on/off, enable functions and interrupts.

7	6	5	4	3	2	1	0
NPIEN	SAI	Reserved	AIEN	Reserved		AEN	PON

Fields	Bits	Description
NPIEN	7	No Persist Interrupt Enable. When asserted NP Threshold conditions will generate an interrupt, bypassing the persist filter.
SAI	6	Sleep after interrupt. When asserted, the device will power down at the end of an ALS cycle if an interrupt has been generated.
Reserved	5	Reserved. Write as 0.
AIEN	4	ALS Interrupt Enable. When asserted permits ALS interrupts to be generated, subject to the persist filter.
Reserved	3:2	Reserved. Write as 0.
AEN	1	ALS Enable. This field activates ALS function. Writing a one activates the ALS. Writing a zero disables the ALS.
PON	0	Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator.

Control Register (0x01)

The CONTROL register is used to configure the ALS gain and integration time. In addition, a system reset is provided. Upon power up, the CONTROL register resets to 0x00.

7	6	5	4	3	2	1	0
SRESET	Reserved	AGAIN		Reserved	ATIME		

<table>
<tr><th>Fields</th><th>Bits</th><th colspan="3">Description</th></tr>
<tr><td>SRESET</td><td>7</td><td colspan="3">System reset. When asserted, the device will reset equivalent to a power-on reset. SRESET is self-clearing.</td></tr>
<tr><td>Reserved</td><td>6</td><td colspan="3">Reserved. Write as 0.</td></tr>
<tr><td rowspan="6">AGAIN</td><td rowspan="6">5:4</td><td colspan="3">ALS gain sets the gain of the internal integration amplifiers for both photodiode channels.</td></tr>
<tr><td>FIELD VALUE</td><td colspan="2">DESCRIPTION</td></tr>
<tr><td>00</td><td colspan="2">Low gain mode</td></tr>
<tr><td>01</td><td colspan="2">Medium gain mode</td></tr>
<tr><td>10</td><td colspan="2">High gain mode</td></tr>
<tr><td>11</td><td colspan="2">Maximum gain mode</td></tr>
<tr><td>Reserved</td><td>3</td><td colspan="3">Reserved. Write as 0.</td></tr>
<tr><td rowspan="8">ATIME</td><td rowspan="8">2:0</td><td colspan="3">ALS time sets the internal ADC integration time for both photodiode channels.</td></tr>
<tr><td>FIELD VALUE</td><td>INTEGRATION TIME</td><td>MAX COUNT</td></tr>
<tr><td>000</td><td>100 ms</td><td>36863</td></tr>
<tr><td>001</td><td>200 ms</td><td>65535</td></tr>
<tr><td>010</td><td>300 ms</td><td>65535</td></tr>
<tr><td>011</td><td>400 ms</td><td>65535</td></tr>
<tr><td>100</td><td>500 ms</td><td>65535</td></tr>
<tr><td>101</td><td>600 ms</td><td>65535</td></tr>
</table>

ALS Interrupt Threshold Register (0x04 - 0x0B)

The ALS interrupt threshold registers provide the values to be used as the high and low trigger points for the comparison function for interrupt generation. If C0DATA crosses below the low threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

If the C0DATA exceeds the persist thresholds (registers: 0x04 - 0x07) for the number of persist cycles configured in the PERSIST register an interrupt will be triggered. If the C0DATA exceeds the no-persist thresholds (registers: 0x08 - 0x0B) an interrupt will be triggered immediately following the end of the current integration.

Note that while the interrupt is observable in the STATUS register (0x13), it is visible only on the INT pin when AIEN or NPIEN are enabled in the ENABLE register (0x00).

Upon power up, the interrupt threshold registers default to 0x00.

Register	Address	Bits	Description
AILTL	0x04	7:0	ALS low threshold lower byte
AILTH	0x05	7:0	ALS low threshold upper byte
AIHTL	0x06	7:0	ALS high threshold lower byte
AIHTH	0x07	7:0	ALS high threshold upper byte
NPAILTL	0x08	7:0	No Persist ALS low threshold lower byte
NPAILTH	0x09	7:0	No Persist ALS low threshold upper byte
NPAIHTL	0x0A	7:0	No Persist ALS high threshold lower byte
NPAIHTH	0x0B	7:0	No Persist ALS high threshold upper byte

PERSIST Register (0x0C)

The Interrupt persistence filter sets the number of consecutive out-of-range ALS cycles necessary to generate an interrupt. Out-of-range is determined by comparing C0DATA (0x14 and 0x15) to the interrupt threshold registers (0x04 - 0x07). Note that the no-persist ALS interrupt is not affected by the interrupt persistence filter. Upon power up, the interrupt persistence filter register resets to 0x00.

7	6	5	4	3	2	1	0
Reserved				APERS			

Field	Bits	Description	
Reserved	7:4	Reserved. Write as 0.	
APERS	3:0	ALS interrupt persistence filter	
		FIELD VALUE	**PERSISTENCE**
		0000	Every ALS cycle generates an interrupt
		0001	Any value outside of threshold range
		0010	2 consecutive values out of range
		0011	3 consecutive values out of range
		0100	5 consecutive values out of range
		0101	10 consecutive values out of range
		0110	15 consecutive values out of range
		0111	20 consecutive values out of range
		1000	25 consecutive values out of range
		1001	30 consecutive values out of range
		1010	35 consecutive values out of range
		1011	40 consecutive values out of range
		1100	45 consecutive values out of range
		1101	50 consecutive values out of range
		1110	55 consecutive values out of range
		1111	60 consecutive values out of range

PID Register (0x11)

The PID register provides an identification of the devices package. This register is a read-only register whose value never changes.

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="2">Reserved</td><td colspan="2">PACKAGEID</td><td colspan="4">Reserved</td></tr>
</table>

Field	Bits	Description
Reserved	7:6	Reserved.
PID	5:4	Package Identification = 00
Reserved	3:0	Reserved.

ID Register (0x12)

The ID register provides the device identification. This register is a read-only register whose value never changes.

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">ID</td></tr>
</table>

Field	Bits	Description
ID	7:0	Device Identification = 0x50

Status Register (0x13)

The Status Register provides the internal status of the device. This register is read only.

7	6	5	4	3	2	1	0
Reserved		NPINTR	AINT	Reserved			AVALID

Field	Bits	Description
Reserved	7:6	Reserved. Write at zero.
NPINTR	5	No-persist Interrupt. Indicates that the device has encountered a no-persist interrupt condition.
AINT	4	ALS Interrupt. Indicates that the device is asserting an ALS interrupt.
Reserved	3:1	Reserved.
AVALID	0	ALS Valid. Indicates that the ADC channels have completed an integration cycle since the AEN bit was asserted.

ALS Data Register (0x14 - 0x17)

ALS data is stored as two 16-bit values; one for each channel. When the lower byte of either channel is read, the upper byte of the same channel is latched into a shadow register. The shadow register ensures that both bytes are the result of the same ALS integration cycle, even if additional integration cycles occur between the lower byte and upper byte register readings.

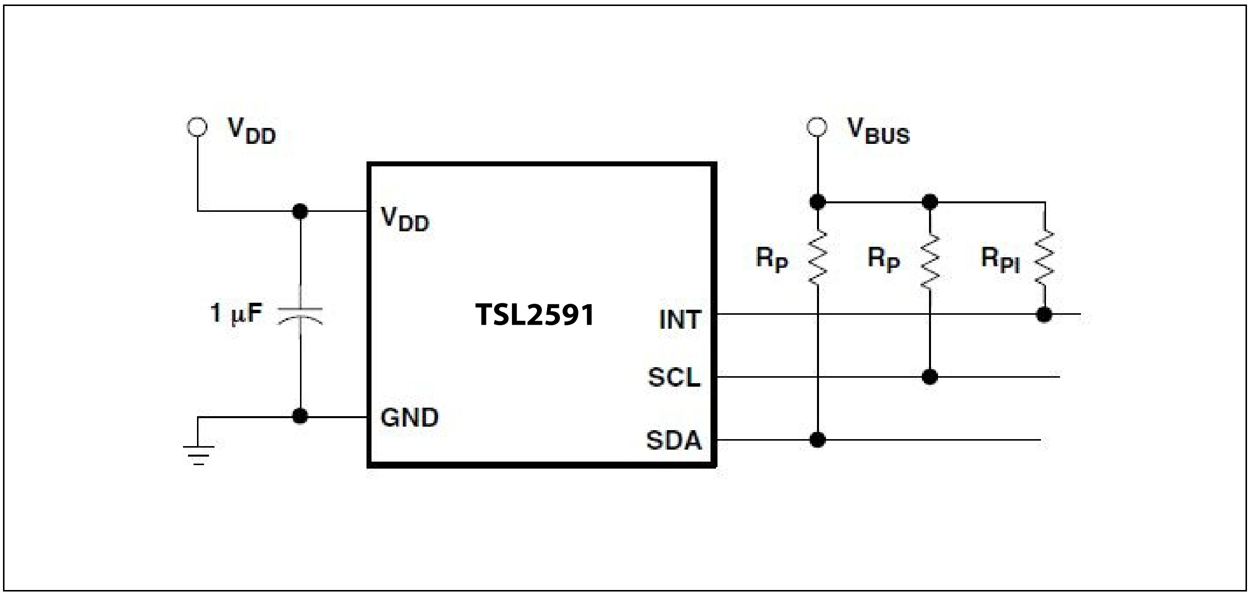
Each channel independently operates the upper byte shadow register. So to minimize the potential for skew between CH0 and CH1 data, it is recommended to read all four ADC bytes in sequence.

Register	Address	Bits	Description
C0DATAL	0x14	7:0	ALS CH0 data low byte
C0DATAH	0x15	7:0	ALS CH0 data high byte
C1DATAL	0x16	7:0	ALS CH1 data low byte
C1DATAH	0x17	7:0	ALS CH1 data high byte

Application Information

Figure 16 shows a typical hardware application circuit. A 1-µF low-ESR decoupling capacitor should be placed as close as possible to the V_{DD} pin. V_{BUS} in this figure refers to the I²C bus voltage, which is equal to V_{DD}.

Figure 16:
Typical Application Hardware Circuit

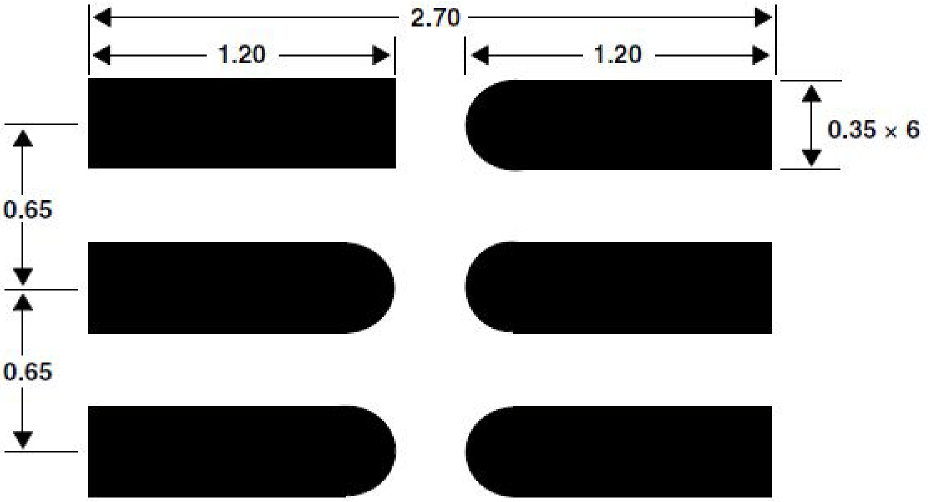


The I²C signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (RP) value is a function of the I²C bus speed, the I²C bus voltage, and the capacitive load. The ams OSRAM EVM running at 400 kbps, uses 1.5-kΩ resistors. A 10-kΩ pull-up resistor (RPI) can be used for the interrupt line.

PCB Pad Layout

Suggested land pattern based on the IPC−7351B Generic Requirements for Surface Mount Design and Land Pattern Standard (2010) for the small outline no-lead (SON) package is shown in Figure 17.

Figure 17:
Suggested FN Package PCB Layout (Top View)

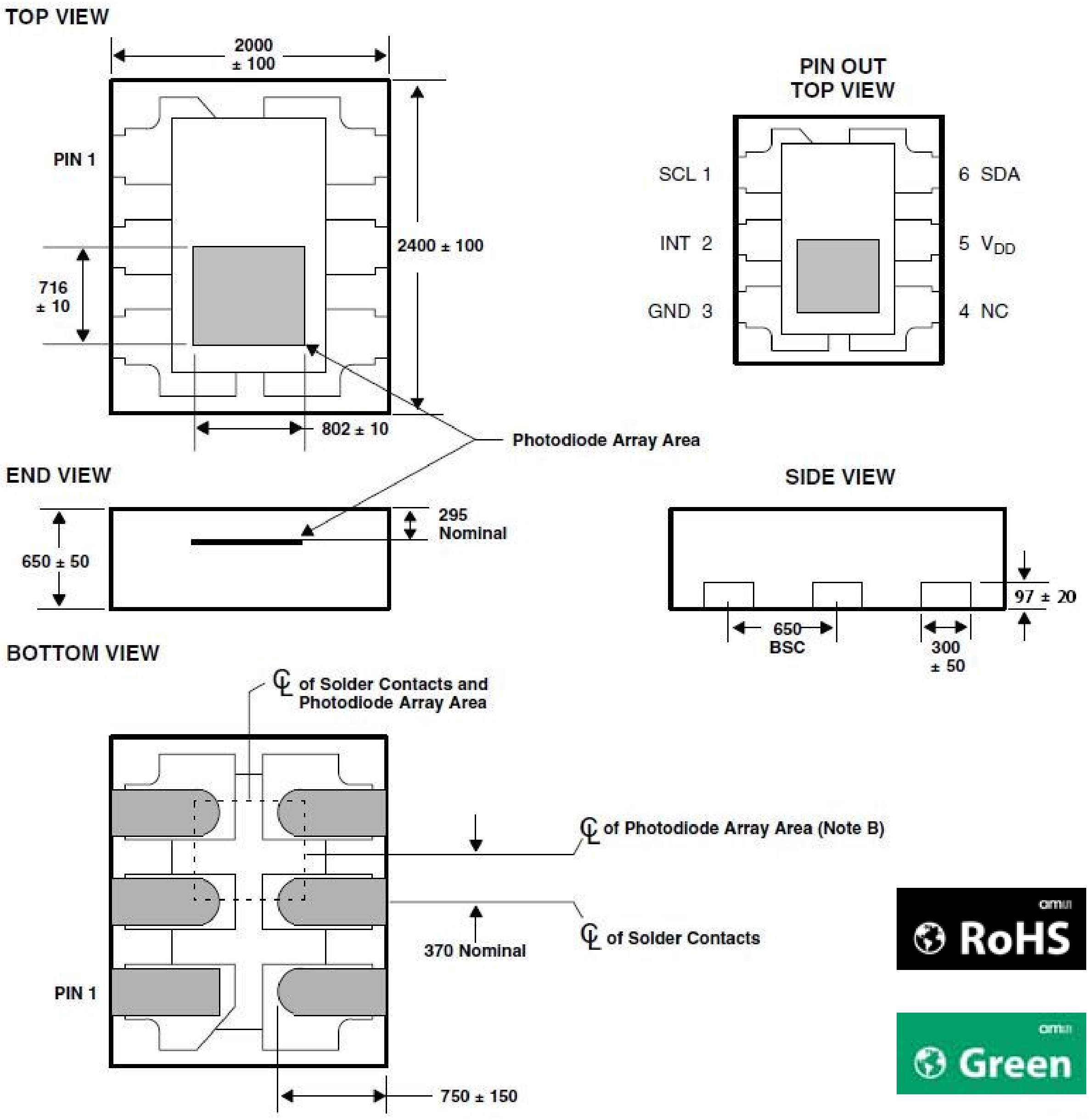


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Package Drawings & Markings

Figure 18:
FN Package – Dual Flat No-Lead Packaging Configuration

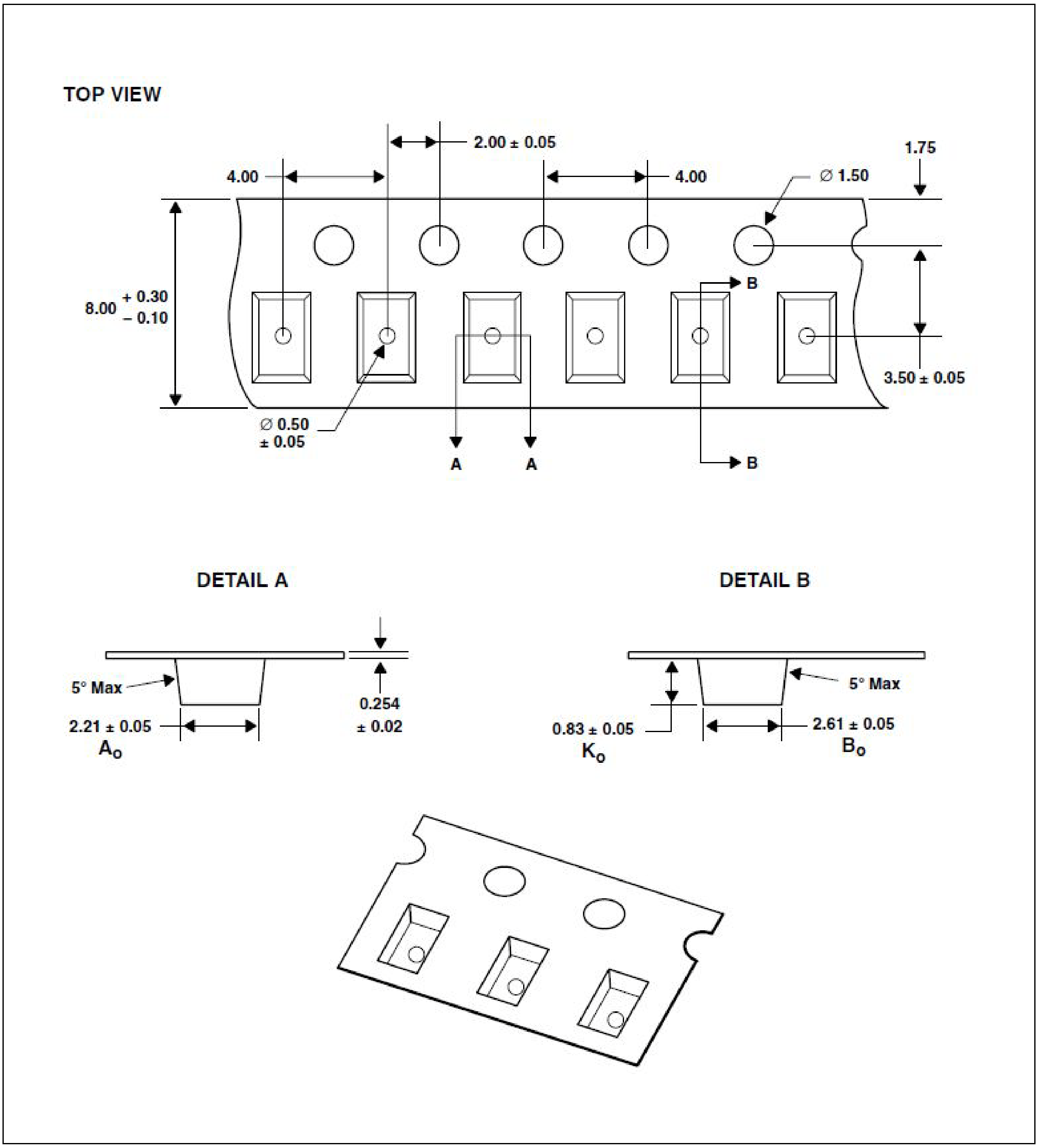


Note(s):

1. All linear dimensions are in micrometers.
2. The die is centered within the package within a tolerance of ±75 μm.
3. Package top surface is molded with an electrically non-conductive clear plastic compound having an index of refraction of 1.55.
4. Contact finish is copper alloy A194 with pre-plated NiPdAu lead finish.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

Mechanical Data

Figure 19:
FN Package Carrier Tape and Reel Information



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A_O, B_O and K_O are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 178 millimeters in diameter and contains 3500 parts.
5. ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481 - B.
6. In accordance with EIA Standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering Information

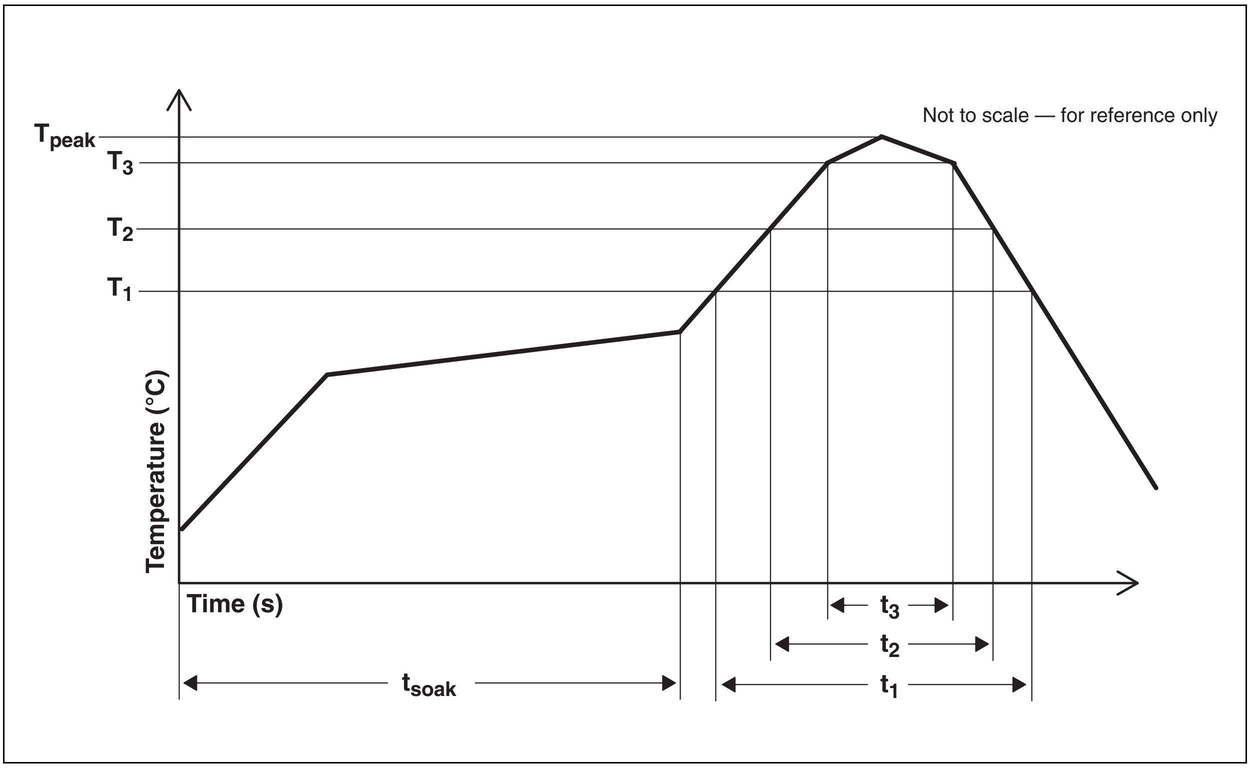
The package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Figure 20:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T_1)	t_1	Max 60 s
Time above 230 °C (T_2)	t_2	Max 50 s
Time above T_{peak} - 10 °C (T_3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/s

Figure 21:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping.

Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The FN package has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 22:
Ordering Information

Ordering Code	Address	Interface	Delivery Form
TSL25911FN	0x29	I^2C $V_{bus} = V_{DD}$ Interface	ODFN-6

Buy our products or get free samples online at:
www.ams.com/Product

Technical Support is available at:
www.ams.com/Technical-Support

Provide feedback about this document at:
www.ams.com/Document-Feedback

For further information and requests, e-mail us at:
ams_sales@ams.com

For sales offices, distributors and representatives, please visit:
www.ams.com/Contact

Headquarters
ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe

Tel: +43 (0) 3136 500 0

Website: www.ams.com

RoHS Compliant & ams Green Statement

RoHS: The term RoHS compliant means that ams-OSRAM AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment EU 2015/863), including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

Important Information: The information provided in this statement represents ams-OSRAM AG knowledge and belief as of the date that it is provided. ams-OSRAM AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams-OSRAM AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams-OSRAM AG and ams-OSRAM AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Copyrights & Disclaimer

Copyright ams-OSRAM AG, Tobelbader Strasse 30, 8141 Premstaetten, Austria-Europe. Trademarks Registered. All rights reserved. The material herein may not be reproduced, adapted, merged, translated, stored, or used without the prior written consent of the copyright owner.

Devices sold by ams-OSRAM AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams-OSRAM AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams-OSRAM AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams-OSRAM AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams-OSRAM AG for each application. This product is provided by ams-OSRAM AG "AS IS" and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams-OSRAM AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams-OSRAM AG rendering of technical or other services.

Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 2-04 (2018-Jun-05) to current revision 3-00 (2023-Feb-08)	Page
Updated "Shelf Life" to 24 months	27
Updated Ordering Information	28

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide